TEXAS INSTRUMENTS

Cache Memory Management

Data Book

Data Book

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1990

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Datapath VLSI Products

Cache Memory Management Data Book

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INTRODUCTION

In this data book, Texas Instruments presents technical information on the Cache Memory Management product lines. This data book includes specifications and operational information on the following high-performance Advanced-CMOS, NMOS, and Bipolar products:

- Cache
- Dynamic Memory Support
- Error Detection and Correction Circuits
- Specialized Products

The Cache Memory Management Data Book contains design and specification data for 35 devices. Sixteen application reports dealing with the above product lines are also included.

The General Information section includes an alphanumeric index, ordering information, glossary of symbols, terms, and definitions, timing interval conventions, an explanation of the function tables, timing diagram conventions, and basic data sheet structure.

A section on the development of logic symbols to meet both ANSI/IEEE Std 91-1984 and IEC Publication 617-12 are included for the reader's better understanding.

Package dimensions are given in the Mechanical Data section of the book in metric measurement and parenthetically in inches.

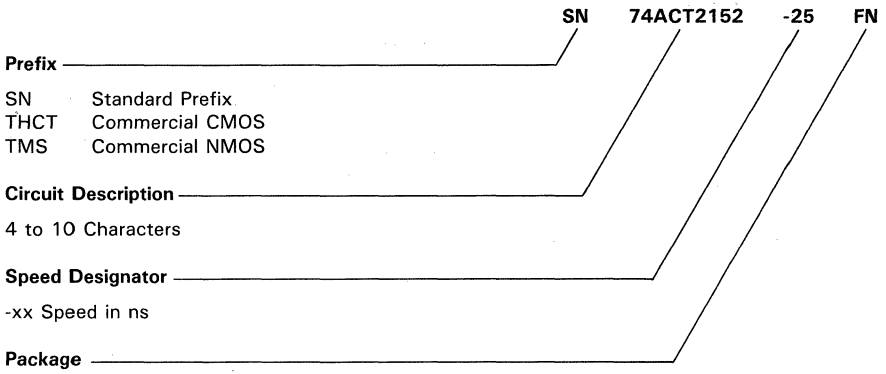
ESD Guidelines utilized in TI's products are included for the reader's better understanding.

Complete technical data for any Texas Instruments semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at 1-800-232-3200.

Contents

ORDERING INSTRUCTIONS

Factory orders for Cache Memory Management products described in this book should include a four-part type number as explained in the following example:



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INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i **Input capacitance**
The internal capacitance at an input of the device.

C_o **Output capacitance**
The internal capacitance at an output of the device.

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into† the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into† the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into† the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into† an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into† an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into† an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into† an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

†Current out of a terminal is given as a negative value.

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**

The current flowing into† an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**

The current flowing into† an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}.)

t_f **Fall time**

The time interval between two reference points (90% and 10% unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

†Current out of a terminal is given as a negative value.

t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_r **Rise time**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_t **Transition time (general)**
The time interval between two reference points (10% and 90% unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassifed time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for READ and W for WRITE).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or ''don't care'' level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Example symbology:

Classified	Unclassifed	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supersede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between the specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(R)}$	t_{RLRH}	Read pulse duration

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_r		Transition time (general)

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address

This supersedes the older form t_{PVX}.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  or  , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Shift registers provide a good example of the features of a function table. The function table of a shift register embodies all of the symbols used in most function tables. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

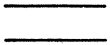
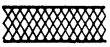
The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. The entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING: INPUT FORCING FUNCTIONS	MEANING: OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

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The front page of the data sheet begins with a list of key features such as organization, interface, compatibility, operation, and technology (N or P channel, silicon or metal-oxide gate). In addition, the top view of the device is shown with the pinout provided. Next, a general description of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's operation which includes the function of each pin (i.e., the relationship between each input/output and a given type of application).

Augmenting the descriptive text, there appears a logic symbol prepared in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12 and explained in Section 10 of this book. Following the symbol is usually a functional block diagram or a logic diagram. Usually, the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the operating free-air temperature range. If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Next, are the recommended operating conditions, (e.g., supply voltages, input voltages, and operating temperature). These devices are specified to work reliably and to meet all data sheet parameters when operated in accordance with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), it is no longer specified to meet the data sheet parameters. Operation beyond the absolute maximum ratings can result in catastrophic failures.

The next section provides a table of electrical characteristics over full ranges of recommended operating conditions (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of $T_A = 25°C$ with all power supply voltages at nominal value.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The switching characteristics over recommended supply voltage range are device performance characteristics inherent to device operation once the inputs are applied. These parameters are specified for the test conditions given. The timing requirements over recommended supply voltage range and operating free-air temperature indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams that follow. The interrelationship of the timing requirements to the switching characteristics is illustrated in the parameter measurement information section.

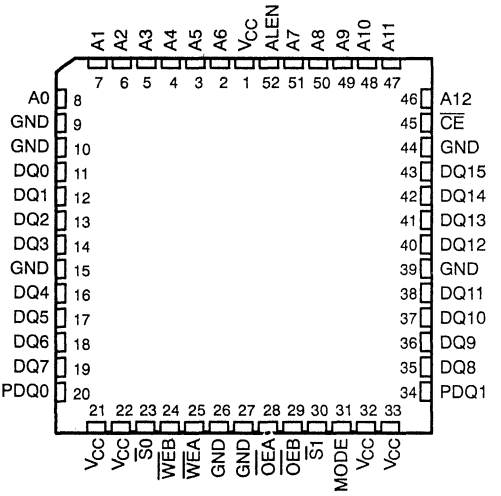
At the end of a data sheet, additional applications information may be provided, such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

Contents

D3291, NOVEMBER 1989–REVISED JUNE 1990

- **Interfaces Directly with the Intel 82385 Cache Controller**
- **Access Time . . . 25 ns Max**
- **Fast Access Time Supports 33-MHz Intel ESCA 80386 Operation**
- **Configurable for 2-Way or Direct Mapped Arrays**
- **Contains Address Latches and Byte Contol**
- **Cascadable for Larger Caches**
- **Byte Parity Storage Bits**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2140A is a 147,456-bit static RAM with address latches and byte control that can be configured as 2-way 4K x 18 or direct mapped 8K x 18. The 'ACT2140A is fabricated using advanced silicon-gate CMOS technology for simple, high-speed interface with bipolar TTL circuits. The 'ACT2140A was designed so that it will interface directly with the Intel 82385 cache controller. Significant reductions in memory component count, board area, and power dissipation can be achieved by using this device. When using the 2-way mode, two 'ACT2140As replace 16 4K x 4 static RAMs, two latches, eight bidirectional transceivers, and one AND gate.

The MODE input of the 'ACT2140A allows the device to be used as either a 2-way set associative or direct mapped data RAM. When MODE is tied high, the 'ACT2140A is configured as two banks of 4K x 18 with common outputs as shown in logic diagram. When MODE is tied low, the 'ACT2140A is configured as one bank of 8K x 18 as shown in logic diagram.

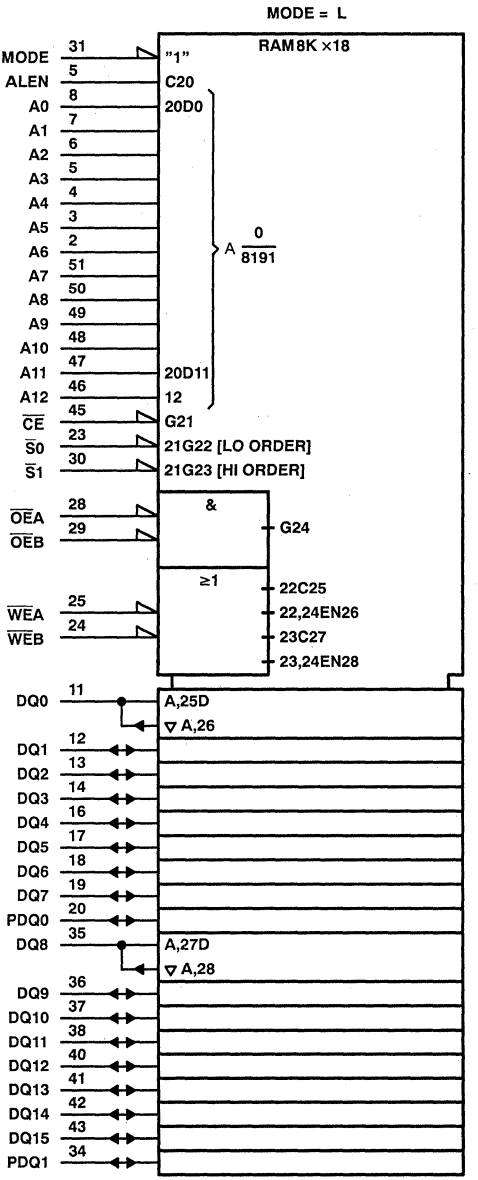
The SN74ACT2140A is characterized for operation from 0°C to 70°C.

ADVANCE INFORMATION

This device is covered by U.S. Patent 4,837,743.

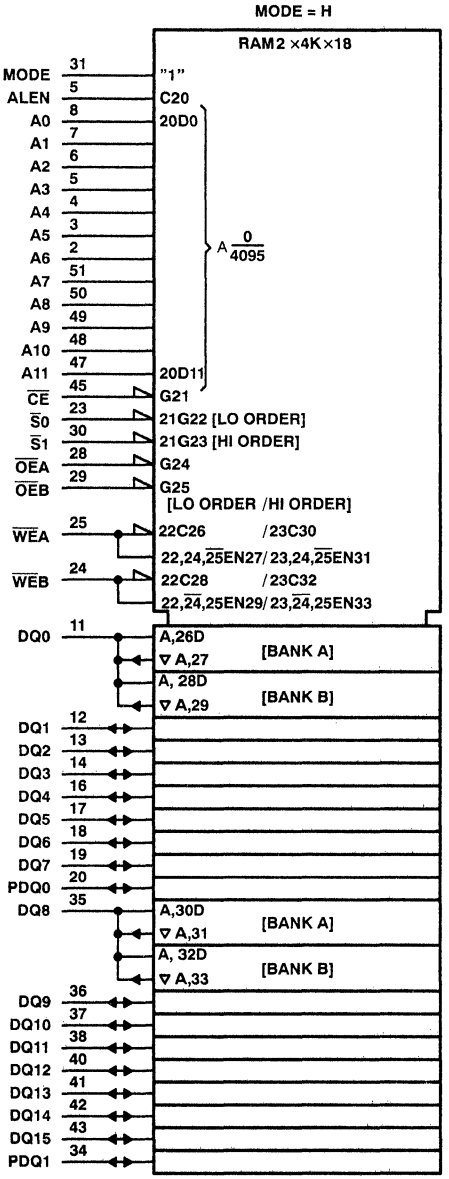
ADVANCE INFORMATION

logic symbol†



† This symbol is in accordance with ANSI/IEEE 91-1984.

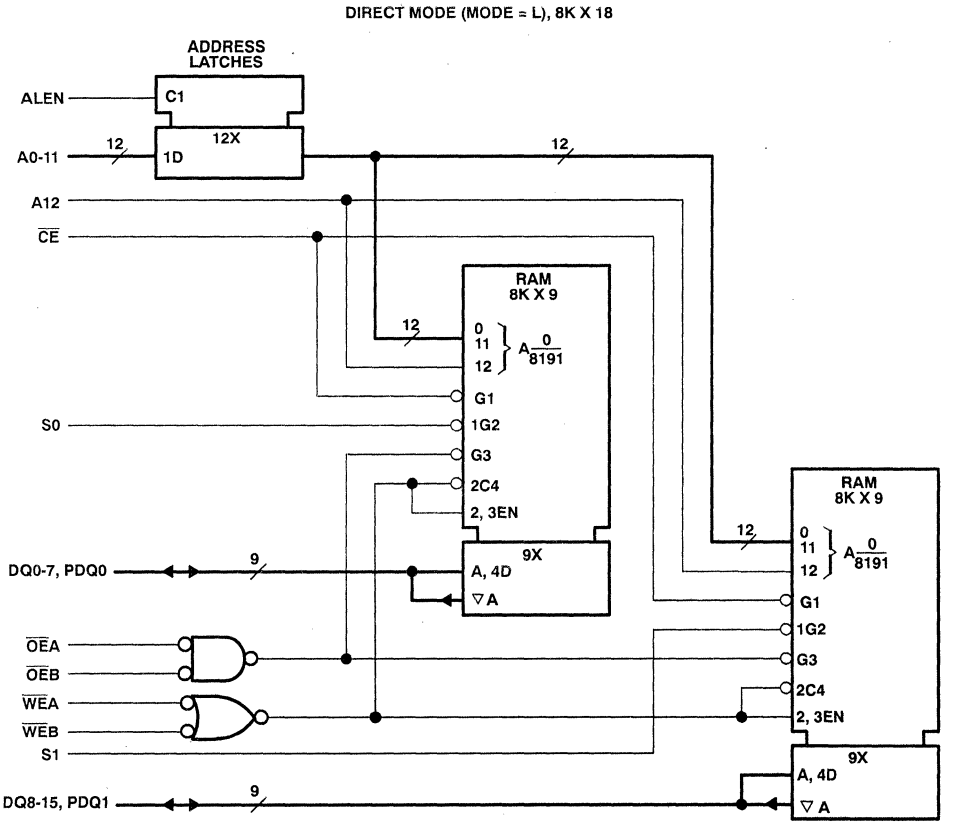
logic symbol†



† This symbol is in accordance with ANSI/IEEE 91-1984.

ADVANCE INFORMATION

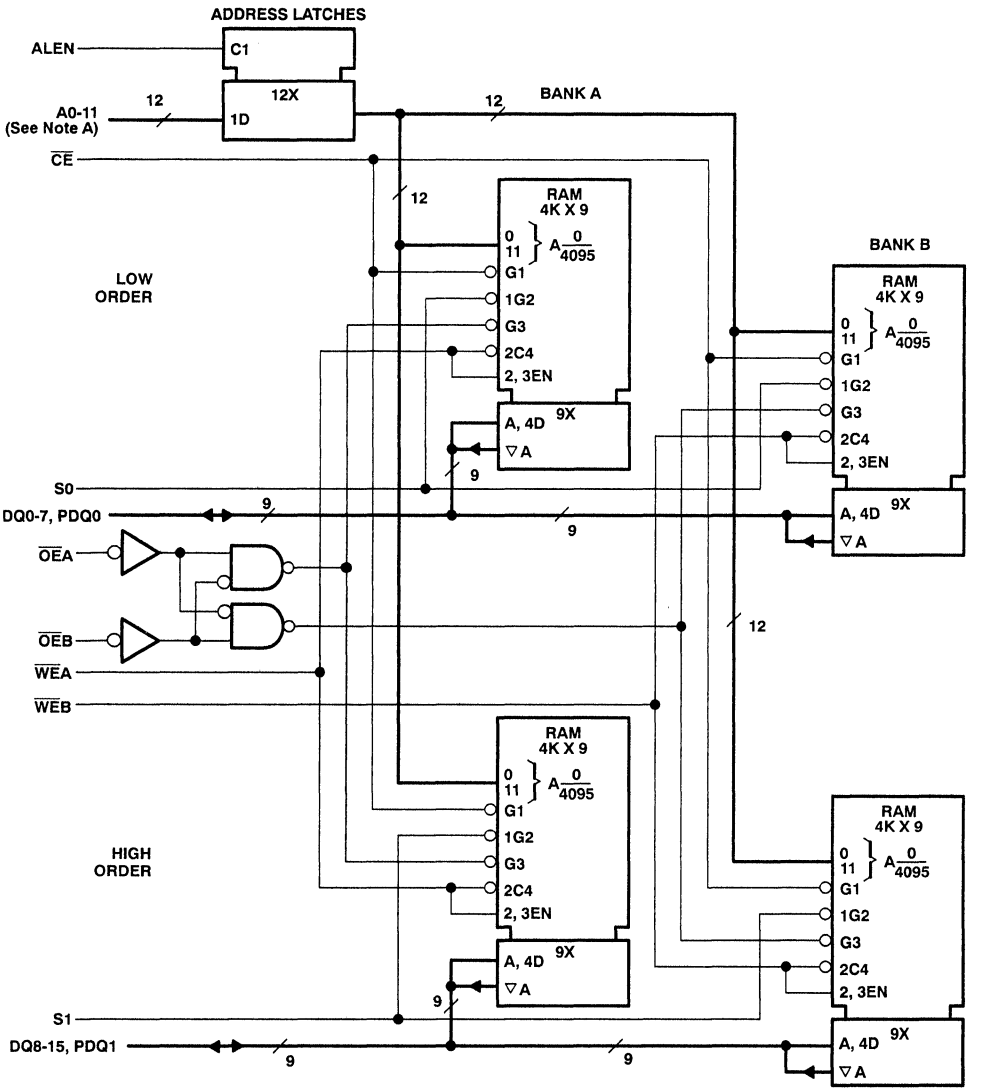
logic diagram (positive logic)



NOTE A: For a valid read operation in the direct mode, $\overline{OE}$A and $\overline{OE}$B must be low simultaneously.

logic diagram (positive logic)

TWO-WAY MODE (MODE = H) 2 X 4K X 18



NOTES: A. A12 should be grounded.
B. For a valid write operation in the two-way mode, $\overline{WEA}$ and $\overline{WEB}$ must not be low simultaneously.

ADVANCE INFORMATION

FUNCTION TABLES

TWO-WAY MODE (MODE = HIGH) 2 X 4K X 18 (see Note 1)

INPUTS							I/O		FUNCTION
$\overline{CE}$	$\overline{S0}$	$\overline{S1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	D0-D7, DP0	D8-D15, DP1	
X	H	H	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT
X	X	X	H	H	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
X	X	X	L	L	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
L	L	H	L	H	H	H	OUTPUT	HIGH-Z	READ BANK A
L	L	H	H	L	H	H	OUTPUT	HIGH-Z	READ BANK B
L	H	L	L	H	H	H	HIGH-Z	OUTPUT	READ BANK A
L	H	L	H	L	H	H	HIGH-Z	OUTPUT	READ BANK B
L	L	L	L	H	H	H	OUTPUT	OUTPUT	READ BANK A
L	L	L	H	L	H	H	OUTPUT	OUTPUT	READ BANK B
L	L	H	X	X	L	H	INPUT	HIGH-Z	WRITE BANK A
L	L	H	X	X	H	L	INPUT	HIGH-Z	WRITE BANK B
L	H	L	X	X	L	H	HIGH-Z	INPUT	WRITE BANK A
L	H	L	X	X	H	L	HIGH-Z	INPUT	WRITE BANK B
L	L	L	X	X	L	H	INPUT	INPUT	WRITE BANK A
L	L	L	X	X	H	L	INPUT	INPUT	WRITE BANK B
L	L	L	X	X	L	L	HIGH-Z	HIGH-Z	INVALID WRITE
H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT

DIRECT MODE (MODE = LOW) 8K x 18 (see Note 1)

INPUTS							I/O		FUNCTION
$\overline{CE}$	$\overline{S0}$	$\overline{S1}$	$\overline{OEA}^\dagger$	$\overline{OEB}^\dagger$	$\overline{WEA}^\dagger$	$\overline{WEB}^\dagger$	D0-D7, DP0	D8-D15, DP1	
X	H	H	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT
X	X	X	H	X	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
X	X	X	X	H	X	X	HIGH-Z	HIGH-Z	DISABLED OUTPUTS
L	L	H	L	L	H	H	OUTPUT	HIGH-Z	READ
L	H	L	L	L	H	H	HIGH-Z	OUTPUT	READ
L	L	L	L	L	H	H	OUTPUT	OUTPUT	READ
L	L	L	L	H	H	H	OUTPUT	OUTPUT	INVALID READ
L	L	L	H	L	H	H	OUTPUT	OUTPUT	INVALID READ
L	L	H	X	X	L	X	INPUT	HIGH-Z	WRITE
L	H	L	X	X	L	X	HIGH-Z	INPUT	WRITE
L	L	L	X	X	L	X	INPUT	INPUT	WRITE
L	L	H	X	X	X	L	INPUT	HIGH-Z	WRITE
L	H	L	X	X	X	L	HIGH-Z	INPUT	WRITE
L	L	L	X	X	X	L	INPUT	INPUT	WRITE
H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	DESELECT

† For compatibility with functionally equivalent devices, it may be necessary to wire $\overline{OEA}$ to $\overline{OEB}$ and $\overline{WEA}$ to $\overline{WEB}$ when MODE is tied low.

NOTE 1: Address latches for A0-A11 are latched when input signal ALEN is low and transparent when ALEN is high. A12 is functional only when MODE = low is always transparent. A12 should be grounded in the 2-way mode.

Terminal Functions

PIN NAME	DESCRIPTION
A0-A11	Address inputs. Address the random access memory locations. A0-A11 are latched on the falling edge of the ALEN input.
A12	A12 address input. In the direct mode, MODE = low, A12 is a nonlatchable (always transparent) address bit. A12 is used when implementing 64K-byte caches for the 82385. In the two-way mode, MODE = high, A12 is not functional and should be tied to GND.
ALEN	Address Latch Enable input. ALEN controls the internal address latch that resides between the address inputs, A0-A11, and the memory array. When ALEN is high, the latch is transparent. A falling edge at ALEN latches the levels at the address inputs.
$\overline{CE}$	Chip Enable input. $\overline{CE}$ enables the chip for read and write operations when asserted low. $\overline{CE}$ disables the chip for read and write operations when high. As shown in write cycle 2, $\overline{CE}$-controlled writes can be performed.
DQ0-DQ15	Data input/output. DQ0-DQ15 are three-state terminals that provide access to the memory array contents.
MODE	Mode input. When MODE is high, this device is configured as a two-way data RAM with two 4K X 18 memory banks. When MODE is low, this device is configured as a direct 8K x 18 data RAM.
$\overline{OEA}$, $\overline{OEB}$	Output Enable inputs. In the two-way mode, MODE = high, RAM bank A is enabled when $\overline{OEA}$ is low and RAM bank B is enabled when $\overline{OEB}$ is low. When $\overline{OEA}$ and $\overline{OEB}$ go low or high simultaneously, both banks are deselected. In the direct mode, MODE = low, $\overline{OEA}$ and $\overline{OEB}$ can be externally wired together. A low on $\overline{OEA}$ and $\overline{OEB}$ will then enable the output of the 8K X 18 RAM.
PDQ0, PDQ1	Parity input/output. PDQ0 and PDQ1 are three-state terminals that provide access into the memory array for the storage and retrieval of externally generated and checked parity bits. If these pins are not used, they should be left open.
$\overline{S0}$, $\overline{S1}$	Select Inputs. $\overline{S0}$ and $\overline{S1}$ individually enable the two bytes of memory. $\overline{S}$ low enables bits DQ0-DQ7 (and PDQ0) and $\overline{S1}$ enables bits DQ8-DQ15 (and PDQ1). As shown in write cycle 3, $\overline{S}$-controlled writes can be performed.
$\overline{WEA}$, $\overline{WEB}$	Write Enable inputs. In the two-way mode, $\overline{WEA}$ low writes data into memory bank A and $\overline{WEB}$ writes data into memory bank B. In the direct mode, $\overline{WEA}$ and $\overline{WEB}$ can be wired together. A low on $\overline{WEA}$ and $\overline{WEB}$ will then write data into the 8K X 18 memory.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) ..... −0.5 to 7 V
Input voltage range, any inputs ..... −0.5 to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±25mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±25mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25mA
Continuous current through V_{CC} or GND pins ..... ±200mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... − 30°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values are with respect to GND.

ADVANCE INFORMATION

recommended operating conditions (see important notice)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (see Note 3)	−0.5		0.8	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data, the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times in the threshold region at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to latch the address inputs using ALEN or disable the device using $\overline{CE}$ or S0 and S1, during the time that slow rise or fall times exist at the address inputs. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs with the device enabled and the address latch transparent should be avoided in order to ensure that a slow rise/fall condition does not occur. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V,	I_{OH} = −1 mA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	I_{OL} = 4 mA				0.4	V
I_I	Input current	V_{CC} = 5.25 V,	V_I = 0 to V_{CC}				±10	μA
I_{OZ}	Off-state output current	V_{CC} = 5.25 V,	V_O = 0 to V_{CC}				±10	μA
I_{CC1}	Supply current (operative)‡	V_{CC} = 5.25 V, $\overline{OEA}$ = $\overline{OEB}$ = high,	$\overline{S0}$, $\overline{S1}$, and $\overline{CE}$ = low, MODE = high or low	$t_{c(rd)}$ = 60 ns,		120	180	mA
I_{CC2}	Supply current (deselect)	V_{CC} = 5.25 V,	$\overline{CE}$ = high,	MODE = high or low		40	90	mA
I_{CC3}	Supply current (standby)§	V_{CC} = 5.25 V,	All inputs = 0 V or 3 V			26	50	mA
C_i	Input capacitance	V_I = 0					5	pF
C_o	Output capacitance	V_O = 0					8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ θ_{JA} = 50°C/W, $T_J = T_A + \theta_{JA} \cdot P$
§ The 'ACT2140A is in standby when ALEN is low and $\overline{WEA}$ and $\overline{WEB}$ are high; or when A0-A11 are stable and $\overline{WEA}$ and $\overline{WEB}$ are high. To assure low standby current, V_{IH} levels must be 3 V minimum.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

read cycle

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{c(rd)}$	Read cycle time‡	t_{RC}	60		ns
$t_{a(A)}$	Access time, ALEN high or address to output	t_{AA}		25	ns
$t_{a(A12)}$	Access time, A12 to output (see Note 4)	t_{A12A}		17	ns
$t_{a(S)}$	Access time, $\overline{S0}$, $\overline{S1}$ to output	t_{CS}		25	ns
$t_{a(CE)}$	Access time, $\overline{CE}$ to output	t_{CE}		20	ns
$t_{a(OE)}$	Access time, $\overline{OEA}$ or $\overline{OEB}$ to output	t_{OE}		10	ns
t_v	Valid time, output after address change or ALEN high	t_{OH}	3		ns
$t_{en(S)}$	Enable time, $\overline{S0}$, $\overline{S1}$ to output	t_{LZ}	3		ns
$t_{en(CE)}$	Enable time, $\overline{CE}$ to output	t_{LZ}	3		ns
$t_{en(OE)}$	Enable time, $\overline{OEA}$ or $\overline{OEB}$ to output	t_{OLZ}	0		ns
$t_{dis(S)}$	Disable time, $\overline{S0}$, $\overline{S1}$ to output	t_{HZ}		15	ns
$t_{dis(CE)}$	Disable time, $\overline{CE}$ to output	t_{HZ}		15	ns
$t_{dis(OE)}$	Disable time, $\overline{OEA}$ or $\overline{OEB}$ to output	t_{OHZ}		10	ns

NOTE 4: The parameter $t_{a(A12)}$ is measured in the direct mode (MODE = low) with ALEN low.
‡ 60 ns equates to the Intel 82386/82385 running at 33 MHz.

write cycle

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{en(WE)}$	Enable time, $\overline{WEA}$ or $\overline{WEB}$ to output	t_{WLZ}	3		ns
$t_{dis(WE)}$	Disable time, $\overline{WEA}$ or $\overline{WEB}$ to output	t_{WHZ}		15	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

read cycle

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{w1}	Pulse duration, ALEN high	t_{ALEN}	8		ns
t_{su1}	Setup time, address before ALEN low	t_{ASL}	4		ns
t_{h1}	Hold time, address after ALEN low	t_{AHL}	5		ns

† See Parameter Measurement Information for load circuits and voltage waveforms.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)†

write cycle

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{c(WR)}$	Write cycle time‡	t_{WC}	60		ns
$t_{v(AW)}$	Address valid before end of write	t_{AW}	20		ns
t_{w1}	Pulse duration, ALEN high	t_{ALEN}	8		ns
t_{w2}	Pulse duration, write enable low	t_{WP}	20		ns
t_{w3}	Pulse duration, $\overline{CE}$ low, $\overline{CE}$ controlled write	t_{CP}	20		ns
t_{w4}	Pulse duration, $\overline{CE}$ high, $\overline{CE}$ controlled write		10		ns
t_{su1}	Setup time, address before ALEN low	t_{ASL}	4		ns
t_{su2}	Setup time, address before write start	t_{AS}	0		ns
t_{su3}	Setup time, data before end of write	t_{DW}	10		ns
t_{su4}	Setup time, $\overline{S0}$, $\overline{S1}$, $\overline{CE}$, or $\overline{WE}$ low before end of write	t_{CW}	20		ns
t_{h1}	Hold time, address after ALEN low	t_{AHL}	5		ns
t_{h2}	Hold time, ALEN low or address after end of write	t_{WR}	2		ns
t_{h3}	Hold time, data after end of write	t_{DH}	0		ns

† See Parameter Measurement Information for load circuits and voltage waveforms.
‡ 60 ns equates to the Intel 82386/82385 running at 33 MHz.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

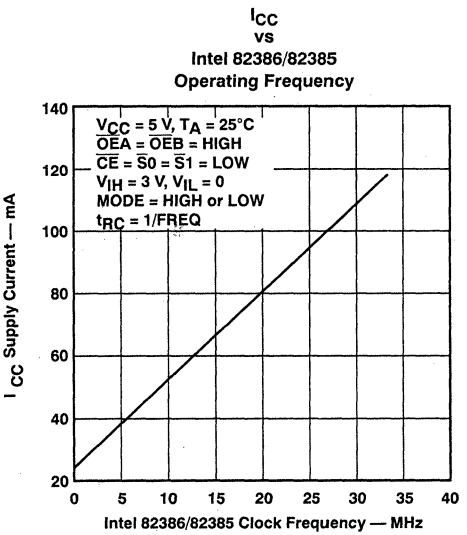
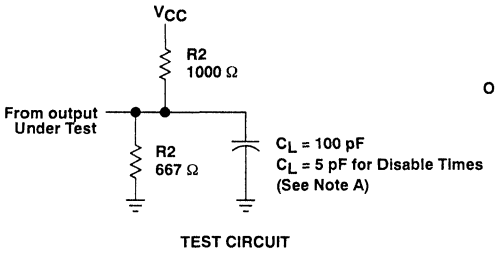
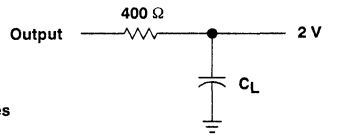


Figure 1

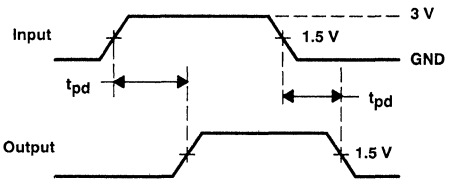
PARAMETER MEASUREMENT INFORMATION



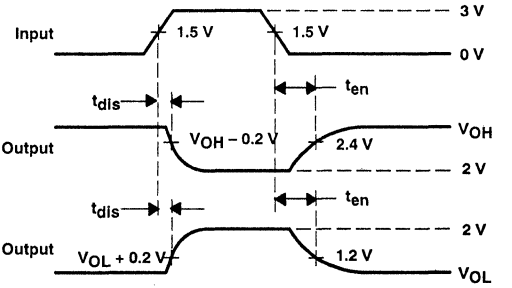
TEST CIRCUIT



THEVENIN EQUIVALENT
TEST CIRCUIT



PROPAGATION-TIME VOLTAGE WAVEFORMS



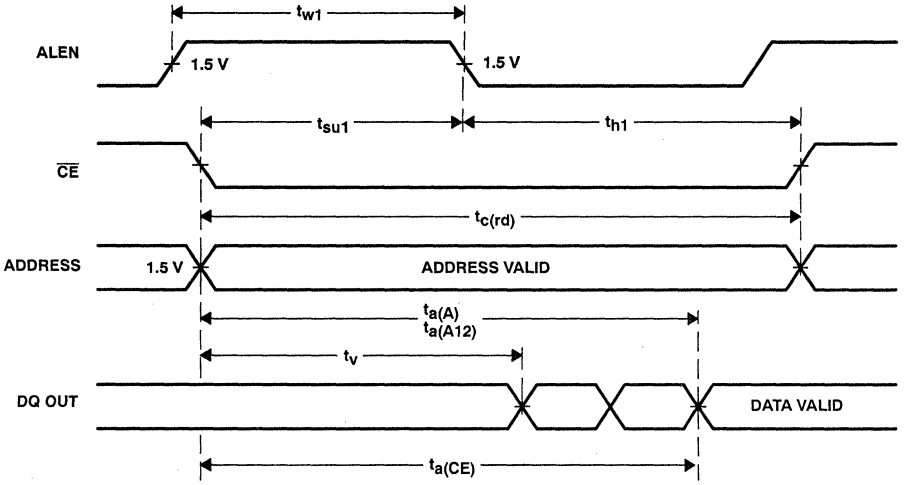
ENABLE/DISABLE VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and test fixture capacitance.

Figure 2. Test Circuit and Voltage Waveforms

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

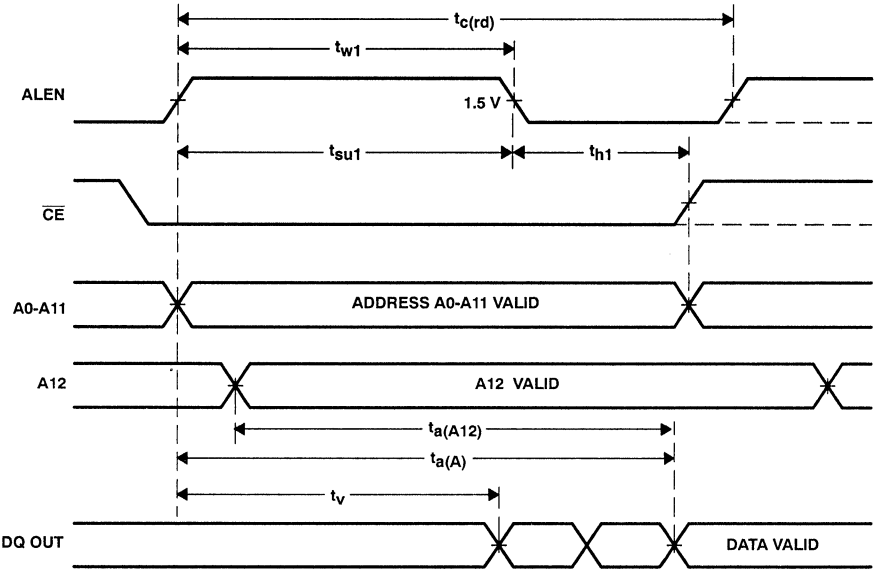


NOTE: $\overline{WE}$ high, $\overline{CS}$ low, and $\overline{OE}$ low.

Figure 3. Read Cycle 1 Waveforms

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

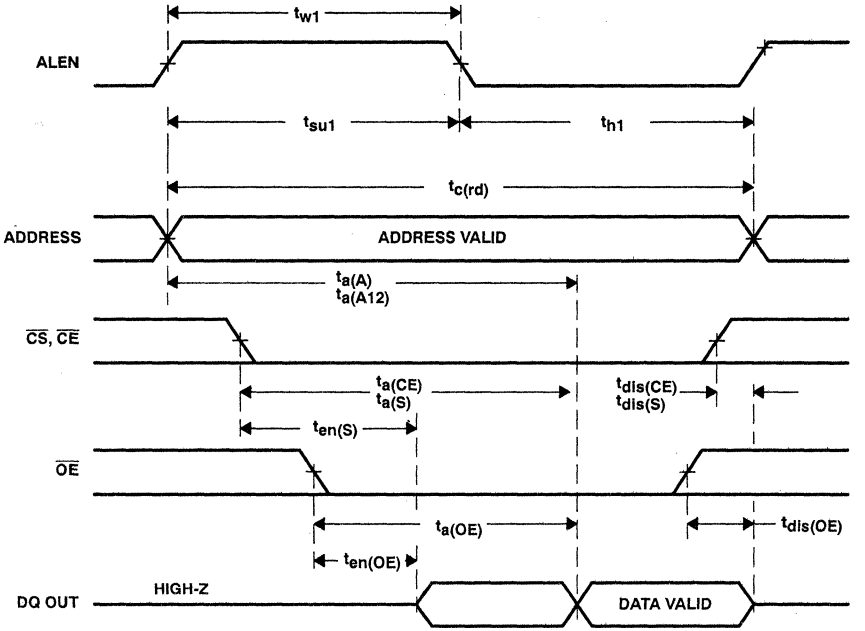


NOTE: $\overline{WE}$ high, $\overline{CS}$ low, and $\overline{OE}$ low.

Figure 4. Read Cycle 2 Waveforms

ADVANCE INFORMATION

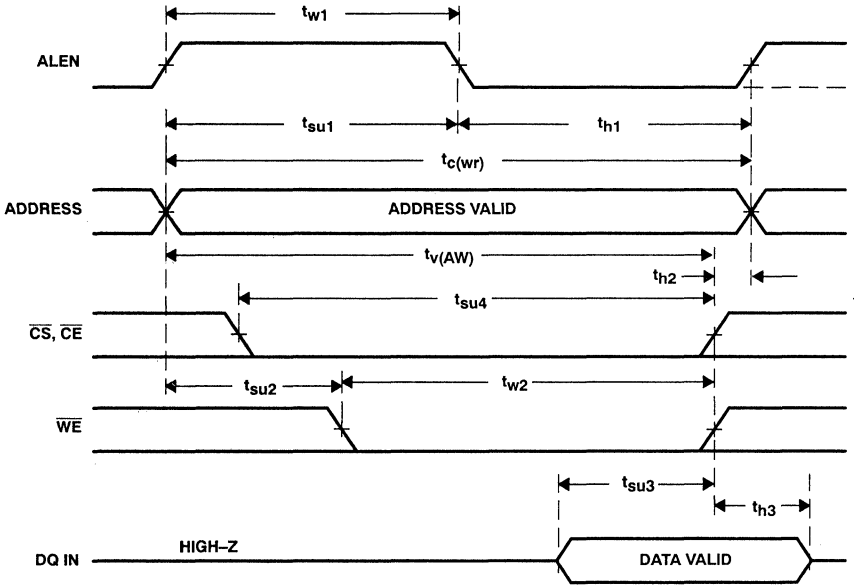
PARAMETER MEASUREMENT INFORMATION



NOTE: $\overline{WE}$ high.

Figure 5. Read Cycle 3 Waveforms

PARAMETER MEASUREMENT INFORMATION

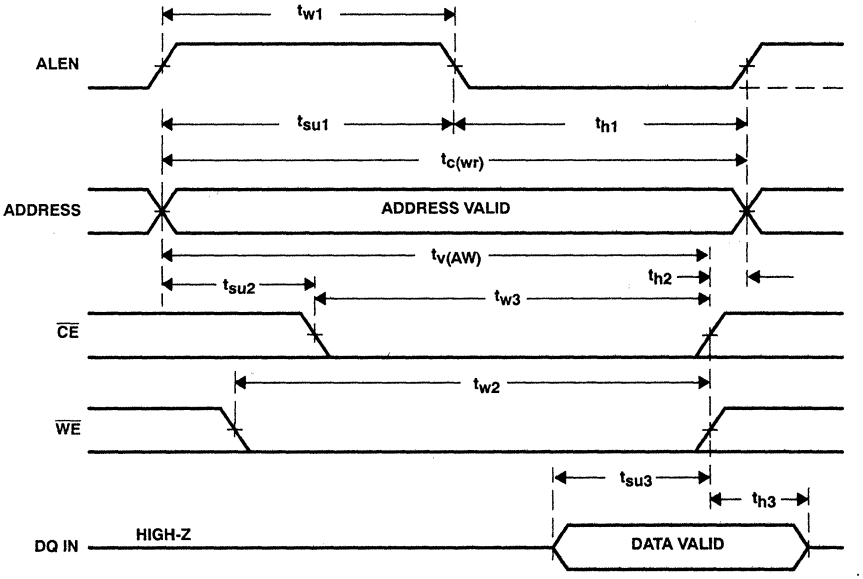


NOTE: $\overline{WE}$ controlled.

Figure 6. Write Cycle 1 Waveforms

ADVANCE INFORMATION

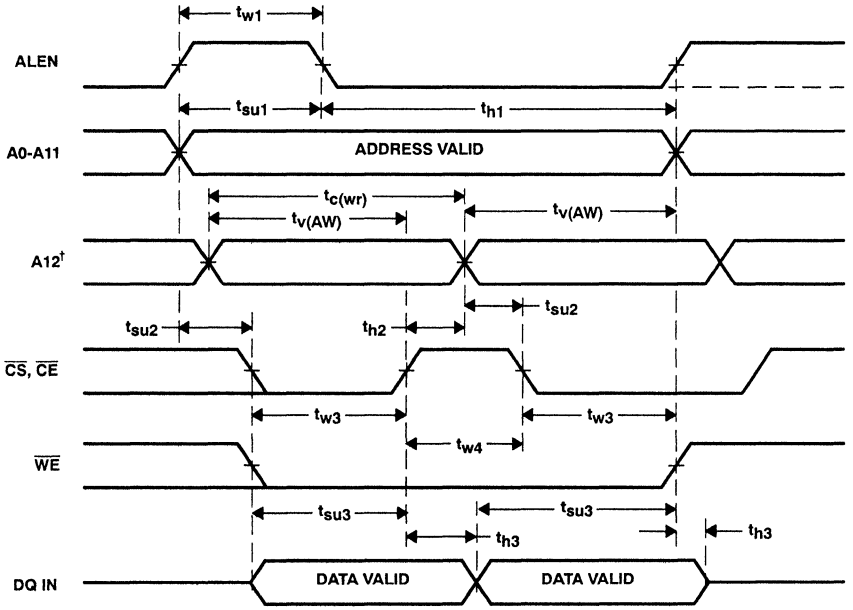
PARAMETER MEASUREMENT INFORMATION



NOTE: $\overline{CE}$ controlled and $\overline{OE}$ high.

Figure 7. Write Cycle 2 Waveforms

PARAMETER MEASUREMENT INFORMATION



† A12 is an active input only when MODE low.
NOTE: $\overline{CS}$ or $\overline{CE}$ controlled and $\overline{OE}$ high.

Figure 8. Write Cycle 3 Waveforms

ADVANCE INFORMATION

APPLICATION INFORMATION

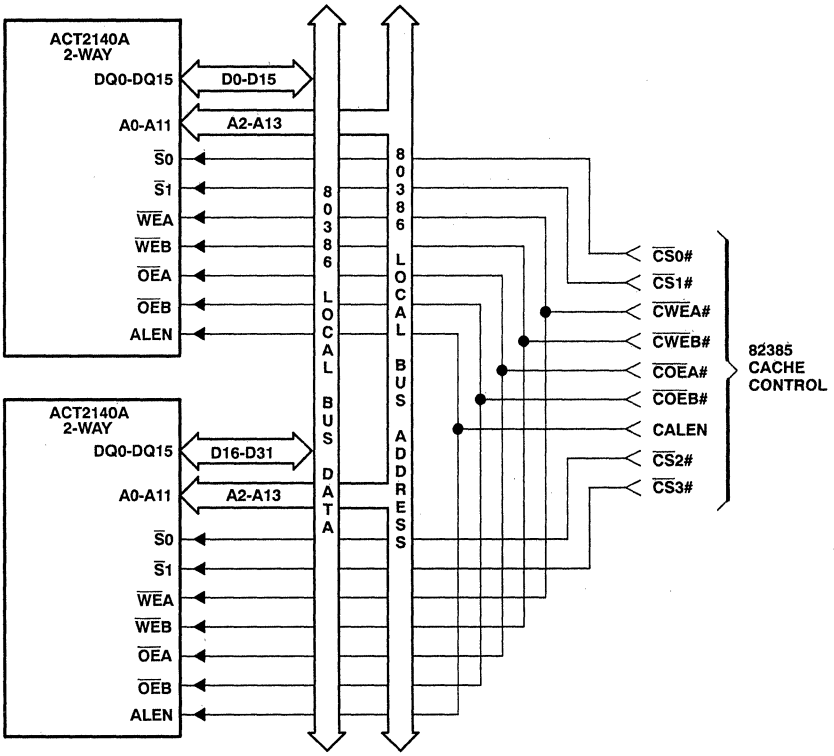


Figure 9. 32K-Byte 2-Way Cache

APPLICATION INFORMATION

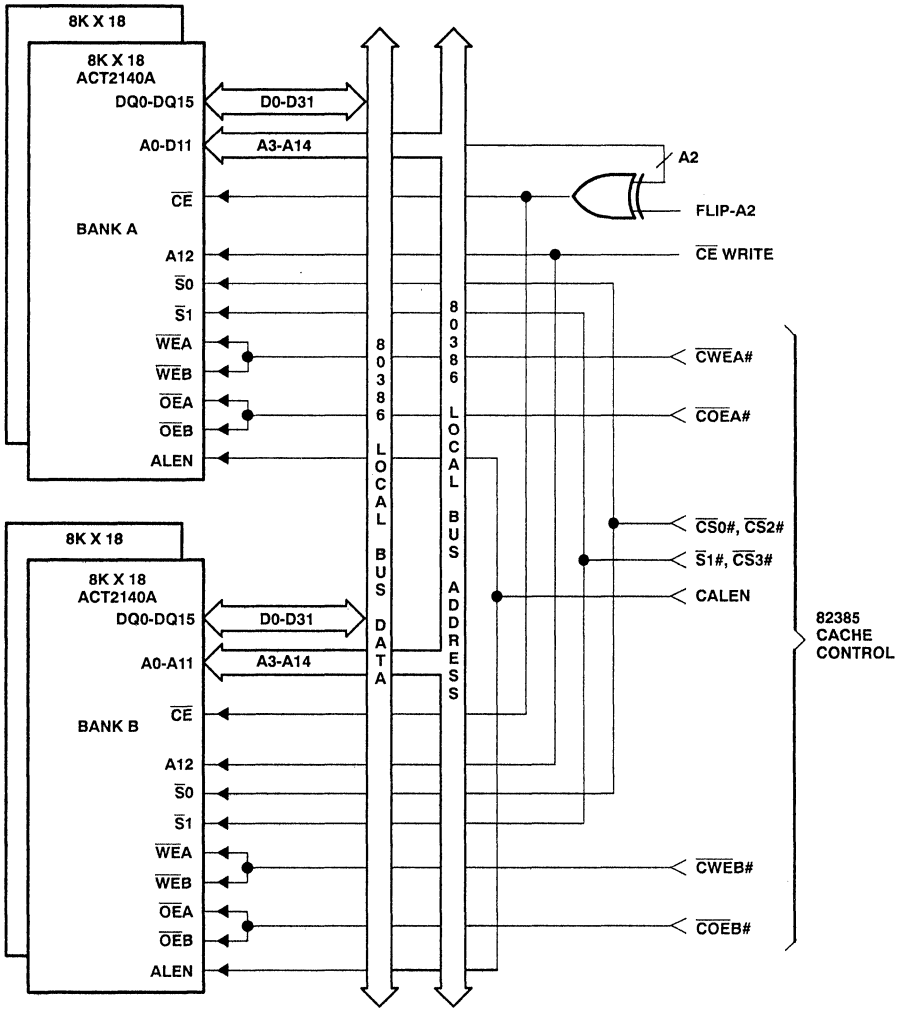


Figure 10. 64K-Byte 2-Way Cache Memory for the Intel 82385

ADVANCE INFORMATION

APPLICATION INFORMATION

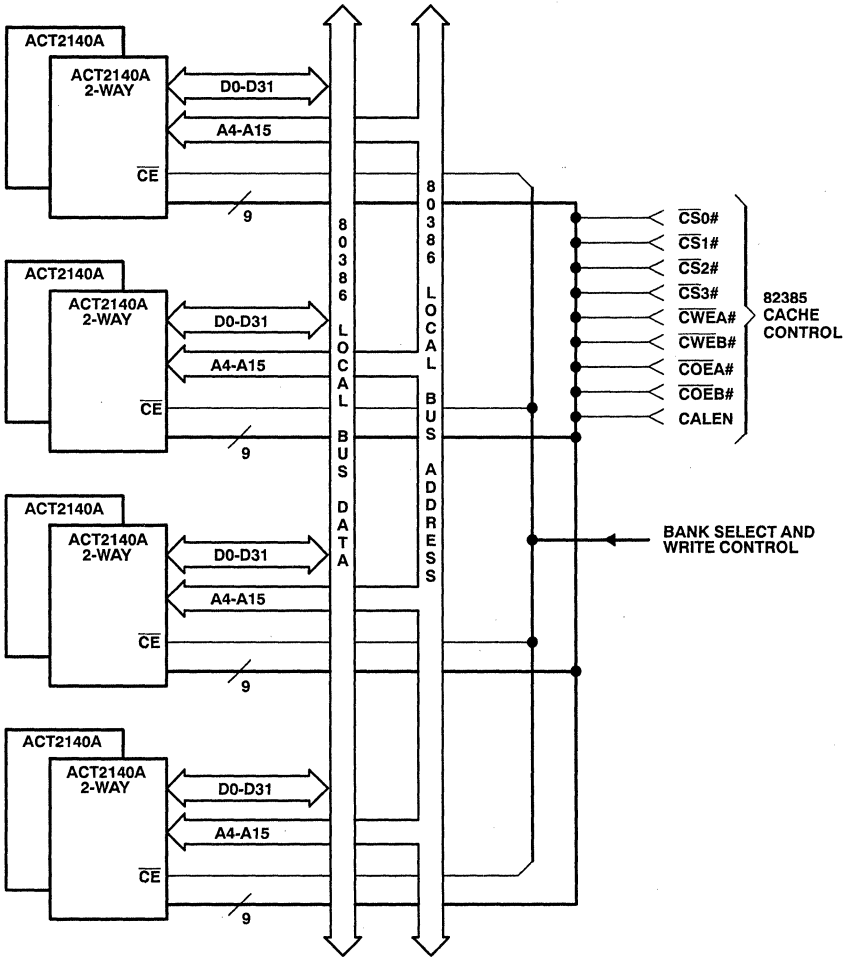
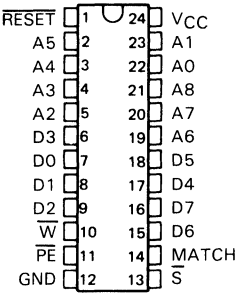


Figure 11. Intel 82385 and SN74ACT2140A 128K-Byte 2-Way Cache

D2911, MARCH 1982—REVISED SEPTEMBER 1985

- **'ACT2150A is Recommended for New Designs**
- **Fast Address to Match Valid Delay — Three Speed Ranges: 35 ns, 45 ns, 55 ns**
- **512 × 9 Internal RAM**
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **Max Power Dissipation: 660 mW**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable SMOS (Scaled NMOS) Technology**
- **TTL- and CMOS Compatible Inputs and Outputs**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be acheived with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 × 9 RAM locations are cleared and the MATCH output is forced high.

The cache address comparator operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

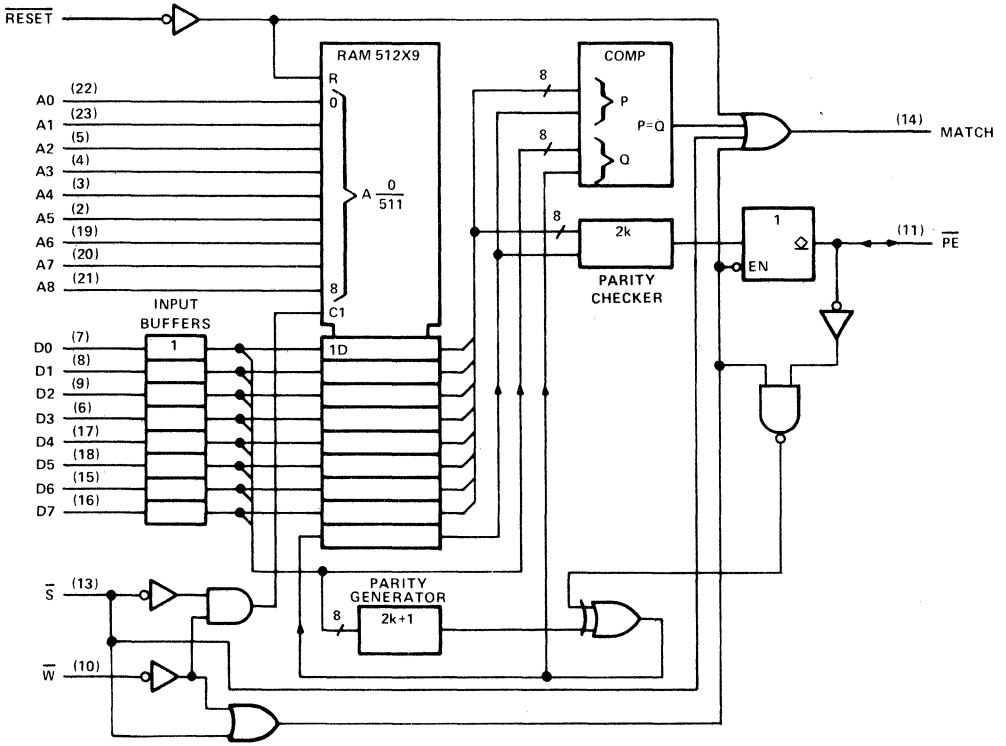
MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where S = V_{IL}, W = V_{IH}, RESET = V_{IH}

functional block diagram (positive logic)



This diagram has been changed to correct errors in previous versions. No functional change has been made in the chip.

TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity Error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range, any input . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated condtions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		6	V
V_{IL}	Low-level input voltage (See Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS2150-3		TMS2150-4 TMS2150-5		UNIT
			MIN	MAX	MIN	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4		2.4		V
		V_{CC} = 4.5 V, I_{OH} = −20 μA	3.5		3.5		
$V_{OL(M)}$	MATCH low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 4 mA		0.4		0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.4		0.4	V
I_I	Input current	V_I = 0 V to 5.5 V		10		10	μA
$I_{OL(PE)}$	$\overline{PE}$ output sink current	V_{CC} = 4.5 V, V_{OL} = 0.4 V	12		12		mA
I_{OS}‡	Short-circuit MATCH output current	V_{CC} = 5.5 V, V_O = GND		−150		−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		145		135	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_{IL}		155		145	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		5		5	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		6		6	pF

‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature†

PARAMETER		TMS2150-3		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address to MATCH		35		45		55	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$		45		55		65	ns
$t_{a(S)}$	Access time from $\overline{S}$ to MATCH		20		25		35	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		20		35		45	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		30		30		40	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		20		25		35	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		20		25		35	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		20		25		35	ns
$t_{v(A)}$	MATCH valid time after change of address	5		5		5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	15		15		15		ns

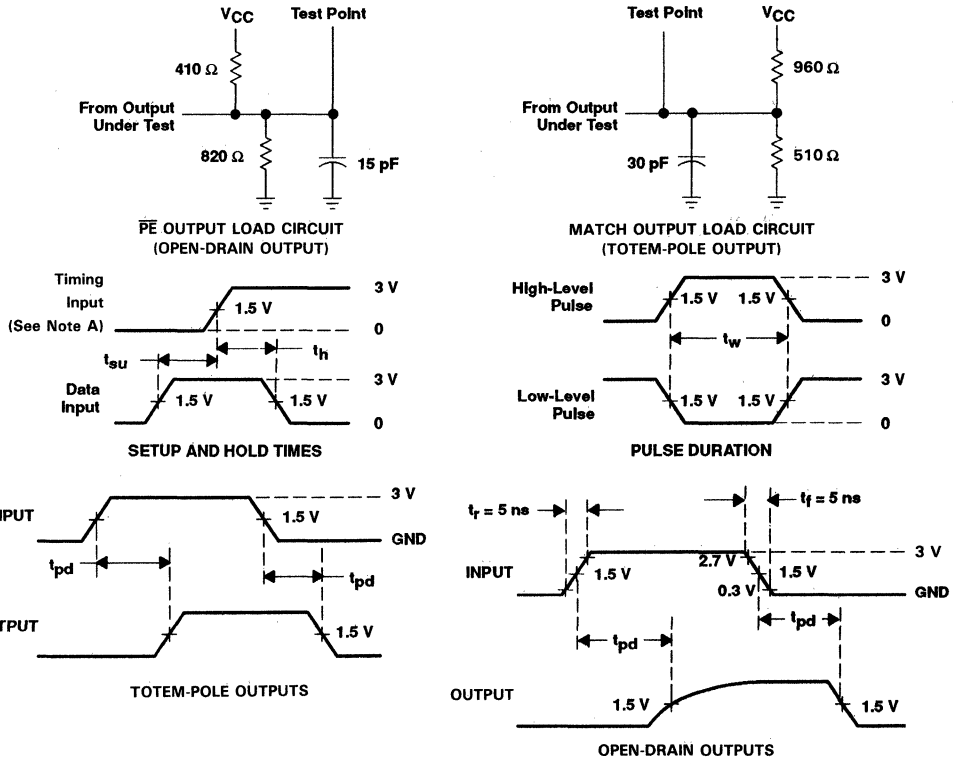
†See Parameter Measurement Information for load circuits and voltage waveforms.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS2150-3		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time, without writing $\overline{PE}$	30		40		50		ns
$t_{cPE(W)}$	Write cycle time, writing $\overline{PE}$ (see Note 3)	35		40		50		ns
$t_{c(rd)}$	Read cycle time	35		45		55		ns
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		35		45		ns
$t_{(WL)}$	Pulse duration $\overline{W}$ low, without writing $\overline{PE}$	20		25		30		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	35		40		45		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		30		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		30		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		30		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		5		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	5		5		10		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		5		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		0		ns
t_{AVWH}	Address valid to write enable high	30		40		50		ns

NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

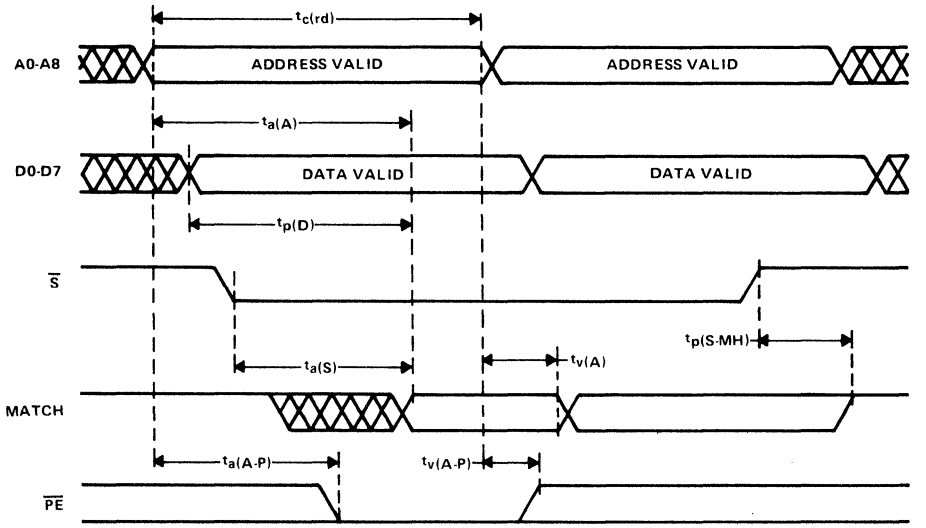
PARAMETER MEASUREMENT INFORMATION



NOTE A: Input rise and fall times are 5 ns.

FIGURE 1. TIMING REFERENCE LEVELS

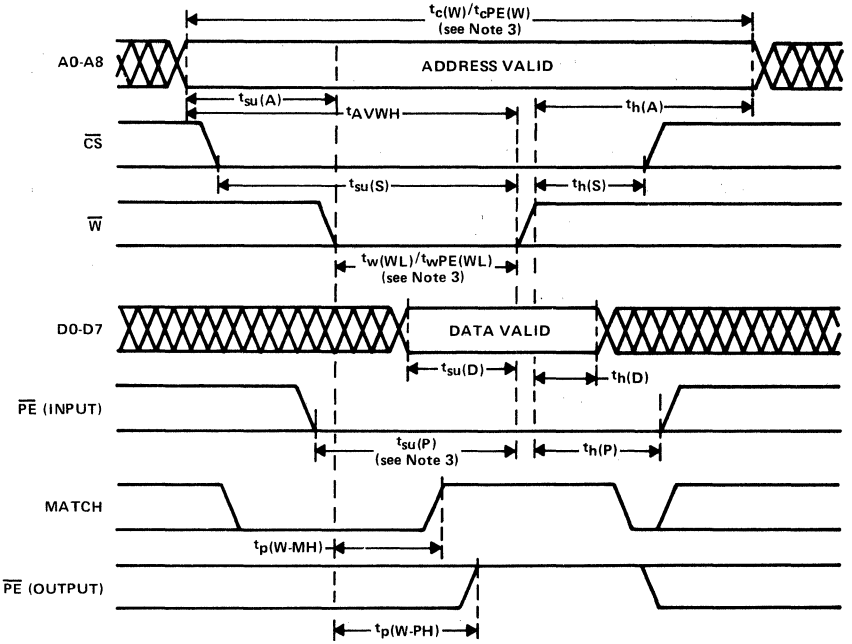
PARAMETER MEASUREMENT INFORMATION



NOTE: Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2 V. The timing reference level for output pulses is 1.5 V.

FIGURE 2. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 3. WRITE CYCLE TIMING

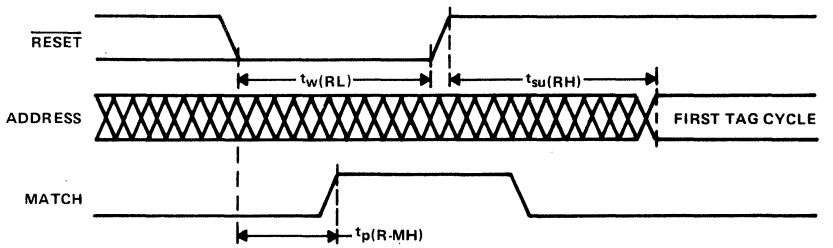
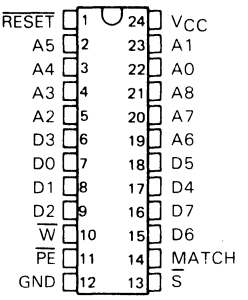


FIGURE 4. RESET CYCLE TIMING

D3183, NOVEMBER 1988—REVISED MARCH 1990

- **Address to MATCH Valid Time**
  'ACT2150A-20 . . . 20 ns max
  'ACT2150A-30 . . . 30 ns max
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using Advanced CMOS technology for high-speed, low-power interface with bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be acheived with this device.

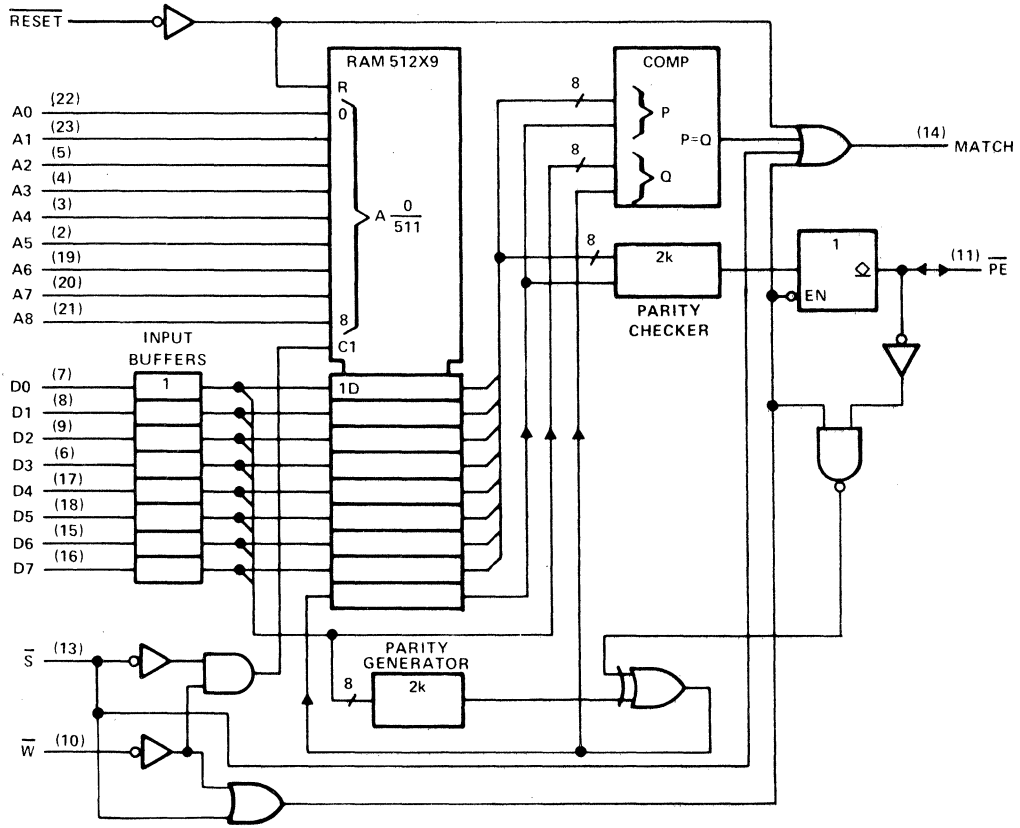
When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The SN74ACT2150A operates from a single 5 V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic ''Small Outline'' packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

logic diagram (positive logic)



MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH}, $\overline{RESET}$ = V_{IH}

TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage range, any input . . . . . −1.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated condtions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage	$\overline{PE}$			5.5	V
I_{OH}	High-level output current	MATCH			−8	mA
I_{OL}	Low-level output current	MATCH			8	mA
		$\overline{PE}$			16	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using the pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2 V). In systems with −1.5 V or more undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'ACT2150A-20			'ACT2150A-30			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	I_{OH} = −8 mA, V_{CC} = 4.5 V	2.4			2.4			V
		I_{OH} = −20 μA, V_{CC} = 4.5 V	3.5			3.5			
$V_{OL(M)}$	MATCH low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	I_{OL} = 16 mA, V_{CC} = 4.5 V,			0.4			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10			10	μA
I_{OS}	Short-circuit MATCH output current	V_O = GND, V_{CC} = 5.5 V			−150			−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		53	95		53	95	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_L		2.75	6		2.75	6	mA
C_i	Input capacitance	f = 1 MHz			5			5	pF
C_o	Output capacitance	f = 1 MHz			6			6	pF

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature†

PARAMETER		'ACT2150A-20		'ACT2150A-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		20		30	ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		22		30	ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		30		35	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		10		15	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		15		20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		10		15	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		10		12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		10		12	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		15		20	ns
$t_{v(A-M)}$	MATCH valid time after change of address	3		3		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

PARAMETER		'ACT2150A-20		'ACT2150A-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		40		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	20		25		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	20		25		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	0		0		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		ns
t_{AVWH}	Address valid to write enable high	20		25		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

PARAMETER MEASUREMENT INFORMATION

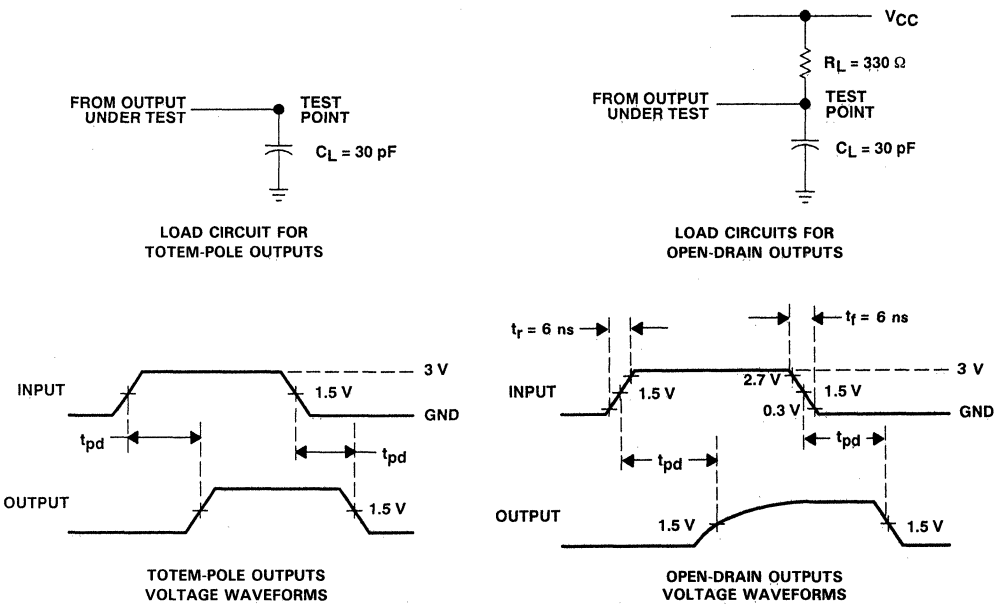


FIGURE 1. LOAD CIRCUITS AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

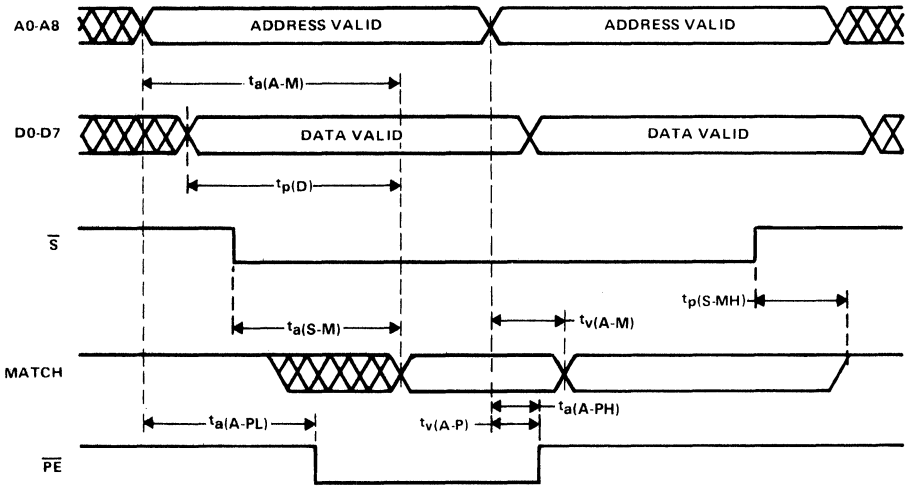
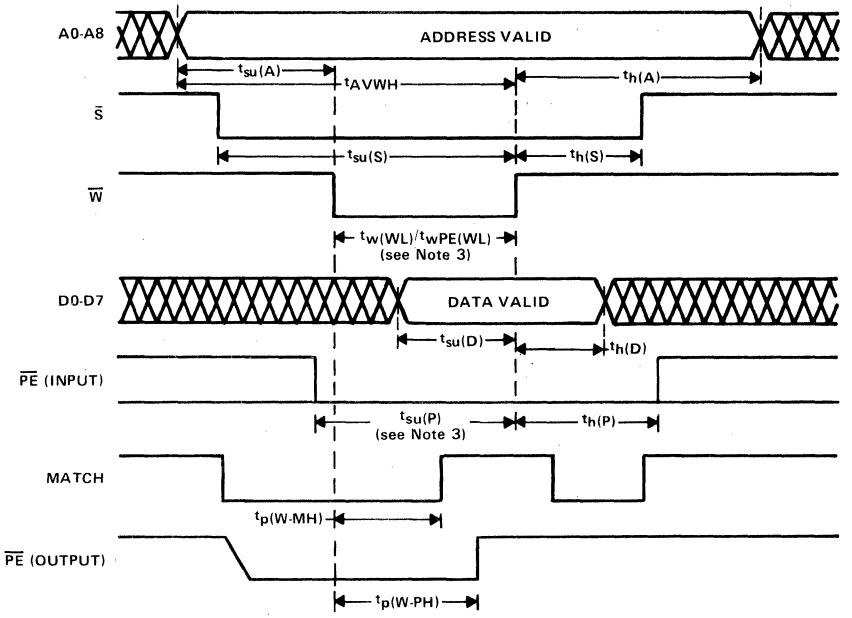


FIGURE 2. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 3. WRITE CYCLE TIMING

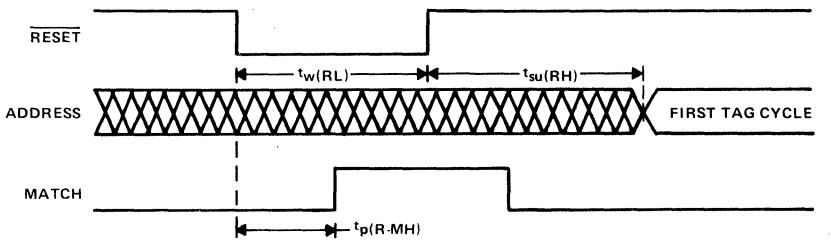


FIGURE 4. RESET CYCLE TIMING

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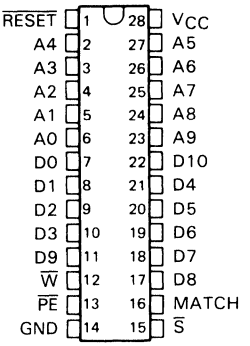
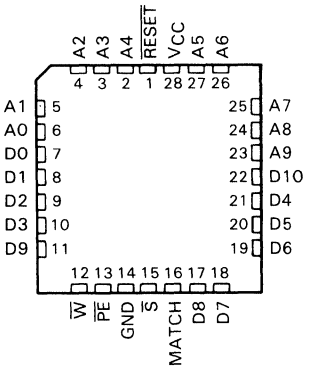
D3105, SEPTEMBER 1987–REVISED MARCH 1990

- **Fast Address to Match Delay . . . 22 ns Max**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generator and Checking**
- **Parity Error Output, Force Parity Error Input**
- **Easily Expandable**
- **Choice of Totem-Pole ('ACT2151) or Open-Drain ('ACT2153) MATCH Output**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process**
- **Fully TTL-Compatible**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2151 and 'ACT2153 cache address comparators consist of a high-speed 1K × 11 static RAM array, parity generator, parity checker, and 12-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2151 has a totem-pole match output while the 'ACT2153 has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A9 with the data D0-D10 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D10 plus generated odd parity are written in the 12-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 1K × 11 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

EPIC is a trademark of Texas Instruments Incorporated.
These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

These cache address comparators operate from a single 5-V supply and are offered in 28-pin 600-mil plastic dual-in-line or PLCC packages.

The SN74ACT2151 and SN74ACT2153 are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: (A0-A9) = D0-D10 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

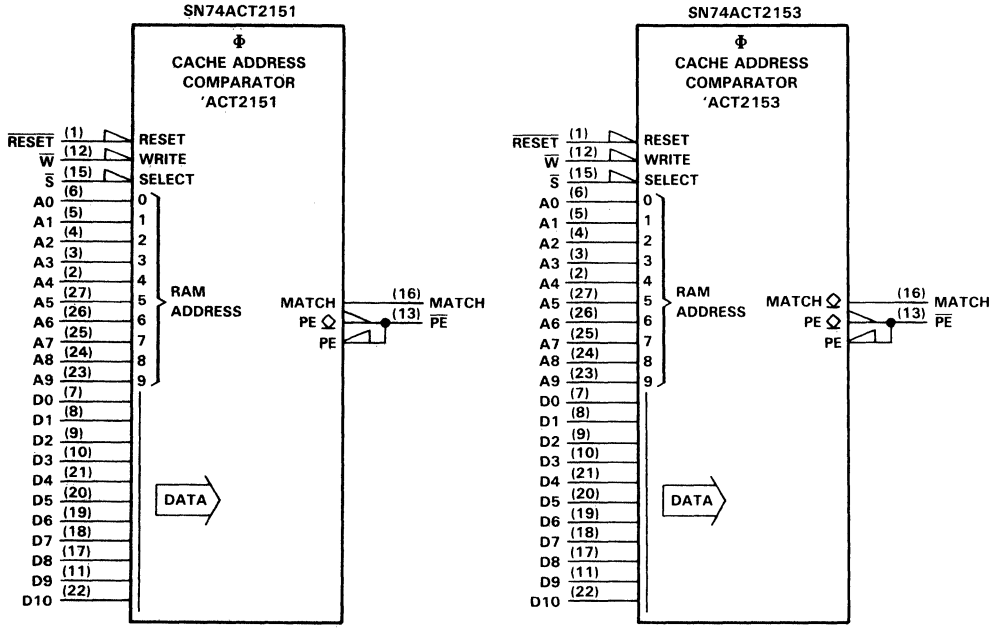
MATCH = V_{OL} if: (A0-A9) ≠ D0-D10 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{W}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	
H	L	H	L	L	Parity error
			L	H	Not equal
			H	L	Undefined error
			H	H	Equal
L	L	H	H	IN	Write
X	H	H	H	H	Device disabled
X	X	L	H	†	Memory reset

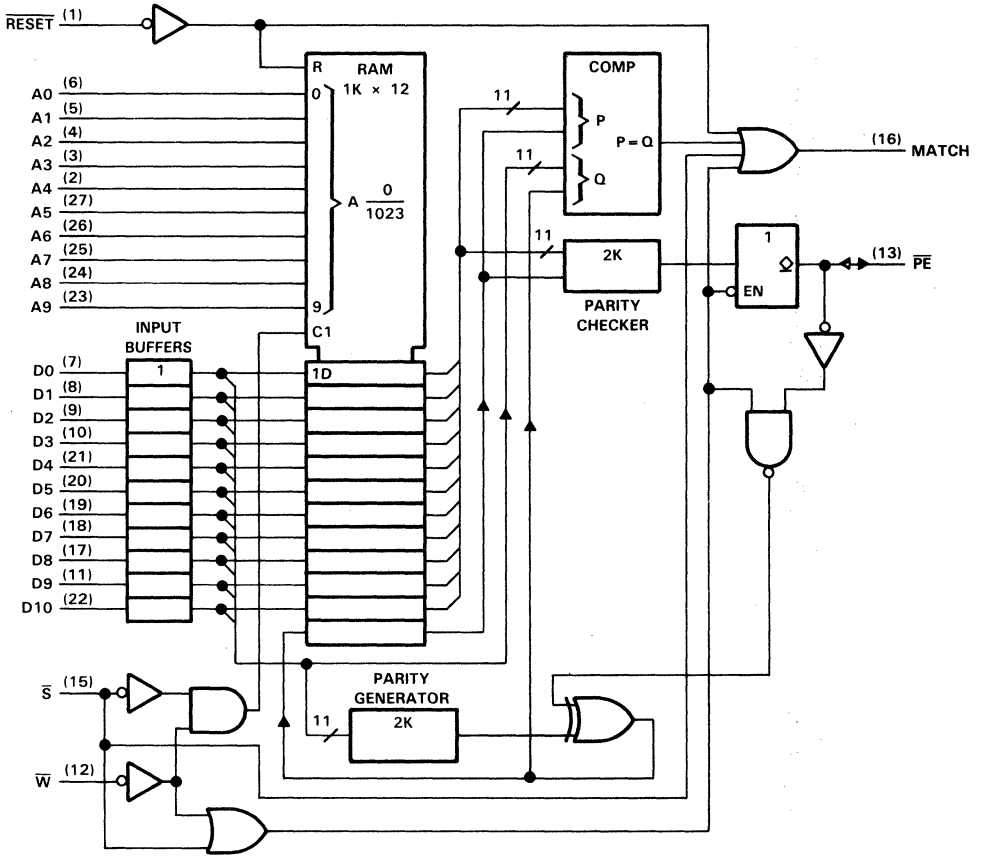
† The state of $\overline{PE}$ is dependent on inputs $\overline{W}$ and $\overline{S}$.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	6	Address inputs, Addresses 1 of 1024 random access memory locations. Must be stable for the duration of the write cycle.
A1	5	
A2	4	
A3	3	
A4	2	
A5	27	
A6	26	
A7	25	
A8	24	
A9	23	
D0	7	Data inputs. Compared with memory locations addressed by A0-A9 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provides input data to the RAM when $\overline{W}$ and $\overline{S}$ are at V_{IL}.
D1	8	
D2	9	
D3	10	
D4	21	
D5	20	
D6	19	
D7	18	
D8	17	
D9	11	
D10	22	
GND	14	Ground
MATCH	16	When MATCH output is at V_{OH} during a compare cycle, D0-D10 plus generated parity equals the contents of the 12-bit memory location addressed by A0-A10. MATCH is also driven high during deselect and reset. Since the 'ACT2153 features an open-drain MATCH output, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	13	Parity Error input/output. During compare cycles. $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. During write cycles, $\overline{PE}$ can force a parity error into the 12th-bit location specified by A0-A9 when $\overline{PE}$ is taken to V_{IL}. $\overline{PE}$ is an open-drain output so an external pull-up resistor of 220 Ω minimum is required.
$\overline{RESET}$	1	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RESET}$ is at V_{IL}.
$\overline{S}$	15	Chip Select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH and $\overline{PE}$ high when $\overline{S}$ is at V_{IH}.
V_{CC}	28	Supply voltage
$\overline{W}$	12	Write control input. Writes D0-D0 and generated parity into RAM and forces MATCH high when $\overline{W}$ and $\overline{S}$ are at V_{IL}. Places selected device in compare mode when $\overline{W}$ is at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage range, any input . . . . . −1.5 to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±25 mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) . . . . . ±25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}): D0-D4 . . . . . ±25 mA
MATCH . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2153) and $\overline{PE}$ outputs only				5.25	V
I_{OH}	High-level output current, MATCH ('ACT2151)				−8	mA
I_{OL}	Low-level output current	MATCH – 'ACT2151			8	mA
		MATCH – 'ACT2153			24	mA
		$\overline{PE}$			24	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with – 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{OH}	MATCH ('ACT2153) and $\overline{PE}$	V_{CC} = 5.25 V, V_{OH} = 5.25 V			10	µA
V_{OH}	MATCH ('ACT2151)	V_{CC} = 4.75 V, I_{OH} = −8 mA	3.7			V
V_{OL}	MATCH ('ACT2153)	V_{CC} = 4.75 V, I_{OL} = 24 mA			0.4	V
	MATCH ('ACT2151)	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4	
	$\overline{PE}$	V_{CC} = 4.75 V, I_{OL} = 24 mA			0.4	
I_I		V_{CC} = 5.25 V, V_I = 0–V_{CC}			±5	µA
I_{CC1}	(operating)	V_{CC} = 5.25 V, $\overline{RESET}$ at 3 V, $\overline{S}$ at 0 V		67	125	mA
I_{CC2}	(reset)	V_{CC} = 5.25 V, $\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		3	25	mA
I_{CC3}	(deselected)	V_{CC} = 5.25 V, $\overline{RESET}$ at 3 V, $\overline{S}$ at 3 V		38	105	mA
C_i		f = 1 MHz			5	pF
C_o		f = 1 MHz			6	pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), see Figures 3, 4, and 5

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{a(A-M)}$	Access time from address to MATCH		16	22	ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		21	30	ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		21	30	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		9	16	ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH		10	15	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		7	15	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		7	15	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		6	15	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		7	15	ns
$t_{p(WH-M)}$	Propagation delay, $\overline{W}$ high to MATCH‡		14	20	ns
$t_{p(WH-PE)}$	Propogation delay, $\overline{W}$ high to $\overline{PE}$‡		14	20	ns
$t_{v(A-M)}$	MATCH valid time after change of address	2			ns
$t_{v(D-M)}$	MATCH valid time after change of data	0			ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high	0			ns
$t_{V(A-P)}$	$\overline{PE}$ valid time after change of address	4			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The MATCH and PE outputs will glitch at the end of a write cycle after $\overline{W}$ returns high. These specs indicate when the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}$ returns high. This is Advanced Information and is subject to change without notice.

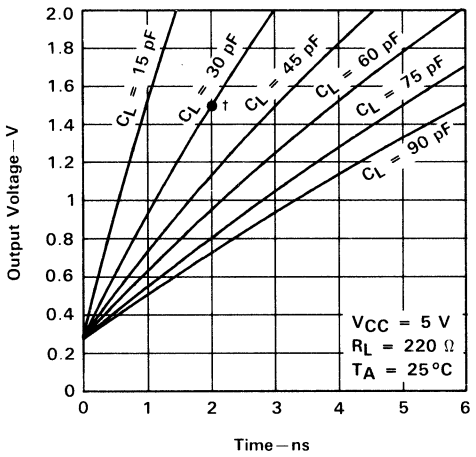
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	35		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	12		ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W}$, writing $\overline{PE}$ (see Note 3)	12		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	10		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	10		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	10		ns
$t_{su(RST)}$	$\overline{RESET}$ inactive setup time before $\overline{W}$ high	15		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		ns
$t_{h(WH-D)}$	Data hold time after $\overline{W}$ high	2		ns
$t_{h(WL-D)}$	Data hold time after $\overline{W}$ low with MATCH high, (see Note 4)	10		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	2		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		ns
t_{AVWH}	Address valid to write enable high	12		ns

NOTES: 3. Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle timing when writing a parity error.
4. $t_{h(WL-D)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high, match will remain high without a glitch low. (As shown in the function table, $\overline{W}$ low forces MATCH high). $t_{h(WL-D)}$ is guaranteed indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH TRANSITION
OF 24-mA OPEN-DRAIN OUTPUTS
FOR VARIOUS LOADS



†Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

FIGURE 1

Figure 1 is provided as a tool to determine how propagation delay specifications for a 24-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 2-ns increase in a specified propagation delay.

PARAMETER MEASUREMENT INFORMATION

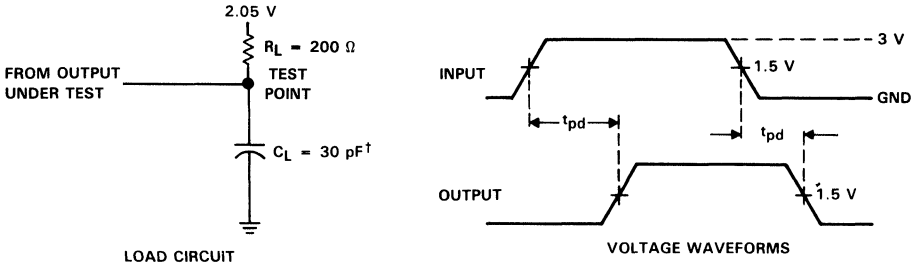


FIGURE 2. 'ACT2151 MATCH OUTPUT

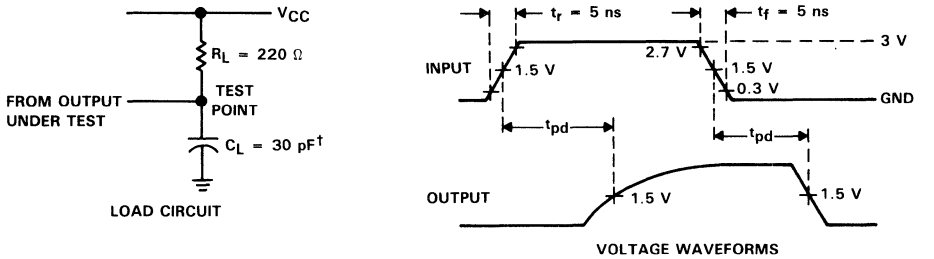
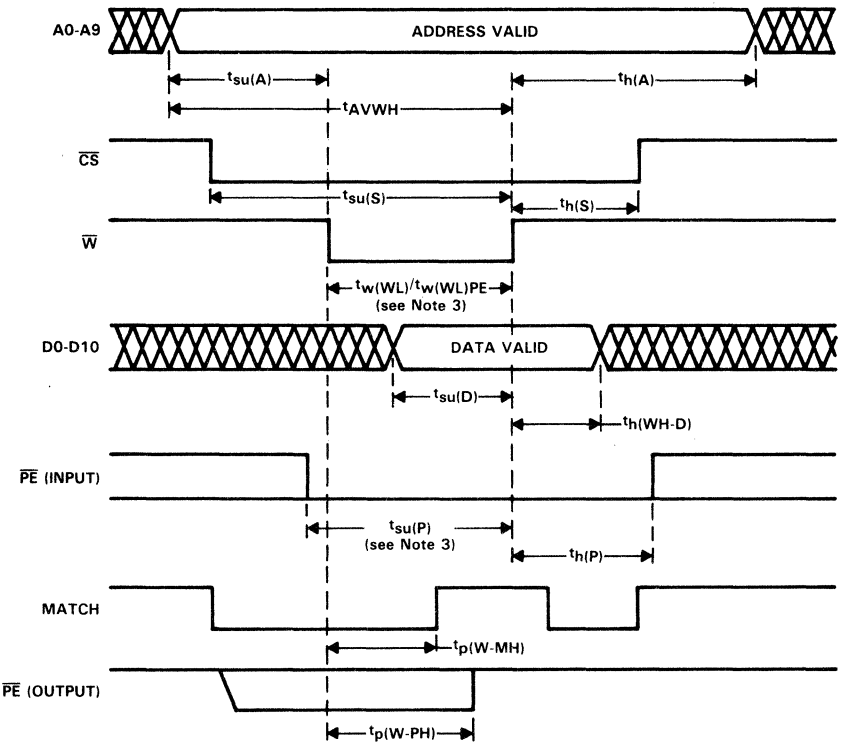


FIGURE 3. OPEN-DRAIN MATCH AND $\overline{PE}$ OUTPUTS

† C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{w(WL)PE}$ and $T_{su(P)}$ apply only during the write cycle when writing a parity error.

FIGURE 4. WRITE CYCLE TIMING

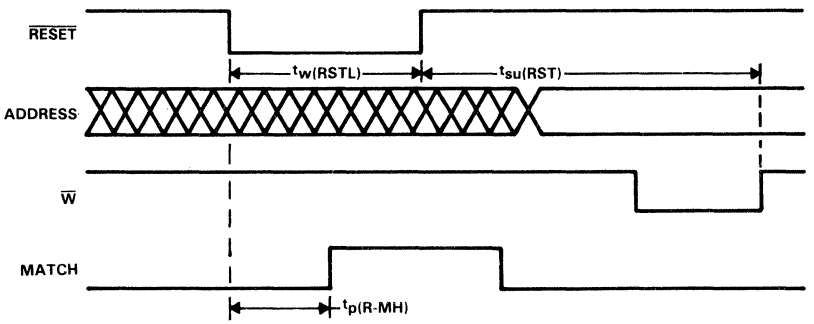


FIGURE 5. RESET CYCLE TIMING

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PARAMETER MEASUREMENT INFORMATION

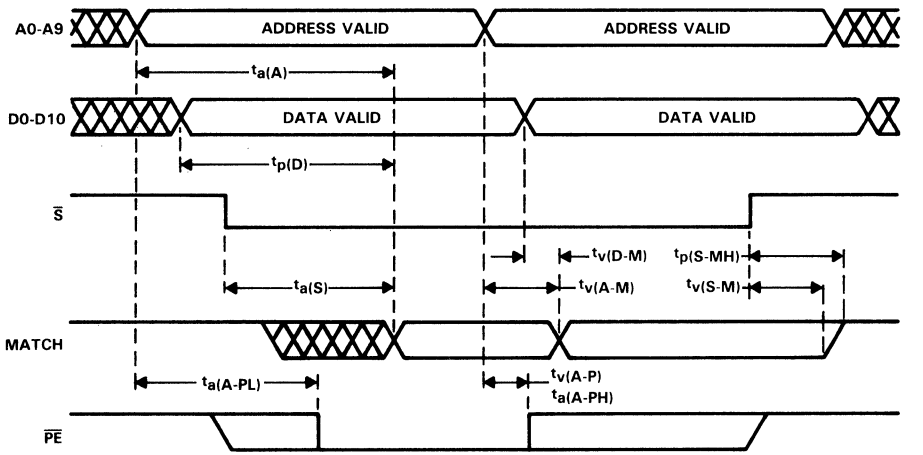


FIGURE 6. COMPARE CYCLE TIMING

APPLICATION INFORMATION

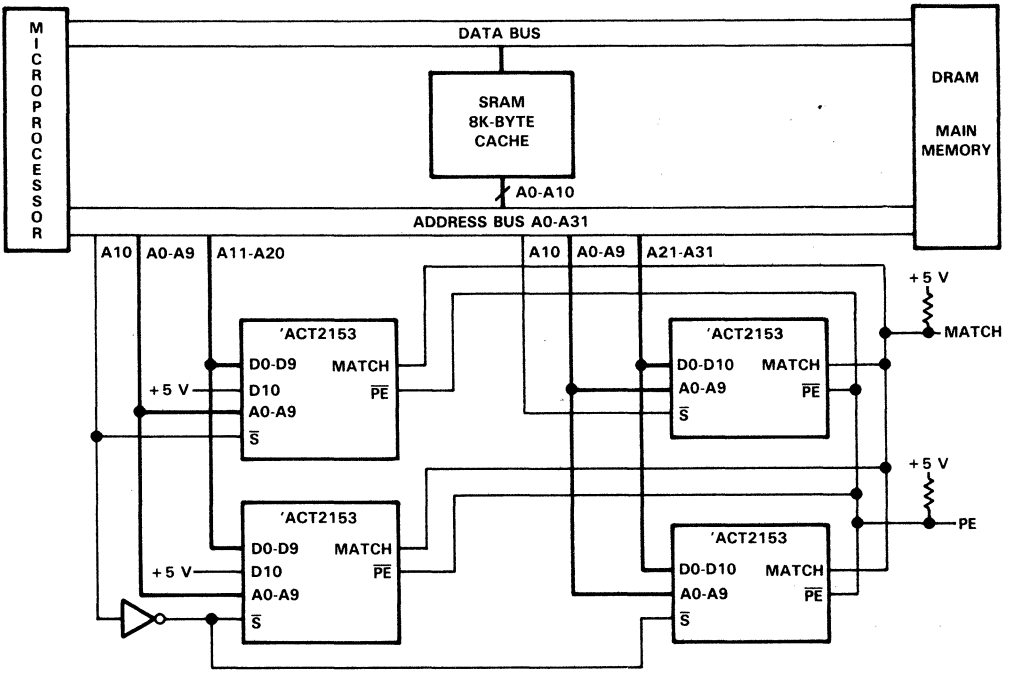
cascading the 'ACT2151 and 'ACT2153

The 'ACT2151 and 'ACT2153 are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A9 inputs of each device with the same index and applying the additional address bits to the D0-D10 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the MATCH output is driven high. It should be noted that a decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH on the 'ACT2153 is an open-drain output for easy AND-tying. Figure 7 shows the 'ACT2153 cascaded.

cache coherency through bus watching

When cache designs are implemented, the problem of cache coherency is always a concern. One solution to this problem is to implement bus-watching using the 'ACT2151 or 'ACT2153. By storing the same tags in the bus-watcher RAM as are stored in the cache tag RAM, the bus-watcher will indicate a hit every time a cache address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 10 shows a possible bus-watcher implementation.

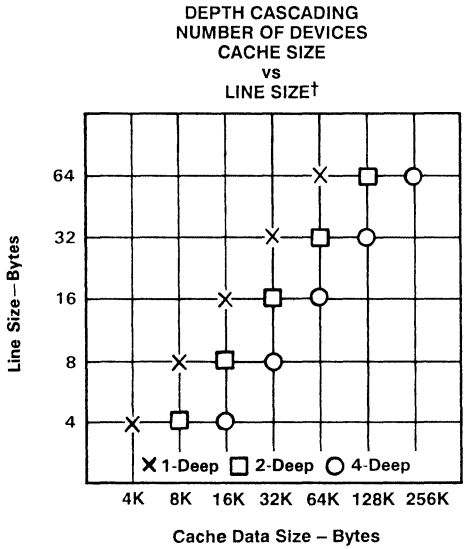
APPLICATION INFORMATION



NOTE: This application assumes a line size of 4 bytes and that a valid bit is used.

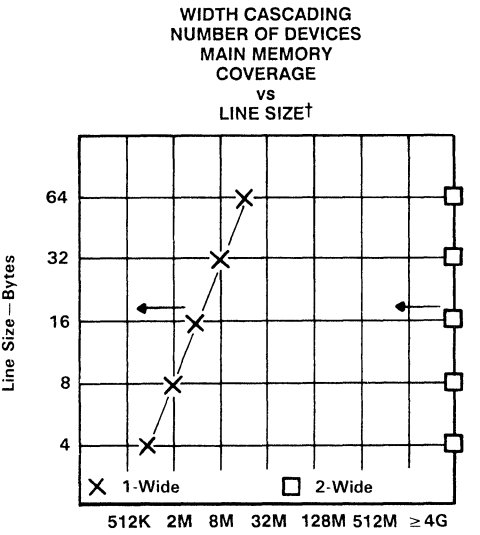
FIGURE 7. CASCADING THE 'ACT2153

APPLICATION INFORMATION



† Direct-Mapped Caches – One tag per line

FIGURE 8



† One Tag/line. Assumes a word length of 32 Bits.

FIGURE 9

depth cascading

For two-way caches, each solution shown is moved to the right one increment doubling the cache size, and the number of devices used. Four-way cache designs using the 'ACT2151 (or 'ACT2153) will quadruple each solution shown within Figure 8.

width cascading

Memory coverage assumes one bit used as a valid bit (See Figure 9). Each solution for given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth, memory coverage increases, i.e.; two deep maps twice as much memory.

usage explanation and example

Figures 8 and 9 provide a quick means for determining if the 'ACT2151 (or 'ACT2153) will provide a good solution and the number of devices needed for implementation. For example, a design requires 32K bytes of direct-mapped cache, memory coverage of 8M and a line size of 16 bytes. (A 16-byte line size means each tag location maps four 32-bit words of cached data.) From Figure 8, it is determined that two 'ACT2151s (or 'ACT2153s) will provide a 32K-byte cache with a 16-byte line. From Figure 9, it is determined that one 'ACT2151 (or 'ACT2153) will map 8M of memory, provided it is cascaded once, in the depth direction (i.e., two deep). Therefore, two deep by one wide is equivalent to two 'ACT2151s (or 'ACT2153s). Two devices provide perfect solution.

APPLICATION DATA

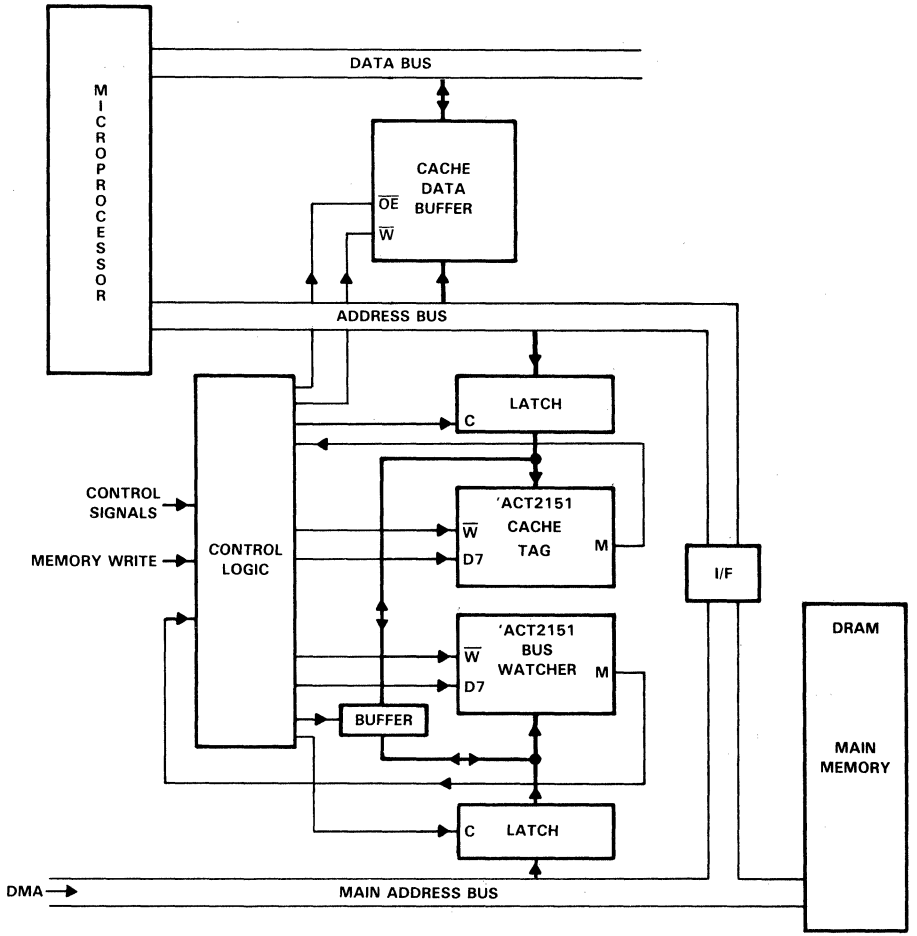
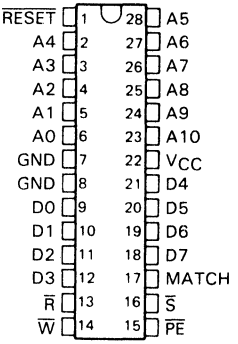


FIGURE 10. BUS WATCHING USING THE 'ACT2151

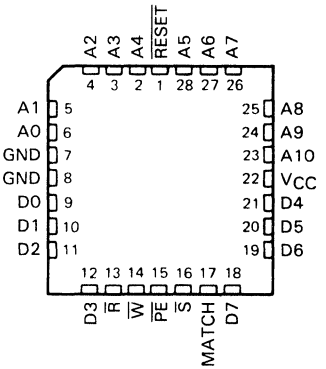
D3156, DECEMBER 1988—REVISED MARCH 1990

- **Fast Address to Match Delay 20 or 25 ns Max**
- **Common I/O with Read Feature**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generator and Checking**
- **Parity Error Output, Force Parity Error Input**
- **Easily Expandable**
- **Choice of Open-Drain or Totem-Pole MATCH Output**
- **EPIC™ (Enhanced Performance Implanted CMOS) 1-μm Process**
- **Fully TTL-Compatible**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The 'ACT2152A and 'ACT2154A cache address comparators consist of a high-speed 2K × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. These cache address comparators are easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2152A has a totem-pole MATCH output while the 'ACT2154A has an open-drain MATCH output for easy AND-tying.

If $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the data D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output on $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

EPIC is a trademark of Texas Instruments Incorporated.
These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

A read mode is provided with the 'ACT2152A and 'ACT2154A, which allows the contents of RAM to be read at the D0-D7 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low, and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high after reset for every addressed memory location, indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

These cache address comparators operate from a single +5-V supply and are offered in 28-pin plastic 600-mil ceramic side brazed, dual-in-line and PLCC packages.

The 'ACT2152A and 'ACT2154A are characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A10] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}
or: $\overline{R}$ = V_{IL}

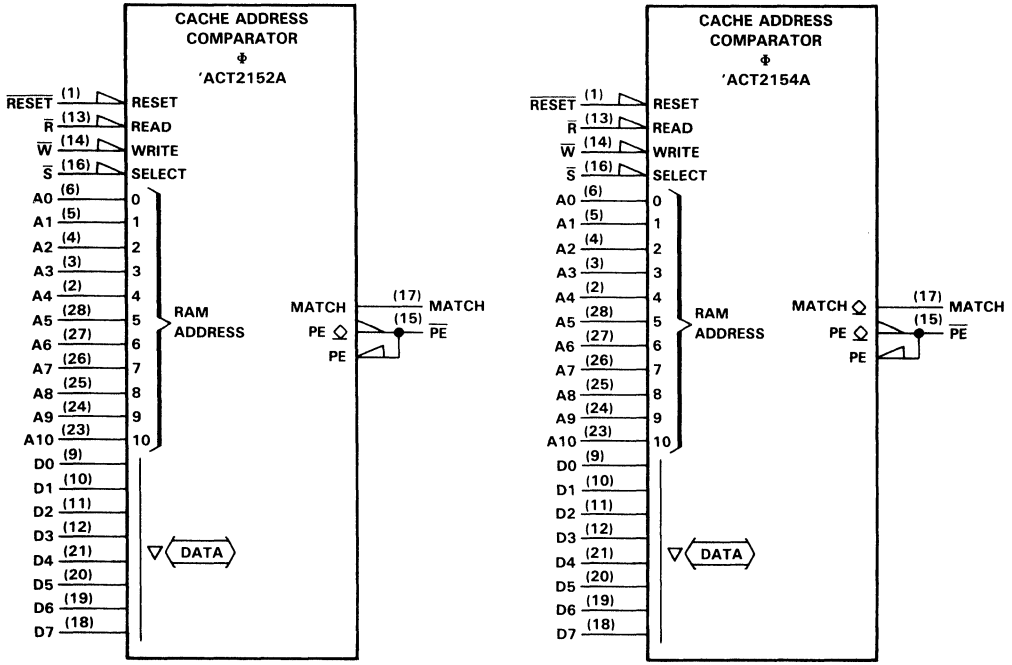
MATCH = V_{OL} if: [A0-A10] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

INPUTS				OUTPUTS		I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	MATCH	$\overline{PE}$	D0-D7	
H	L	L	H	H	H	Output	Read
H	H	L	H	L	L	Input	Parity error
				L	H		Not equal
				H	L		Undefined error
				H	H		Equal
L	X	L	H	H	IN	Input	Write
X	X	H	H	H	H	Hi-Z	Device disabled
X	X	X	L	H	†	†	Memory reset

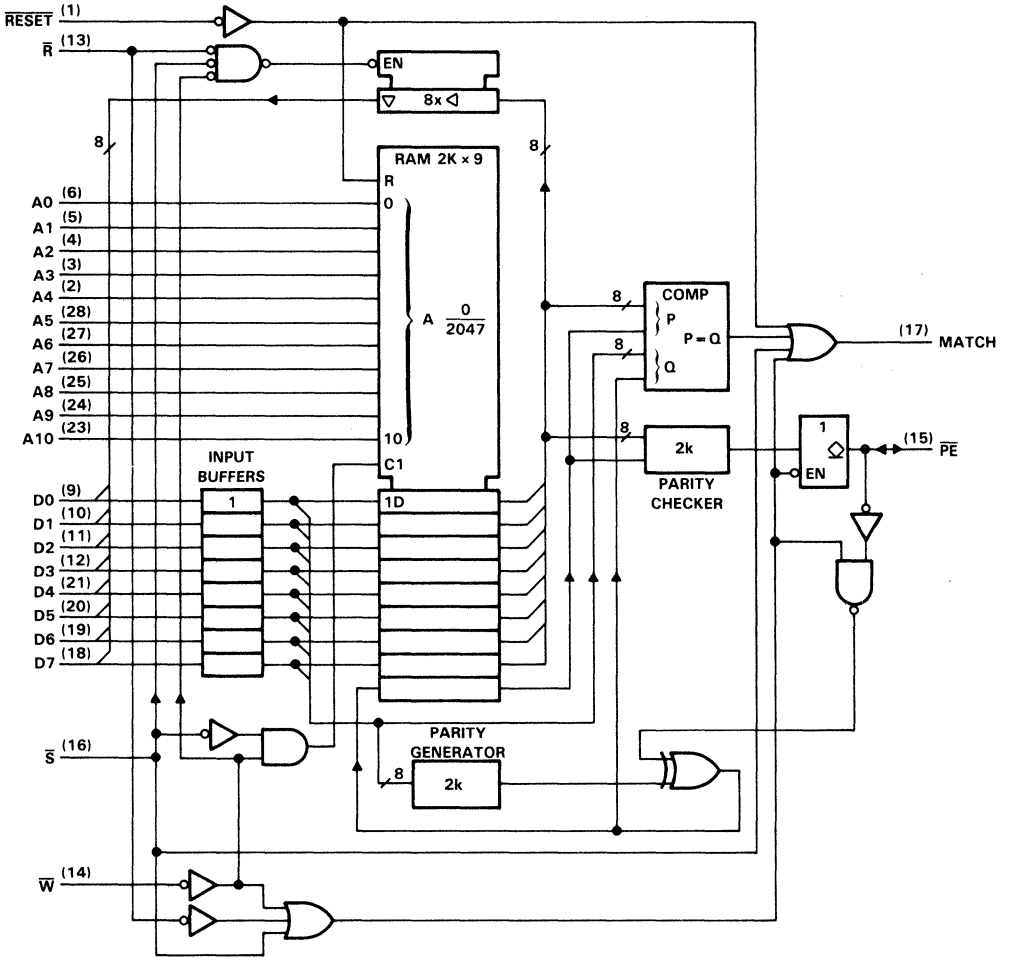
†The state of these pins is dependent on inputs $\overline{W}$, $\overline{R}$, and $\overline{S}$.

logic symbol†



†These symbols are in accordance with ANSI/IEEE Std 91-1984.

functional block diagram (positive logic)



TEXAS INSTRUMENTS
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TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	6	Address inputs. Addresses 1 of 2048 random access memory locations. Must be stable for the duration of the write cycle.
A1	5	
A2	4	
A3	3	
A4	2	
A5	28	
A6	27	
A7	26	
A8	25	
A9	24	
A10	23	
D0	9	Data inputs/outputs. D0-D7 are data inputs during the compare and write modes. D0-D7 are data outputs during the read mode.
D1	10	
D2	11	
D3	12	
D4	21	
D5	20	
D6	19	
D7	18	
GND	7,8	Ground
MATCH	17	When MATCH output is at V_{OH} during a compare cycle, D0-D7 plus generated parity equals the contents of the 9-bit memory location addressed by A0-A10. MATCH is also driven high during deselect, reset, and read. Since the 'ACT2154A features an open-drain MATCH output, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	15	Parity error input/output. During compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. During write cycles, $\overline{PE}$ can force a parity error into the 9th-bit location specified by A0-A10 when $\overline{PE}$ is taken to V_{IL}. $\overline{PE}$ is an open-drain output so an external pull-up resistor of 220 Ω minimum is required.
$\overline{R}$	13	Read input. When $\overline{R}$ and $\overline{S}$ are at V_{IL} and $\overline{W}$ is at V_{IH}, addressed data is output to the D0-D7 pins and the MATCH and $\overline{PE}$ outputs are forced high.
$\overline{RESET}$	1	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RESET}$ is at V_{IL}.
$\overline{S}$	16	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH and $\overline{PE}$ high when $\overline{S}$ is at V_{IH}.
V_{CC}	22	Supply voltage
$\overline{W}$	14	Write control input. Writes D0-D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ and $\overline{S}$ are at V_{IL}. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage, any input . . . . . −1.5 to 7 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Output diode current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}): D0—D8 . . . . . ±25 mA
MATCH, $\overline{PE}$ . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage, write or compare cycles		2.2		V_{CC}+0.5	V
V_{IH}	High-level input voltage, read cycle		2.6		V_{CC}+0.5	
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2154A) and $\overline{PE}$ outputs only				5.5	V
I_{OH}	High-level output current, MATCH ('ACT2152A) and D0-D7				−8	mA
I_{OL}	Low-level output current	MATCH — 'ACT2152A			8	mA
		MATCH — 'ACT2154A			24	mA
		$\overline{PE}$			24	mA
		D0-D7			8	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, in which the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with −1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{OH}	High-level output current	MATCH ('ACT2154A) and $\overline{PE}$	V_{OH} = 5.5 V, V_{CC} = 5.5 V			10			10	μA
V_{OH}	High-level output voltage	MATCH ('ACT2152A) and D0-D7	I_{OH} = −8 mA, V_{CC} = 4.5 V	3.7			3.7			V
V_{OL}	Low-level output voltage	MATCH - 'ACT2154A	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	V
		MATCH - 'ACT2152A	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
		$\overline{PE}$	I_{OL} = 24 mA, V_{CC} = 4.5 V			0.4			0.4	
		D0-D7	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	
I_I	Input current		V_I = 0 − V_{CC}, V_{CC} = 5.5 V			±5			±5	μA
I_{OZ}	Off-state output current		V_O = 0 − V_{CC}, V_{CC} = 5.5 V, $\overline{S}$ at V_{IH}			±10			±10	μA
I_{CC1}	Supply current (operative)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		85	125		85	125	mA
I_{CC2}	Supply current (reset)		$\overline{RESET}$ at 0 V, V_{CC} = 5.5 V, $\overline{S}$ at 0 V		5	25		5	25	mA
I_{CC3}	Supply current (deselected)		$\overline{RESET}$ at 3 V, V_{CC} = 5.5 V, $\overline{S}$ at 3 V		75	105		75	105	mA
C_i	Input capacitance		f = 1 MHz			5			5	pF
C_o	Output capacitance		f = 1 MHz			6			6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), see Figures 1 and 2

compare cycle

PARAMETER			SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-M)}$	Access time from address to MATCH			14	20		18	25	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$ high or low			17	25		22	28	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH	ACT2152A		9	15		11	15	ns
		ACT2154A		8	12		11	15	
$t_{p(D-M)}$	Propagation time, data inputs to MATCH			7	12		10	16	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high			6	12		10	18	ns
$t_{p(RSTH-M)}$	Propagation delay, $\overline{RESET}$ high to MATCH‡			20	30		20	30	ns
$t_{p(RST-PE)}$	Propagation delay, $\overline{RESET}$ high to PE‡			20	30		20	30	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high			6	10		9	12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high			6	10		9	14	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high			8	11		9	11	ns
$t_{p(WH-M)}$	Propagation delay, $\overline{W}$ high to MATCH‡			14	20		14	20	ns
$t_{p(WH-PE)}$	Propagation delay, $\overline{W}$ high to $\overline{PE}$‡			14	20		14	20	ns
$t_{v(A-M)}$	MATCH valid time after change of address		2	6		2	8		ns
$t_{v(D-M)}$	MATCH valid time after change of data		0	3		0	5		ns
$t_{v(S-M)}$	MATCH valid time (low) after $\overline{S}$ high		0	3		0	5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address		0	3		0	5		ns

read cycle

PARAMETER		SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-D)}$	Read Access time from address to D0-D7		20	27		24	30	ns
$t_{en(S-D)}$	Enable time, $\overline{S}$ low to D0-D7		12	20		15	20	ns
$t_{en(R-D)}$	Enable time, $\overline{R}$ low to valid D0-D7 output		10	18		12	20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{R}$ low to MATCH high		6	10		9	12	ns
$t_{p(R-PH)}$	Propagation time, $\overline{R}$ low to $\overline{PE}$ high		6	10		9	15	ns
$t_{dis(R-D)}$	Disable time, $\overline{R}$ to D0-D7 (from high or low level)		10	18		12	20	ns
$t_{dis(S-D)}$	Disable time, $\overline{S}$ to D0-D7 (from high or low level)		10	18		12	20	ns
$t_{dis(W-D)}$	Disable time, $\overline{W}$ to D0-D7 (from high or low level)		10	18		12	20	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The MATCH and PE outputs will glitch at the end of a write or reset cycle after $\overline{W}$ or $\overline{RESET}$ returns high. These specifications indicate when the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}$ or $\overline{RESET}$ returns high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		SN74ACT2152A-20 SN74ACT2154A-20			SN74ACT2152A-25 SN74ACT2154A-25			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	25			30			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	12			15			ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	18			18			ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0			0			ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	10			10			ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	7			7			ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	10			10			ns
$t_{su(RST)}$	$\overline{RESET}$ inactive setup time before $\overline{W}$ low	15			15			ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0			0			ns
$t_{h(WH-D)}$	Data hold time after $\overline{W}$ high	2			5			ns
$t_{h(WL-D)}$	Data hold time after $\overline{W}$ low with MATCH high, (see Note 4)	10			10			ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	2			5			ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0			0			ns
t_{AVWH}	Address valid to write enable high	12			15			ns

NOTES: 3. The pulse-duration requirement specified by $t_{w(WL)PE}$ is only necessary when a parity error exists, (i.e., PE output is low) prior to writing data with correct parity (i.e., PE input is high during write). Parameter $t_{su(P)}$ applies only during the write cycle timing when writing a parity error.

4. $t_{h(WL-D)}$ guarantees that when $\overline{W}$ is taken low during a compare cycle with MATCH high, match will remain high without a low glitch. (As shown in the function table, $\overline{W}$ low forces MATCH high). $t_{h(WL-D)}$ is guaranteed indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

PARAMETER MEASUREMENT INFORMATION

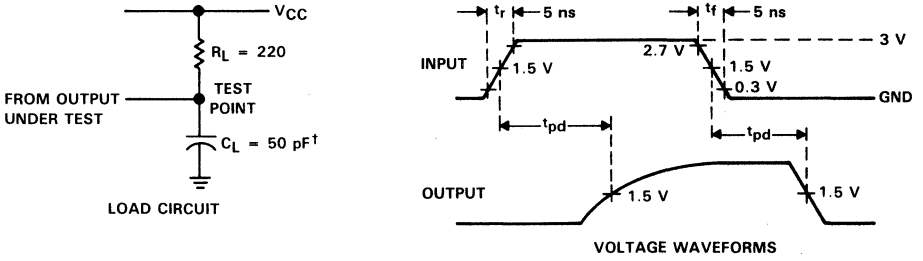


FIGURE 1. OPEN-DRAIN OUTPUTS

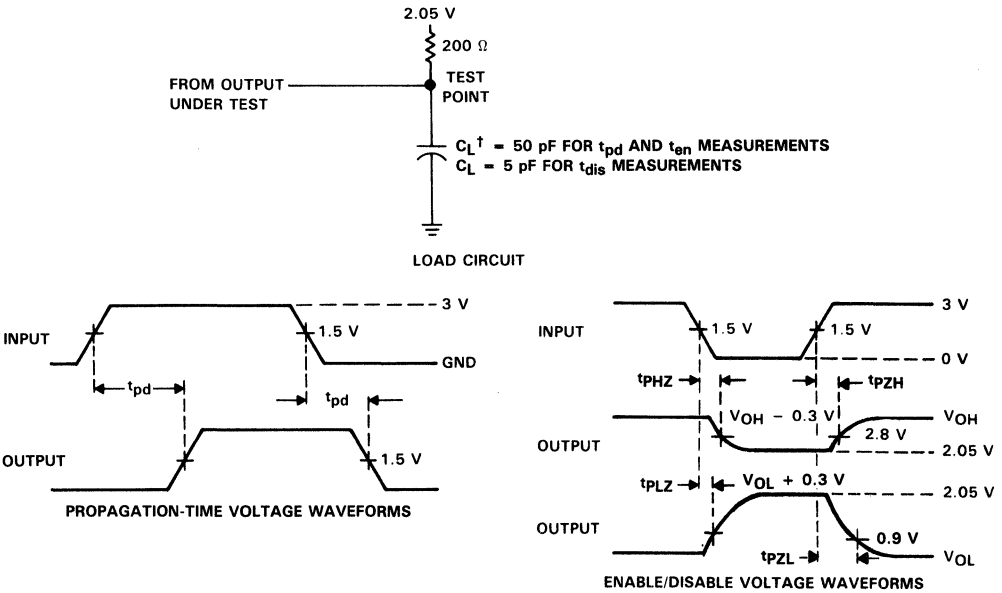
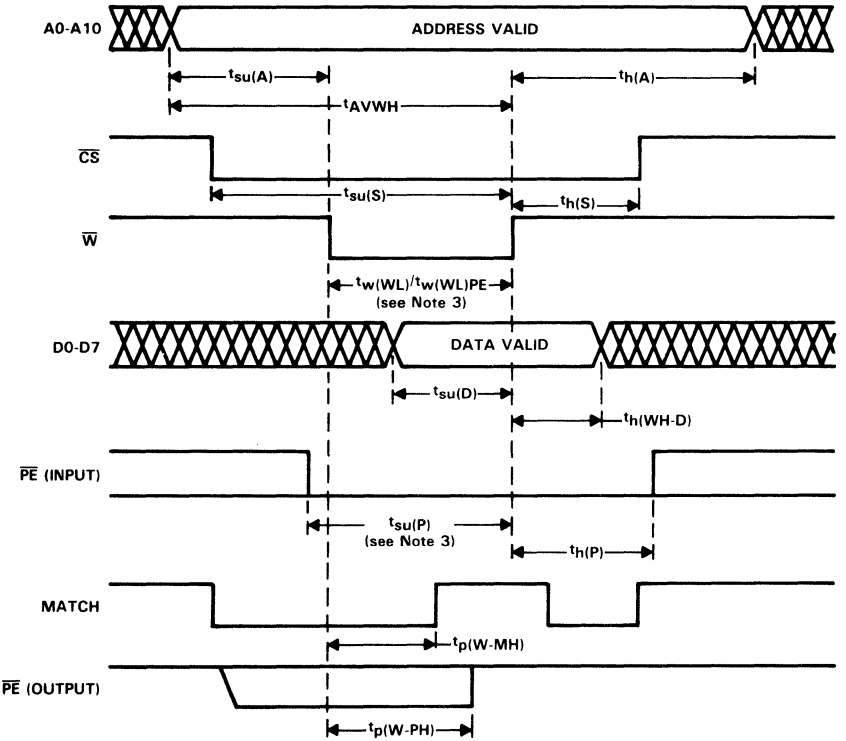


FIGURE 2. ALL OTHER OUTPUTS

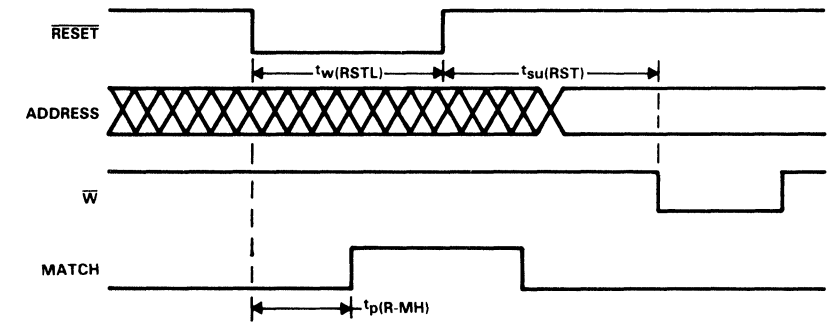
†C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

write cycle timing



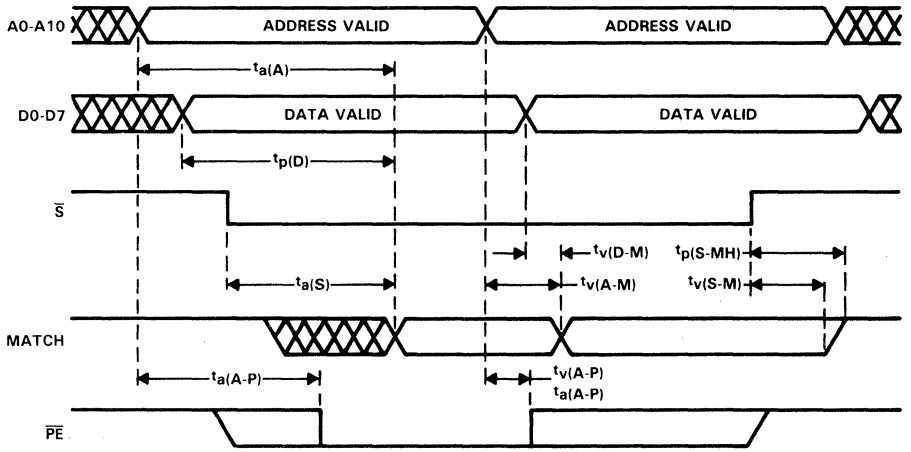
reset cycle timing



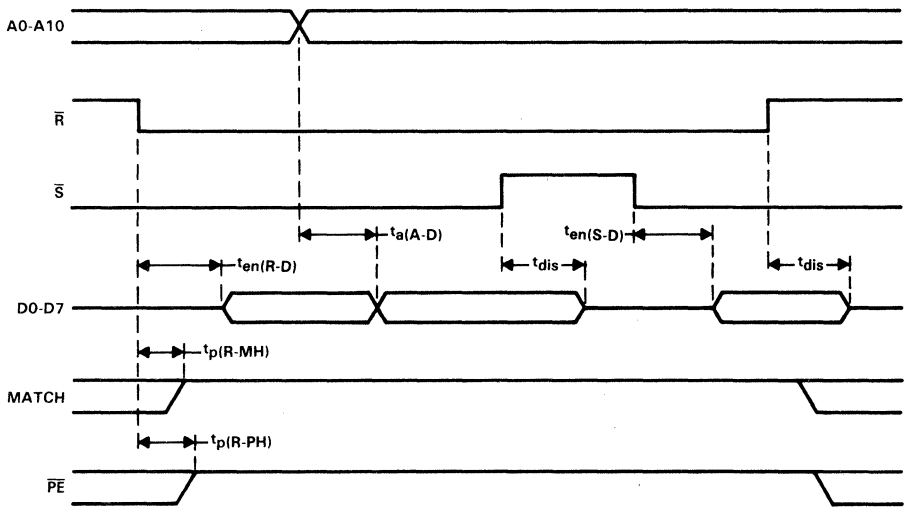
NOTE 3: Parameters $t_{w(WL)PE}$ and $t_{su(P)}$ apply only during the write cycle when writing a parity error.

PARAMETER MEASUREMENT INFORMATION

compare cycle timing



read cycle timing



APPLICATION INFORMATION

cascading the 'ACT2152A and 'ACT2154A

The 'ACT2152A and 'ACT2154A are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D7 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the MATCH output is driven high. It should be noted that a decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH on the 'ACT2154A is an open-drain output for easy AND-tying. Figure 3 shows the 'ACT2154A cascaded.

cache coherency through bus watching

When cache designs are implemented, the problem of cache coherency is always a concern. One solution to this problem is to implement bus-watching using the 'ACT2152A or 'ACT2154A. By storing the same tags in the bus-watcher RAM as are stored in the cache tag RAM, the bus-watcher will indicate a hit every time a cache address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 4 shows a possible bus-watcher implementation.

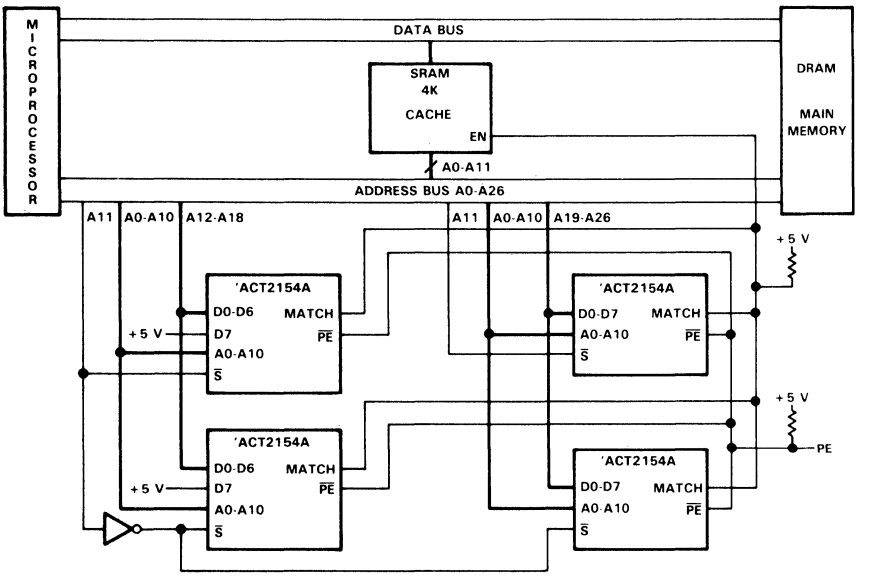


FIGURE 3. CASCADING THE 'ACT2154A

TYPICAL APPLICATION INFORMATION

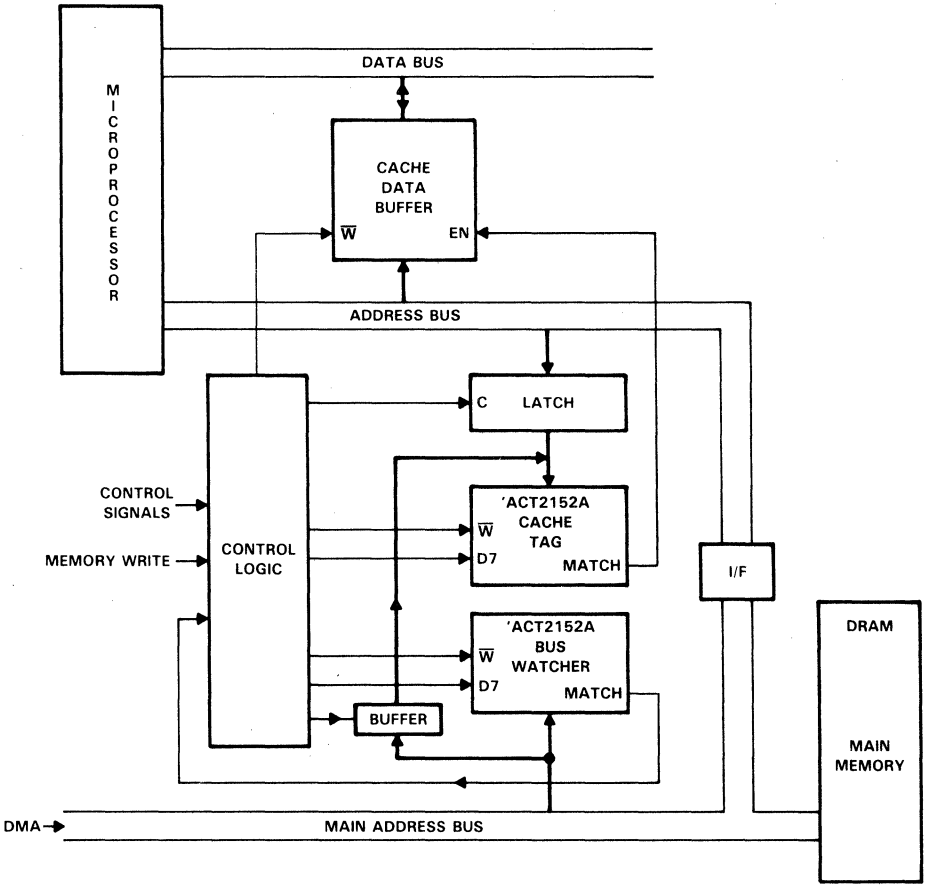
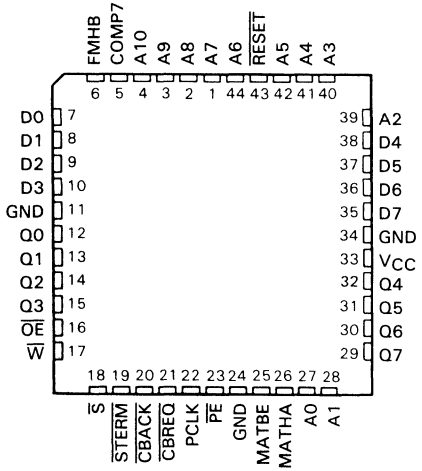


FIGURE 4. BUS WATCHING USING THE 'ACT2152A

D3076, NOVEMBER 1988—REVISED JUNE 1990

- **Address to MATCH Time . . . 22 ns Max**
- **Supports Motorola MC68030 Cache Burst Fill with No Added Wait States**
- **Upward Compatibility for Motorola MC68030 Speed Upgrades**
- **Cache Data RAM with Parity and Internal Burst Counter**
- **Dirty Bit Storage Capability for Use in Copy-Back Caches**
- **Separate I/O Supports Copy-Back**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ACT2155 burst cache address comparator/data RAM consists of a high-speed 2K × 9 static RAM array, 2-bit burst counter and control circuitry, parity generator, parity checker, and 8-bit high-speed comparator. The 'ACT2155 is fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2155 provides a valuable building block for building fast, efficient caches. By combining this device with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

The 'ACT2155 was designed to be used as the tag comparator and data RAM necessary to provide a cache that supports the burst-fill requirement of the Motorola MC68030 microprocessor. The 'ACT2155 directly interfaces with the Motorola MC68030 providing four long words to the processor in four clock cycles. By interfacing directly with the processor, at least 10 ns in delay time is saved when comparing this solution with discrete designs. Even though the 'ACT2155 is designed for use with the Motorola MC68030 processor, it can be used with other processors to implement write-through or copy-back class caches.

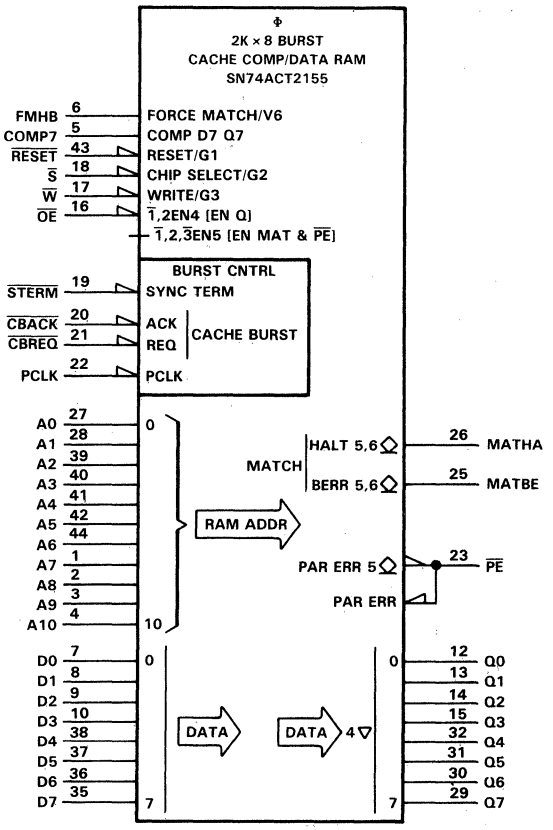
PARTIAL FUNCTION TABLE

INPUTS					OUTPUTS				FUNCTION
$\overline{S}$	$\overline{W}$	$\overline{RESET}$	$\overline{OE}$	FMHB	MATHA†	MATBE	$\overline{PE}$/(I/O)	Q0-Q7	
X	X	X	X	H	H	H	‡	‡	Force MATHA and MATBE unconditionally high
H	X	X	X	X	H	H	Disabled	Hi-Z	Deselect. Inhibits write, read, and compare.
L	H	H	X	L	H or L	H or L	L	‡	Parity error
					L	L	H		Not equal
					H	H	H		Equal
X	H	L	X	X	H	H	Disabled	Hi-Z	Memory reset unconditionally
L	L	H	H	X	H	H	Input	Hi-Z	Write, Low on $\overline{PE}$ forces parity error.
L	L	H	L	X	H	H	Input	Low	Write. Low on $\overline{PE}$ forces parity error.
L	H	H	L	X	‡	‡	Enabled	Enabled	Read

†During the burst mode, MATHA is forced high.
‡The state of these pins is dependent on inputs shown as irrelevant (X).

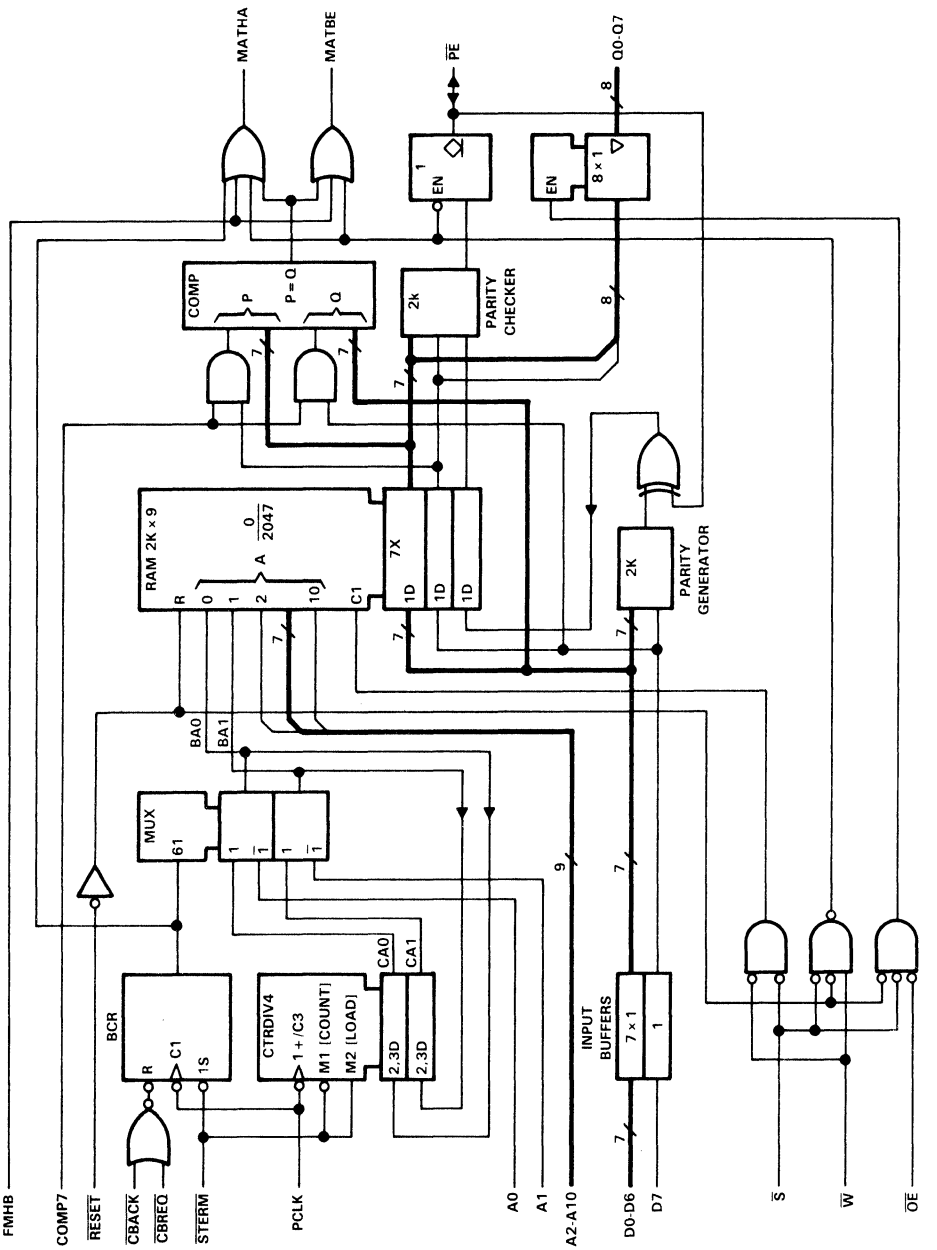
These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	27	Address inputs. Addresses memory location in the 2K × 9 RAM. When in burst mode, address bits A0 and A1 are driven from the internal 2-bit counter independently of the A0 and A1 inputs.
A1	28	
A2	39	
A3	40	
A4	41	
A5	42	
A6	44	
A7	1	
A8	2	
A9	3	
A10	4	
$\overline{\text{CBACK}}$	20	Cache Burst Knowledge input. If $\overline{\text{CBACK}}$ is high, the internal burst control register (BCR) is asynchronously reset, causing inputs A0 and A1 to drive the internal BA0 and BA1 address lines.
$\overline{\text{CBREQ}}$	21	Cache Burst Request input. If CBREQ is high, the internal burst control register (BCR) is asynchronously reset, causing inputs A0 and A1 to drive the internal BA0 and BA1 lines.
D0	7	Data (tag) inputs. Provide input to the RAM when $\overline{\text{W}}$ and $\overline{\text{S}}$ are low. If $\overline{\text{W}}$ is high, the selected device compares D0-D7 to the addressed 8-bit memory locations. Bit D7 and stored bit Q7 can be removed from the comparison by taking COMP7 low.
D1	8	
D2	9	
D3	10	
D4	38	
D5	37	
D6	36	
D7	35	
FMHB	6	Force Match Halt Berr input. If this input is high, the MATBE and MATHA outputs are unconditionally forced high.
MATBE	25	Match Berr output. During the compare mode, MATBE is high when D0-D7 (D0-D6 if COMP7 is low) equals Q0-Q7 (Q0-Q6 if COMP7 is low). MATBE is also high during deselect, write, and reset and when FMHB is high. Since MATBE is an open-drain output, an external pullup resistor of 220 Ω minimum is required. MATBE could be high in the compare mode when a parity error exists.
MATHA	26	Match Halt output. During the compare mode, MATHA is high when D0-D7 (D0-D6 if COMP7 is low) equals Q0-Q7 (Q0-Q6 if COMP7 is low). MATHA is also high during deselect, write, and reset, when FMHB is high, and when the burst control register (BCR) is set. Since MATHA is an open-drain output, an external pullup resistor of 220 Ω minimum is required. MATHA could be high in compare mode when a parity error exists.
COMP7	5	COMP7 input. If COMP7 is low, RAM input and output bits D7 and Q7 are taken out of the comparison allowing this bit to be used for a copy-back status (dirty bit). If COMP7 is high, D7 and Q7 are included in the comparison.
$\overline{\text{OE}}$	16	Output Enable input. $\overline{\text{OE}}$ enables (low) or disables (high) Q0-Q7 when $\overline{\text{S}}$ is low and $\overline{\text{RESET}}$ is high.
PCLK	22	Processor Clock input. The burst control and counter registers are clocked by a high-to-low transition on the PCLK input.
$\overline{\text{PE}}$	23	Parity Error output/input. During compare cycles, a low at $\overline{\text{PE}}$ indicates a parity error in the stored data. During write cycles, $\overline{\text{PE}}$ forces a parity error into the parity bit location specified by A0-A10 when $\overline{\text{PE}}$ is taken low. $\overline{\text{PE}}$ an open-drain output and requires a pullup resistor of 220 Ω minimum. $\overline{\text{PE}}$ is disabled during write, reset, and deselect.

TERMINAL FUNCTIONS (continued)

PIN NAME	PIN NO.	DESCRIPTION
Q0	12	Data outputs. Q0-Q7 display the contents of the addressed memory location when $\overline{S}$ and $\overline{OE}$ are low and RESET is high. Q0-Q7 is disabled during deselect, reset, and when $\overline{OE}$ is high. Enabled outputs are forced low when $\overline{W}$ is low.
Q1	13	
Q2	14	
Q3	15	
Q4	32	
Q5	31	
Q6	30	
Q7	29	
$\overline{RESET}$	43	Reset input. Asynchronously clears the 2K × 9-bit RAM array to a low with valid parity independent of the $\overline{S}$ pin when $\overline{RESET}$ is low. By tying a single data input high, a false match will not occur when D0-D7 inputs are low.
$\overline{S}$	18	Chip select input. Enables device when $\overline{S}$ is low. If $\overline{S}$ is high, MATBE and MATHA are forced high and $\overline{PE}$ and Q0-Q7 are disabled.
$\overline{STERM}$	19	Synchronous Termination input. On the next PCLK falling edge after $\overline{STERM}$ goes low (while $\overline{CBACK}$ and $\overline{CBEQ}$ are low), the 2-bit counter increments the binary value applied to the A0 and A1 inputs and the burst control register (BCR) is set. The set burst control register will cause the counter bits to drive the internal BA0 and BA1 address lines. The burst control register remains set until $\overline{CBREQ}$ or $\overline{CBACK}$ goes high. Taking $\overline{STERM}$ high during a burst holds the counter at the present count.
$\overline{W}$	17	Write control input. Writes D0-D7 and generated parity into the addressed memory location when the device is selected and $\overline{W}$ is low. When $\overline{W}$ is low, MATBE and MATHA are forced high and $\overline{PE}$ is disabled.

operation as an address comparator

The 'ACT2155 compares the contents of the memory location addressed by A0-10 with the address bits applied at D0-D7. An equality is indicated by a high level on the MATBE and MATHA outputs. A low-level output on $\overline{PE}$ signifies a parity error in the addressed internal RAM data. During a write cycle, address bits on D0-D7 plus generated odd parity are written in the 9-bit memory location addressed by A0-A10. Also during write, a parity error may be forced for diagnostic purposes by holding $\overline{PE}$ low.

operation in the burst mode

The 'ACT2155 contains burst control circuitry consisting of a 2-bit wrap-around counter, a mux, and a burst-control register (BCR). The BCR controls the mux which selects A0 and A1 from either the input terminals or from the 2-bit counter. When $\overline{CBREQ}$ or $\overline{CBACK}$ is high, the BCR is asynchronously reset and inputs A0 and A1 drive the RAM. On the next falling edge of PCLK after $\overline{STERM}$ is taken low, the BCR is set and the counter bits (CA0 and CA1) drive the RAM. At the same time that the BCR is set ($\overline{STERM}$ low and a PCLK falling edge), the binary value of A0 and A1 in the counter is incremented. The counter can be held at any count by taking $\overline{STERM}$ high as long as BCR remains set. When the BCR is set, MATHA is forced high.

operation as a data RAM

The 'ACT2155 can be used as a 2K × 8 data RAM with separate I/O, a four word burst mode and parity generation and checking. When using this device as a data RAM, the FMHB input should be tied high to prevent MATHA and MATBE from switching.

using the 'ACT2155 with the Motorola MC68030

The 'ACT2155 interfaces with the Motorola MC68030 through use of 'ACT2155 input signals $\overline{\text{STERM}}$, $\overline{\text{CBREQ}}$, PCLK, $\overline{\text{CBACK}}$, and output signals MATBE and MATHA. Match outputs MATBE and MATHA can be tied directly to processor inputs BERR and HALT respectively. As long as the requested information is in cache, the BERR and HALT signals remain high. When a miss occurs (MATBE and MATHA low), BERR and HALT are driven low simultaneously causing the bus cycle to be retried (rerun). A high level applied at the FMHB input forces MATBE and MATHA high to prevent continuous rerun.

The 'ACT2155 was designed to be used as the tag comparator and data RAM necessary to provide a cache that meets the Motorola MC68030 internal cache burst fill requirement by supplying four long words to the processor in four clock cycles. When the Motorola MC68030 requests a burst fill, a single address is supplied. If the requested information is in the external cache, the 'ACT2155 will indicate a hit. If $\overline{\text{STERM}}$ is low, address bits A1-A0 (A3-A2 from the processor) will be incremented on each PCLK falling edge and the MATBE output will indicate a hit or a miss. If a miss occurs, MATBE will drive BERR low, causing the Motorola MC68030 to abort the burst cycle and to run with the data it received. MATHA is held high during a burst by the BCR. The timing diagram in Figure 7 shows burst mode operation.

The 'ACT2155 internal counter can also be used when writing tag and data into the cache when the burst fill is done from main memory. When $\overline{\text{STERM}}$ is taken high (inserting processor wait states), the 2-bit counter is held at the present count. The counter will continue to increment on the first PCLK falling edge after $\overline{\text{STERM}}$ returns low. When $\overline{\text{CBACK}}$ or $\overline{\text{CBREQ}}$ returns high, the mux will select input pins A0 and A1 to drive the RAM. Figure 2 shows a Motorola MC68030 burst request with data in main memory. For more information on using the 'ACT2155 with the Motorola MC68030, see the *SN74ACT2155/56 Cache Enhances MC68030 Processor Performance* application note.

cascading the 'ACT2155

The 'ACT2155 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D7 inputs. The chip select input allows the 'ACT2155 to be cascaded in depth. When a device is deselected, the MATHA and MATBE outputs are driven high. It should be noted that a decoder can be used to drive the select inputs, since the propagation delay from select to match is much faster than from address to match. MATHA and MATBE are open-drain outputs for easy wired logic. Through the use of the chip select input, the 'ACT2155 can also be cascaded for a deeper cache data buffer. Figure 11 shows the 'ACT2155 cascaded.

initialization

A reset input is provided for initialization. When $\overline{\text{RESET}}$ is taken low, all 2K × 9 RAM locations are cleared to zero (with valid parity) and the MATHA and MATBE outputs are forced high. If a D0-D7 input of zero is compared to any memory location that has not been written into since reset, MATHA and MATBE will be high indicating that D0-D7, plus generated parity, is equal to the reset memory location. $\overline{\text{PE}}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

The burst control register (BCR) must be initialized after power-up by taking $\overline{\text{CBACK}}$ or $\overline{\text{CBREQ}}$ high. This ensures that the A0 and A1 inputs are driving the RAM and not the counter bits CA0 and CA1.

copy-back caches

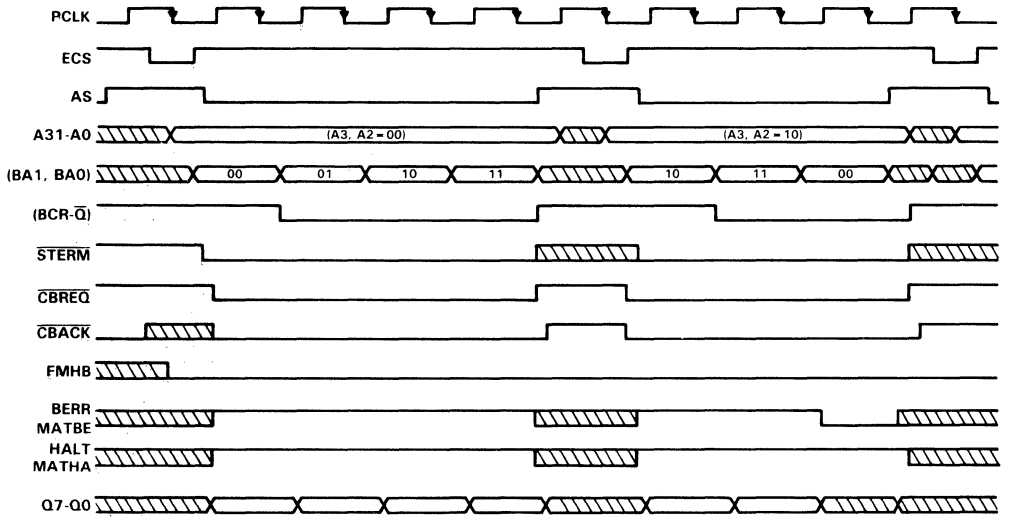
The 'ACT2155 can be used in write through cache designs where writes to cache are immediately sent to main memory, or in copy-back cache designs where a cache write initially only modifies the cache and can later be copied back to main memory. Copy-back caches have an advantage in that the number of

writes to main memory are reduced, thereby reducing bus traffic. To implement a copy-back cache, a dirty bit is needed that indicates whether or not the data is modified from that which is in main memory. The dirty bit is set to 1 when the cache data is modified. Data is only copied back if the dirty bit is set. Otherwise, the data is overwritten.

The COMP7 input of the 'ACT2155 allows bit D7 to be used as a dirty bit. By tying COMP7 low, bits D7 and Q7 are gated out of the comparator so the comparison is only done on D0-D6. With outputs Q0-Q7 enabled ($\overline{OE}$ low), the dirty bit, Q7, can be monitored at the same time as the match signals. If the dirty bit is set during a read or write miss, the tag (Q0-Q6) and data can be stored in latches before writing the new tag and data into cache. Latched data and address can then be copied back to main memory. Figure 12 shows a typical copy-back application.

cache coherency through bus watching

When implementing cache designs, the problem of cache coherency is always a concern. One solution to this problem is to implement bus watching using the 'ACT2155. By storing the same tags in the bus watcher RAM as is stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. The SN74ACT2154 could be used as the bus watcher in a 'ACT2155 write-through design to save board space. Figure 13 shows a possible bus watcher implementation.



MC68030 REQUESTS A CACHE BURST FILL STARTING AT LONG WORD 0. EXTERNAL CACHE ACKNOWLEDGES AND PROVIDES A FULL BURST FILL. IN THIS CASE, ALL 4 LONG WORDS NEEDED TO FILL MC68030 CACHE ARE IN THE X-CACHE. FOUR LONG WORDS ARE LOADED INTO THE MC68030 IN 4 CLOCK CYCLES.

MC68030 REQUESTS A CACHE BURST FILL STARTING AT LONG WORD 2. X-CACHE ACKNOWLEDGES AND PROVIDES LW2 AND LW3, BUT LW0 IS NOT IN THE X-CACHE. THE BURST FILL IS TERMINATED WITH MATBE (BERR). LW0 IS NOT CACHED IN THE MC68030.

FIGURE 1. MOTOROLA MC68030 BURST REQUEST WITH DATA IN EXTERNAL CACHE

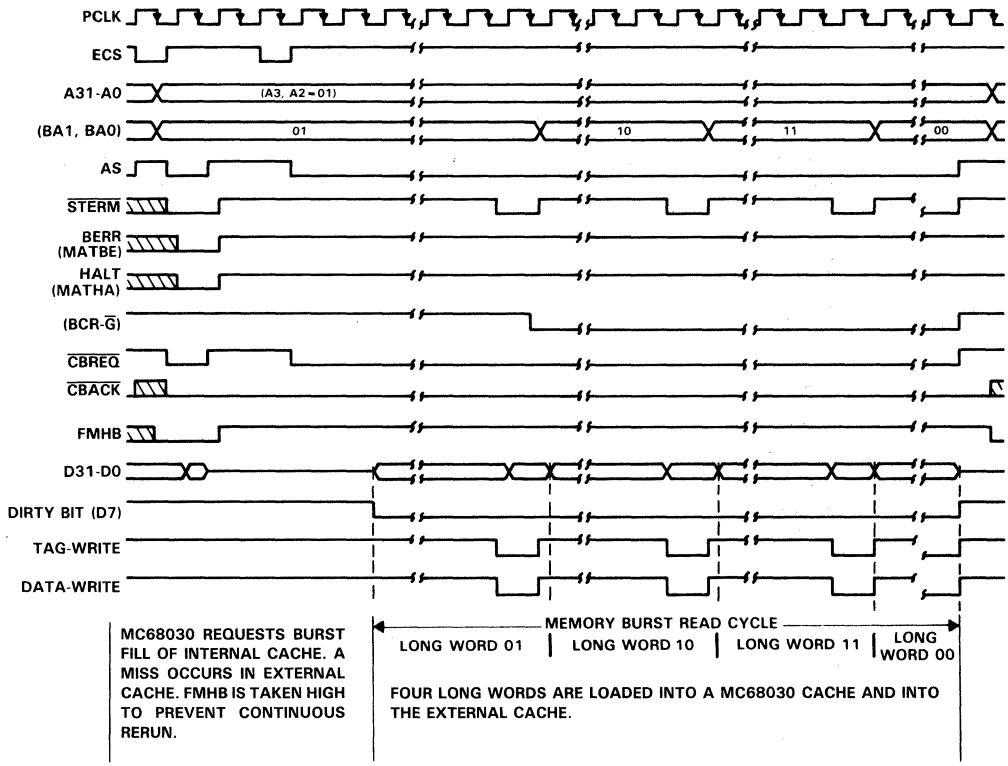


FIGURE 2. MC68030 BURST REQUEST WITH DATA IN MAIN MEMORY

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	−1.5 V to 7 V
Input voltage range, any input	−1.5 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: All voltage values are with respect to GND terminal.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2.2		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATBE, MATHA and $\overline{PE}$ outputs				$V_{CC}+0.5$	V
I_{OH}	High-level output current, Q0-Q7				−8	mA
I_{OL}	Low-level output current	Q0-Q7			8	mA
		MATBE, MATHA, and $\overline{PE}$			24	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with −1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2155-22			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage	Q0-Q7	V_{CC} = 5.5 V, I_{OL} = 8 mA	3.7			V
V_{OL}	Low-level output voltage	MATBE, MATHA or $\overline{PE}$	V_{CC} = 4.5 V, I_{OL} = 24 mA			0.4	V
		Q0-Q7	V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	
I_{OH}	High-level output current	MATBE, MATHA, or $\overline{PE}$	V_{OH} = 5.5 V			10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{OE}$ at V_{IH}			±10	μA
I_I	Input current		V_I = 0 to V_{CC}			±5	μA
I_{CC1}	Supply current (operating)		$\overline{RESET}$ at V_{CC}, $\overline{S}$ at 0 V		85	150	mA
I_{CC2}	Supply current (reset)		$\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		5	50	mA
I_{CC3}	Supply current (deselected)		$\overline{RESET}$ at V_{CC}, $\overline{S}$ at V_{CC}		75	125	mA
C_i	Input capacitance		f = 1 MHz			5	pF
C_o	Output capacitance		f = 1 MHz			6	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

	PARAMETER	SN74ACT2155-22			UNIT
		MIN	TYP‡	MAX	
t_{pd1}	Propagation delay time from address to Q0-Q7		18	27	ns
t_{pd2}	Propagation delay time from address to $\overline{PE}$ low		17	28	ns
t_{pd3}	Propagation delay time from $\overline{S}$ to MATBE and MATHA		8	13	ns
t_{pd4}	Propagation delay time from address to $\overline{PE}$ high		19	28	ns
t_{pd5}	Propagation delay time from $\overline{S}$ to $\overline{PE}$ high		7	15	ns
t_{pd6}	Propagation delay time from address to MATBE and MATHA		17	22	ns
t_{pd7}	Propagation delay time from D0-D7 to MATBE and MATHA		7	15	ns
t_{pd8}	Propagation delay time from $\overline{S}$ high to MATBE and MATHA high		8	13	ns
t_{pd9}	Propagation delay time from $\overline{S}$ low to $\overline{PE}$ low		10	18	ns
t_{pd10}	Propagation delay time from PCLK↓ to MATBE		15	22	ns
t_{pd11}	Propagation delay time from PCLK↓ to MATHA high		14	22	ns
t_{pd12}	Propagation delay time from PCLK↓ to Q0-Q7		18	27	ns
t_{pd13}	Propagation delay time from PCLK↓ to $\overline{PE}$ low		16	28	ns
t_{pd14}	Propagation delay time from PCLK↓ to $\overline{PE}$ high		18	28	ns
t_{pd15}	Propagation delay time from $\overline{W}$ low to Q0-Q7 low		11	20	ns
t_{pd16}	Propagation delay time from $\overline{W}$ high to Q0-Q7		11	20	ns
t_{pd17}	Propagation delay time from $\overline{W}$ low to MATBE and MATHA		6	12	ns
t_{pd18}	Propagation delay time from $\overline{W}$ low to $\overline{PE}$ high		6	12	ns
t_{pd19}	Propagation delay time from $\overline{RESET}$ low to MATBE and MATHA high		7	15	ns
t_{pd20}	Propagation delay time from FMHB to MATHA, MATBE		6	12	ns
t_{en1}	Enable time from $\overline{OE}$ low to Q0-Q7		6	12	ns
t_{en2}	Enable time from $\overline{S}$ low to Q0-Q7		7	15	ns
t_{en3}	Enable time from $\overline{RESET}$ high to Q0-Q7 low		10	20	ns
t_{dis1}	Disable time from $\overline{S}$ high to Q0-Q7		8	15	ns
t_{dis2}	Disable time from $\overline{OE}$ high to Q0-Q7		9	15	ns
t_{dis3}	Disable time from $\overline{RESET}$ low to Q0-Q7		6	15	ns
t_{v1}	Valid time, MATBE and MATHA after change of data	1	4		ns
t_{v2}	Valid time, MATBE and MATHA after change of address	4	10		ns
t_{v3}	Valid time, (low), MATBE and MATHA after $\overline{S}$ high	1	5		ns
t_{v4}	Valid time, $\overline{PE}$ after change of address	4	11		ns
t_{v5}	Valid time, $\overline{PE}$ low after $\overline{S}$ high	1	5		ns
t_{v6}	Valid time, MATBE after PCLK↓	5	10		ns
t_{v7}	Valid time, MATHA after $\overline{CBREQ}$ or $\overline{CBACK}$ high	5	15		ns
t_{v8}	Valid time, MATHA after PCLK↓	5	12		ns
t_{v9}	Valid time, Q0-Q7 after PCLK↓	5	10		ns
t_{v10}	Valid time, $\overline{PE}$ after PCLK↓	3	12		ns
t_{v11}	Valid time, Q0-Q7 after address	3	10		ns
t_{v12}	Valid time, Q0-Q7 after $\overline{CBREQ}$ or $\overline{CBACK}$ high	3	10		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

	PARAMETER	SN74ACT2155-22		UNIT
		MIN	MAX	
t_{w1}	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	12		ns
t_{w2}	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	20		ns
t_{w3}	Pulse duration, $\overline{RESET}$ low	30		ns
t_{w4}	Pulse duration, PCLK high or low	10		ns
t_{su1}	Inactive-state setup time, $\overline{CBREQ}$ before PCLK↓	3		ns
t_{su2}	Inactive-state setup time, $\overline{CBACK}$ before PCLK↓	3		ns
t_{su3}	Setup time, $\overline{STERM}$ before PCLK↓	5		ns
t_{su4}	Setup time, address valid before write enable high	12		ns
t_{su5}	Setup time, $\overline{S}$ before $\overline{W}$ high	10		ns
t_{su6}	Setup time, address before $\overline{W}$ low	0		ns
t_{su7}	Setup time, D0-D7 before $\overline{W}$ high	10		ns
t_{su8}	Setup time, $\overline{PE}$ before $\overline{W}$ high (see Note 3)	8		ns
t_{su9}	Inactive-state setup time, $\overline{RESET}$ before $\overline{W}$ high	15		ns
t_{su10}	Setup time, A0-A1 before PCLK↓	6		ns
t_{su11}	Setup time, $\overline{W}$ high before PCLK↓	−1		ns
t_{h1}	Hold time, $\overline{STERM}$ after PCLK↓	5		ns
t_{h2}	Hold time, address after $\overline{W}$ high	0		ns
t_{h3}	Hold time, $\overline{S}$ after $\overline{W}$ high	0		ns
t_{h4}	Hold time, D0-D7 after $\overline{W}$ high	3		ns
t_{h5}	Hold time, $\overline{PE}$ after $\overline{W}$ high	3		ns
t_{h6}	Hold time, address after PCLK↓	4		ns

†See Parameter Measurement Information for load circuits and voltage waveforms.

NOTE 3. The pulse duration requirement (t_{w2}) is only necessary when a parity error exists. A parity error exists when the $\overline{PE}$ output is low prior to writing data with correct parity (i.e., with the $\overline{PE}$ input high during write). The setup time (t_{su8}) applies only during the write cycle timing when writing a parity error.

PARAMETER MEASUREMENT INFORMATION

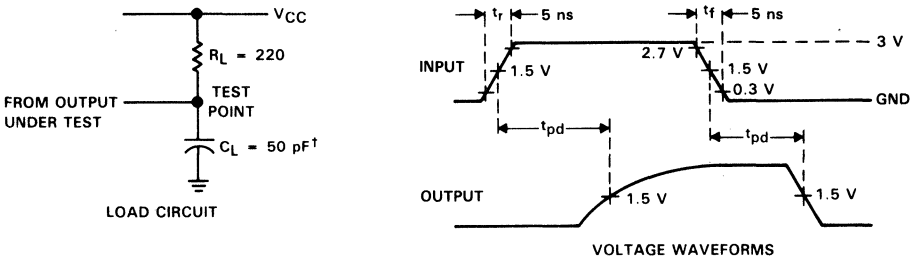


FIGURE 3. OPEN-DRAIN OUTPUTS

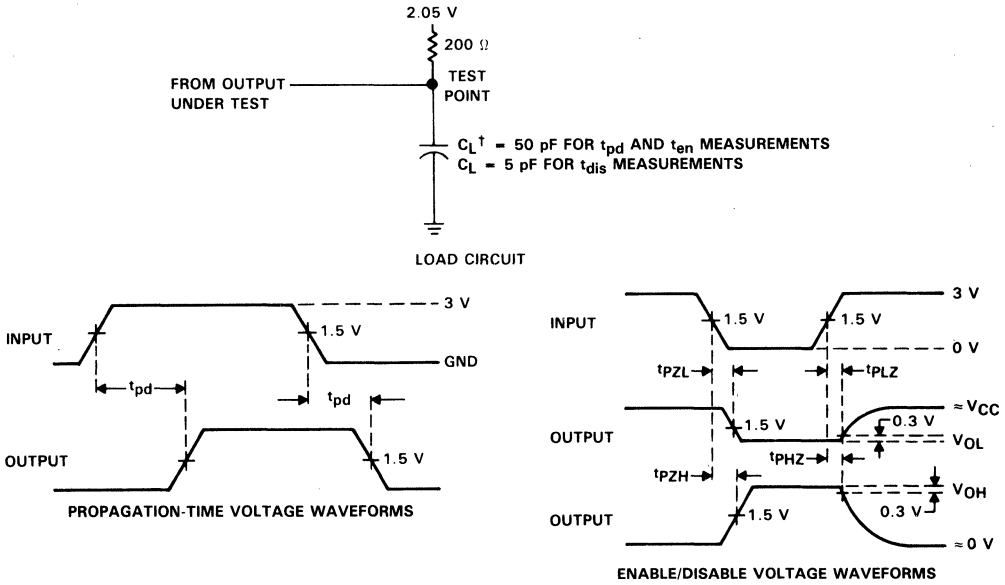


FIGURE 4. ALL OTHER OUTPUTS

†C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

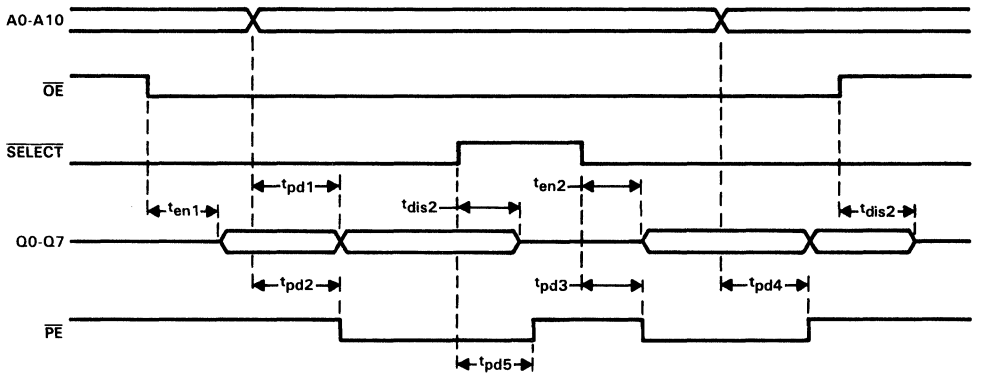


FIGURE 5. READ CYCLE TIMING

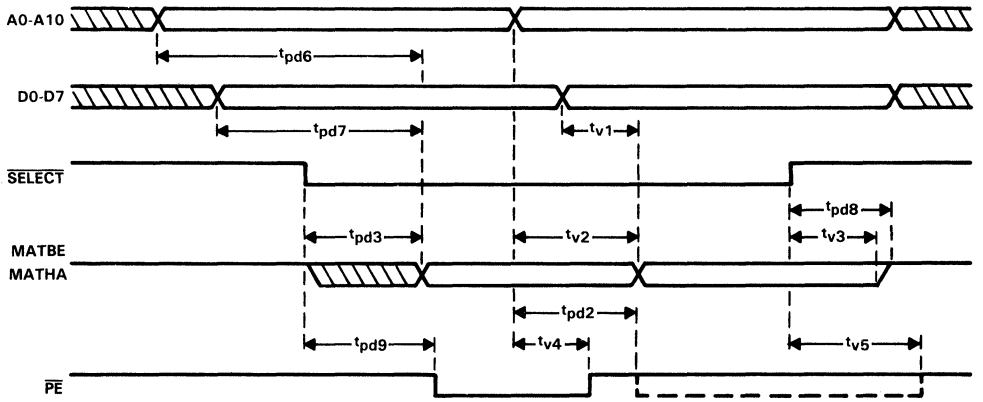


FIGURE 6. COMPARE CYCLE TIMING (WITHOUT BURST REQUEST)

PARAMETER MEASUREMENT INFORMATION

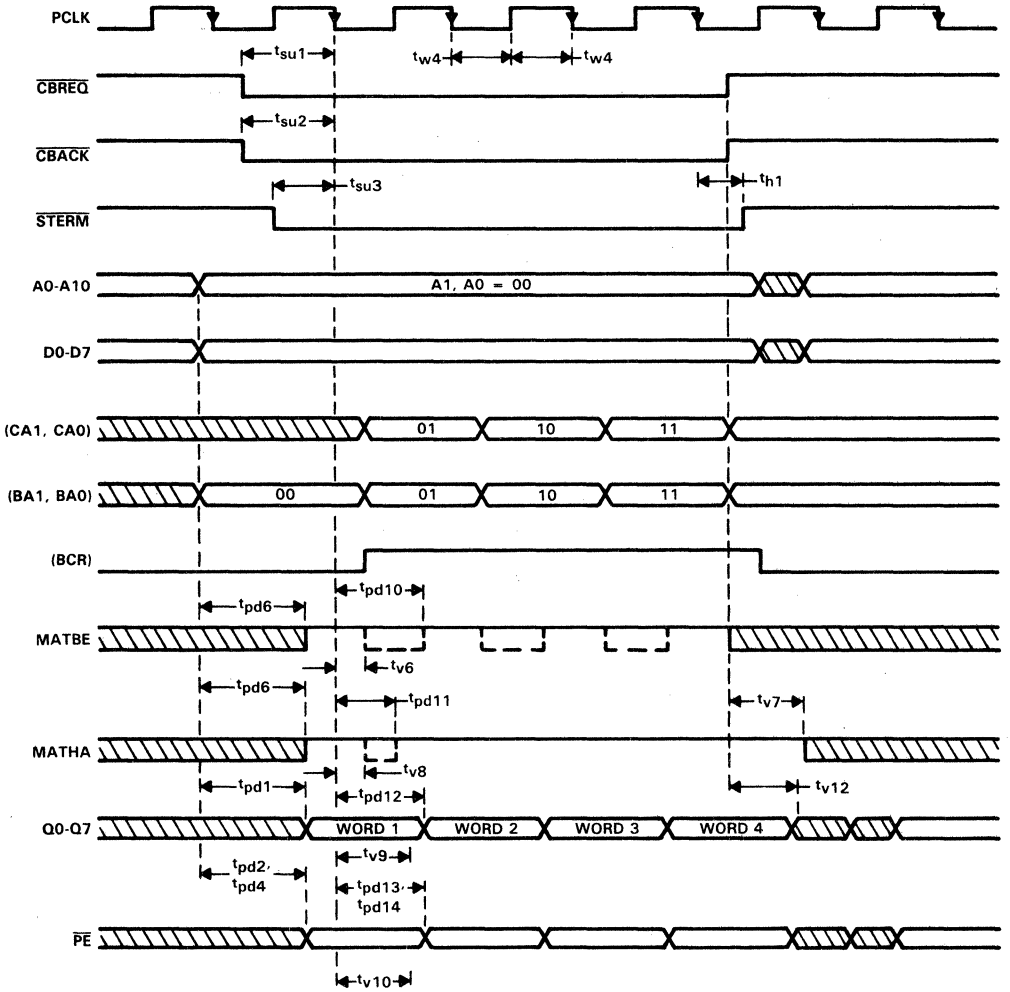


FIGURE 7. BURST COMPARE AND READ CYCLE ($\overline{OE}$ = LOW)

PARAMETER MEASUREMENT INFORMATION

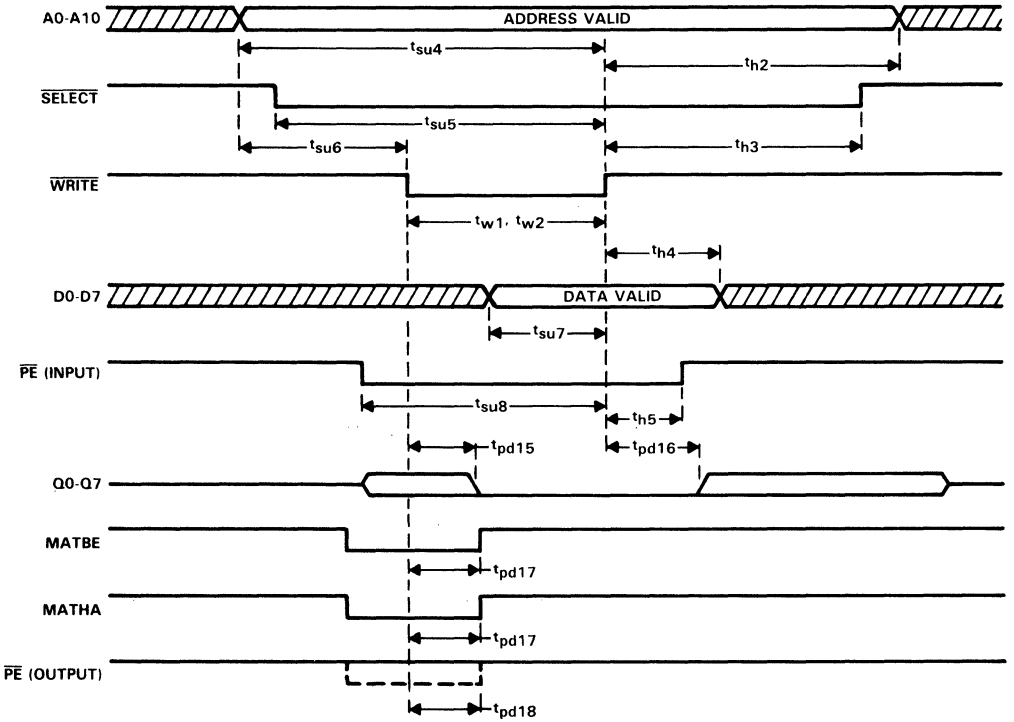


FIGURE 8. WRITE CYCLE TIMING ($\overline{OE}$ = LOW)

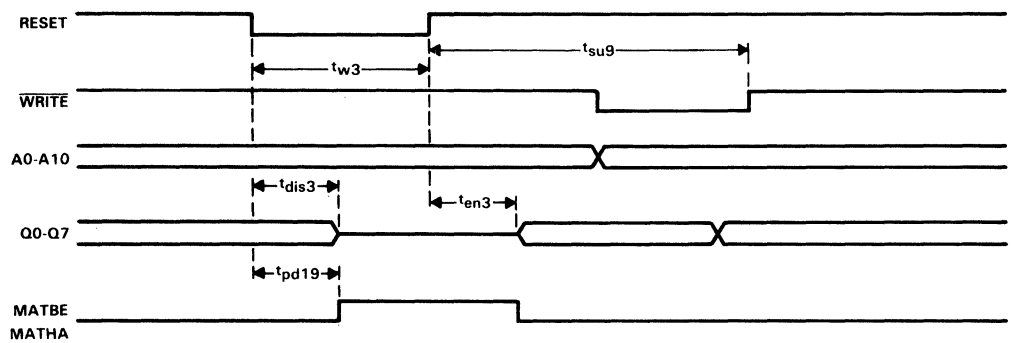


FIGURE 9. RESET CYCLE TIMING ($\overline{OE}$ = LOW)

PARAMETER MEASUREMENT INFORMATION

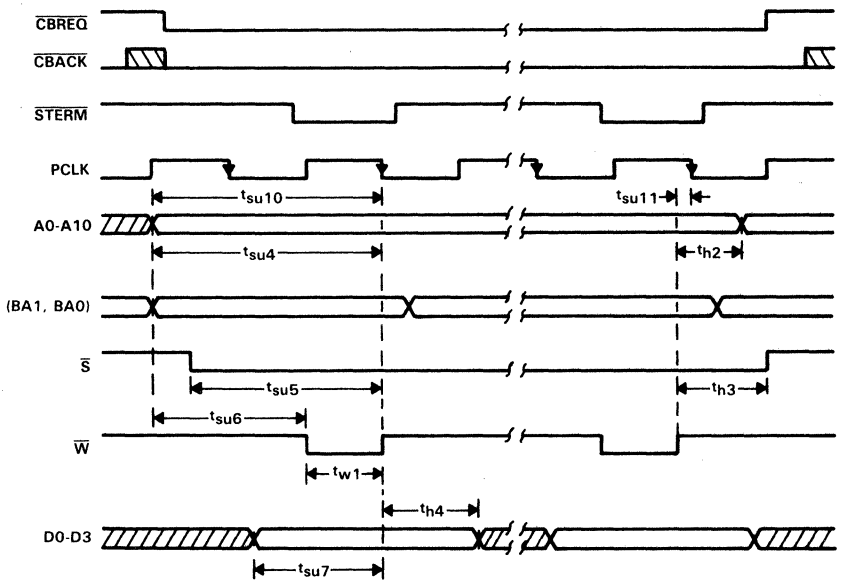


FIGURE 10. BURST-MODE WRITE CYCLE TIMING

APPLICATION INFORMATION

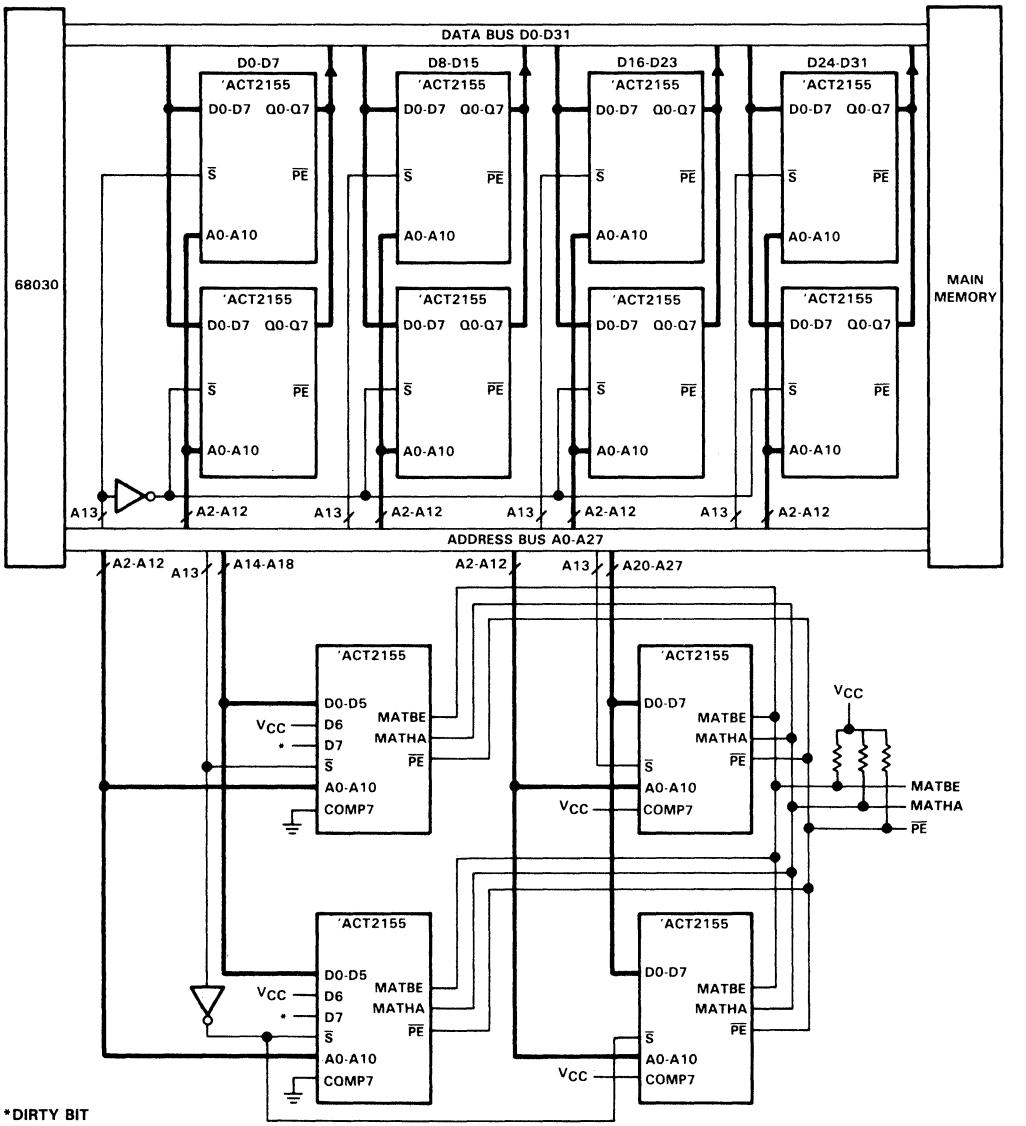


FIGURE 11. CASCADING THE 'ACT2155

APPLICATION INFORMATION

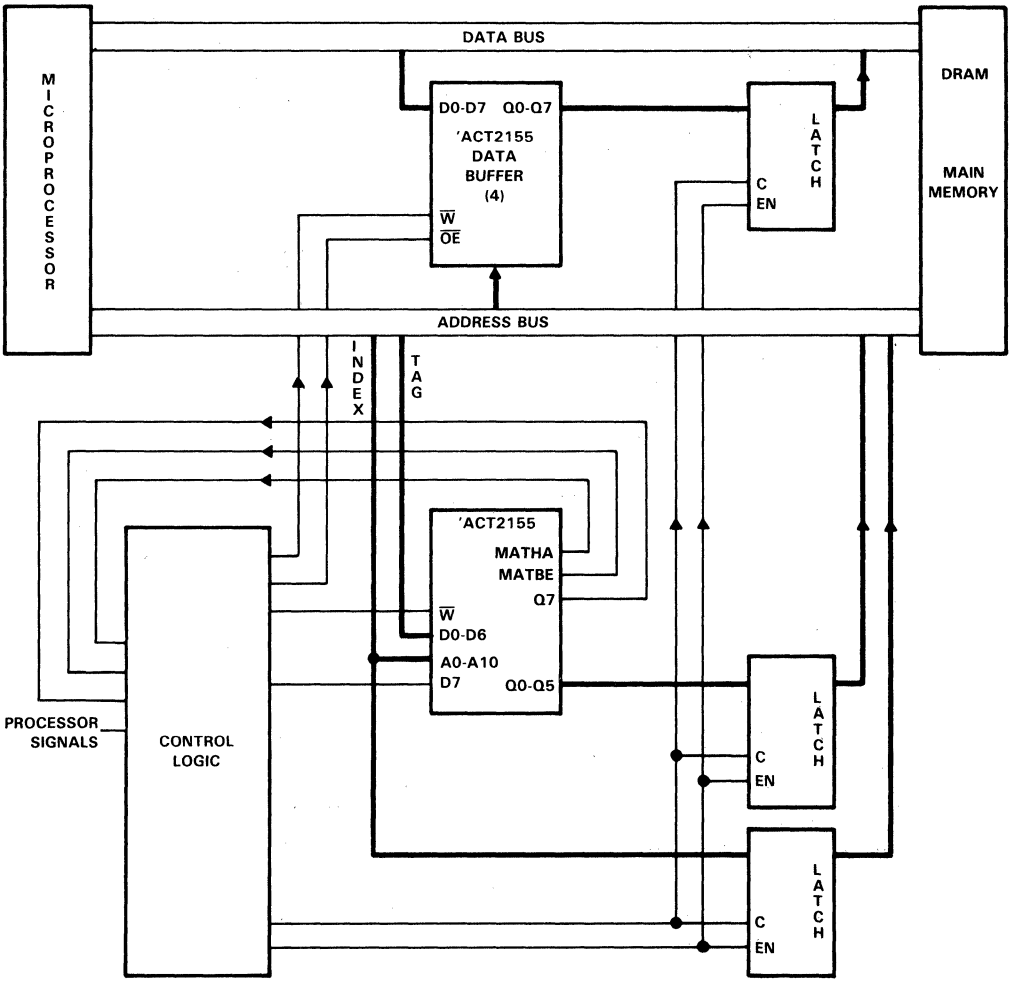


FIGURE 12. COPY-BACK USING THE 'ACT2155

APPLICATION INFORMATION

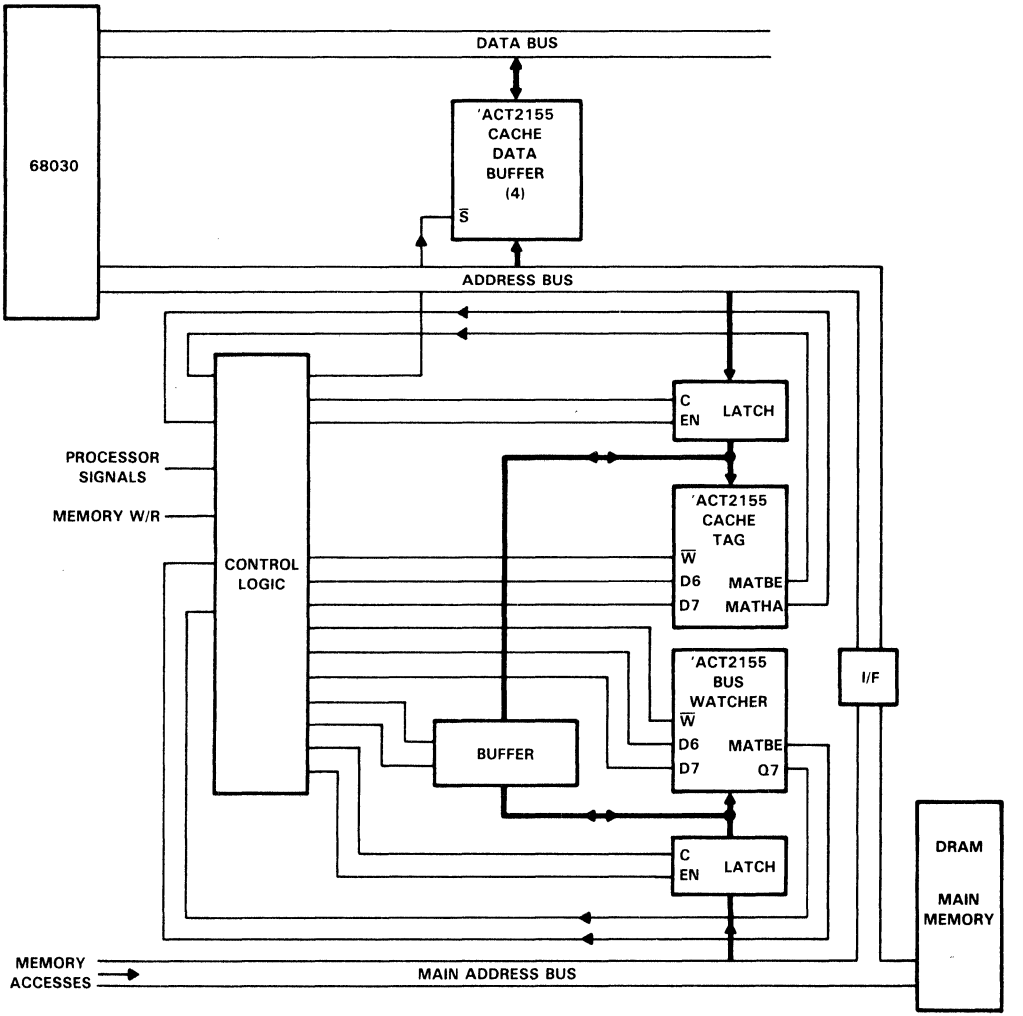
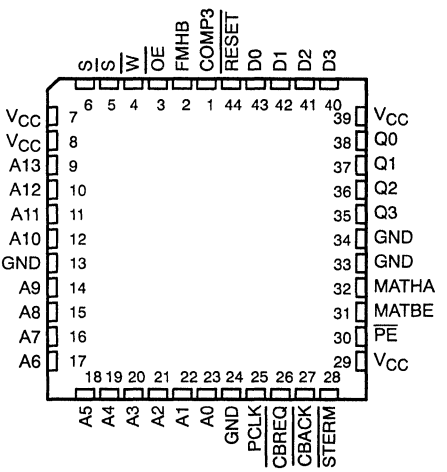


FIGURE 13. BUS WATCHING WITH THE SN74ACT2155

D3412, APRIL 1990–REVISED JUNE 1990

- **Address to MATCH Time . . . 20 ns Max**
- **Supports Motorola MC68030 Cache Burst Fill with Direct Interface**
- **Cache Data RAM with Parity and Internal Burst Counter**
- **Dirty Bit Storage Capability for Use in Copy-Back Caches**
- **Separate I/O Supports Copy-Back**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2156 burst cache address comparator/ data RAM consists of a high-speed 16K x 5 static RAM array, 2-bit burst counter and control circuitry, parity generator, parity checker, and 4-bit high-speed comparator. The 'ACT2156 is fabricated using advanced silicon gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2156 provides a valuable building block for building fast efficient caches. By combining this device with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

The 'ACT2156 was designed to be used as the tag comparator and data RAM necessary to provide a cache that supports the burst fill requirement of the Motorola MC68030 microprocessor. The 'ACT2156 directly interfaces with the MC68030 providing four long words to the processor in four clock cycles. By interfacing directly with the processor, about 10 ns in delay time is saved when comparing this solution with discrete designs. Even though the 'ACT2156 is designed for use with the MC68030 processor, it can also be used with other processors to implement write-through or copy-back class caches.

The SN74ACT2156 is characterized for operation from 0°C to 70°C.

operation as an address comparator

The 'ACT2156 compares the contents of the memory location addressed by A0-A13 with the address bits applied at D0-D3. An equality is indicated by a high level on the MATBE and MATHA outputs. A low-level output on $\overline{PE}$ signifies a parity error in the addressed internal RAM data. During a write cycle, address bits on D0-D3 plus generated odd parity are written in the 5-bit memory location addressed by A0-A13. Also during write, a parity error may be forced for diagnostic purposes by holding $\overline{PE}$ low.

operation in the burst mode

The 'ACT2156 contains burst control circuitry consisting of a 2-bit wrap-around counter, a mux, and a Burst Control Register (BCR). The BCR controls a mux which selects A0 and A1 from either the input terminals or the 2-bit counter. When $\overline{CBREQ}$ or $\overline{CBACK}$ is high, the BCR is asynchronously reset and inputs A0 and A1 drive the RAM. On the next falling edge of PCLK after $\overline{STERM}$ is taken low, the BCR is set and the counter bits (CA0

This device is covered by U.S. Patents 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

and CA1) drive the RAM. At the same time that the BCR is set ($\overline{STERM}$ low and a PCLK falling edge), the binary value of A0 and A1 in the counter is incremented. The counter can be held at any count by taking $\overline{STERM}$ high as long as BCR remains set. When the BCR is set, MATHA is forced high.

operation as a data RAM

The 'ACT2156 can be used as a 16K x 4 data RAM with separate I/O, a four-word burst mode and parity generation and checking. When using this device as a data RAM, the FMHB input should be tied high to prevent MATHA and MATBE from switching.

using the 'ACT2156 with the MC68030

The 'ACT2156 interfaces with the Motorola MC68030 through use of 'ACT2156 input signals, $\overline{STERM}$, $\overline{CBREQ}$, PCLK, and $\overline{CBACK}$, and output signals MATBE and MATHA. Match outputs MATBE and MATHA can be tied directly to processor inputs $\overline{BERR}$ and $\overline{HALT}$, respectively. As long as the requested information is in cache, the $\overline{BERR}$ and $\overline{HALT}$ signals remain high. When a miss occurs (MATBE and MATHA low), $\overline{BERR}$ and $\overline{HALT}$ are driven low simultaneously causing the bus cycle to be retried (rerun). A high level applied at the FMHB input forces MATBE and MATHA high to prevent continuous rerun.

The 'ACT2156 was designed to be used as the tag comparator and data RAM necessary to provide a cache that meets the Motorola MC68030 internal cache burst fill requirement by supplying four long words to the processor in four clock cycles. When the MC68030 requests a burst fill, a single address is supplied. If the requested information is in the external cache, the 'ACT2156 will indicate a hit. If $\overline{STERM}$ is low, address bits A1-A0 (A3-A2 from the processor) will be incremented on each PCLK falling edge and the MATBE output will indicate a hit or a miss. If a miss occurs, MATBE will drive $\overline{BERR}$ low causing the MC68030 to abort the burst cycle and to run with the data it received. MATHA is held high during a burst by the BCR. The timing diagram in Figure 9 shows burst mode operation.

The 'ACT2156 internal counter can also be used when writing tag and data into the cache, when the burst fill is done from main memory. When $\overline{STERM}$ is taken high (inserting processor wait states), the 2-bit counter is held at the present count. The counter will continue to increment on the first PCLK falling edge after $\overline{STERM}$ returns low. When $\overline{CBACK}$ or $\overline{CBREQ}$ returns high, the mux will select input pins A0 and A1 to drive the RAM. Figure 10 shows a MC68030 burst request with data in main memory. For more information on using the 'ACT2156 with the MC68030, see the *"SN74ACT2155/56 Cache Enhances MC68030 Processor Performance"* applications note.

cascading the 'ACT2156

The 'ACT2156 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A13 inputs of each device with the same index and applying the additional address bits to the D0-D3 inputs. The chip select inputs allow the 'ACT2156 to be cascaded in depth. When a device is deselected, the MATHA and MATBE outputs are driven high. It should be noted that a decoder can be used to drive the select inputs, since the propagation delay from select to match is much faster than from address to match. MATHA and MATBE are open-drain outputs for easy wired logic. Through the use of the chip select inputs, the 'ACT2156 can also be cascaded for a deeper cache data buffer. Figure 12 shows the 'ACT2156 cascaded.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 16K x 5 RAM locations are cleared to zero (with valid parity) and the MATHA and MATBE outputs are forced high. If a D0-D3 input of zero is compared to any memory location that has not been written into since reset, MATHA and MATBE will be high indicating that D0-D3, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed

memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit must be tied high regardless of the address width.

The burst control register (BCR) must be initialized after power-up by taking $\overline{\text{CBACK}}$ or $\overline{\text{CBREQ}}$ high. This ensures that the A0 and A1 inputs are driving the RAM and not the counter bits CA0 and CA1.

copy-back caches

The 'ACT2156 can be used in write-through cache designs where writes to cache are immediately sent to main memory, or in copy-back cache designs where a cache write initially only modifies the cache and can later be copied back to main memory. Copy-back caches have an advantage in that the number of writes to main memory are reduced thereby reducing bus traffic. To implement a copy-back cache, a dirty bit is needed that indicates whether or not the data is modified from that which is in main memory. The dirty bit is set to 1 when the cache data is modified. Data is only copied back if the dirty bit is set, otherwise, it is simply overwritten.

The COMP3 input of the 'ACT2156 allows bit D3 to be used as a dirty bit. By tying COMP3 low, bits D3 and Q3 are gated out of the comparator so the comparison is only done on D0-D2. With outputs Q0-Q3 enabled ($\overline{\text{OE}}$ low) the dirty bit, Q3, can be monitored at the same time as the match signals. If the dirty bit is set during a read or write miss, the tag and data can be stored in latches before writing the new tag and data into cache. Latched data and address can then be copied back to main memory. Figure 13 shows a typical copy-back application.

When implementing cache designs, the problem of cache coherency is always a concern. One solution to this problem is to implement bus watching using the 'ACT2156. By storing the same tags in the bus watcher RAM as is stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. If dirty data is being accessed, the good copy of that data can be copied from cache to main memory. Figure 14 shows a possible bus watcher implementation.

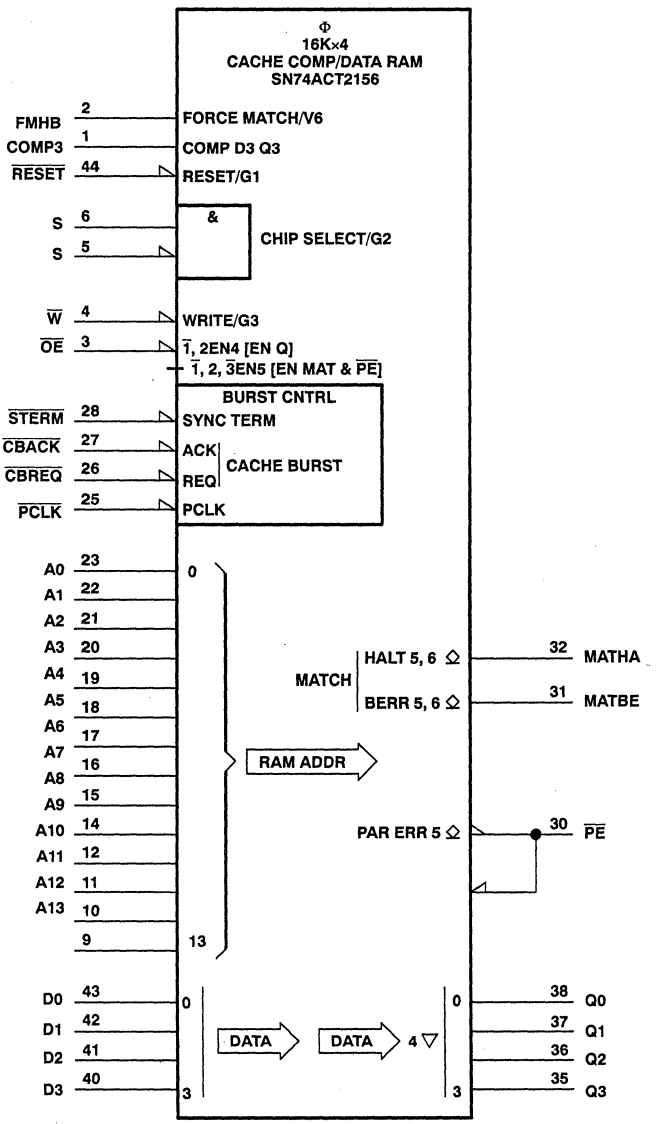
FUNCTION TABLE

INPUTS						OUTPUTS				FUNCTION
S	$\overline{S}$	W	$\overline{\text{RESET}}$	$\overline{\text{OE}}$	FMHB	MATHA†	MATBE	$\overline{\text{PE}}$ (I/O)	Q0–Q3	
X	X	X	X	X	H	H	H	‡	‡	Force MATHA and MATBE unconditionally high
X	H	X	X	X	X	H	H	Disabled	Hi–Z	Deselect. Inhibits write, read and compare
L	X	X	X	X	X	H	H	Disabled	Hi–Z	Deselect. Inhibits write, read and compare
H	L	H	H	X	L	H or L	H or L	L	‡	Parity error
						L	L	H		Not equal
						H	H	H		Equal
X	X	H	L	X	X	H	H	Disabled	Hi–Z	Memory reset unconditionally
H	L	L	H	H	X	H	H	Input	Hi–Z	Write. V_{IL} on $\overline{\text{PE}}$ forces bad parity
H	L	L	H	L	X	H	H	Input	Low	Write. V_{IL} on $\overline{\text{PE}}$ forces bad parity
H	L	H	H	L	X	‡	‡	Enabled	Enabled	Read

During burst mode, MATHA is forced high.

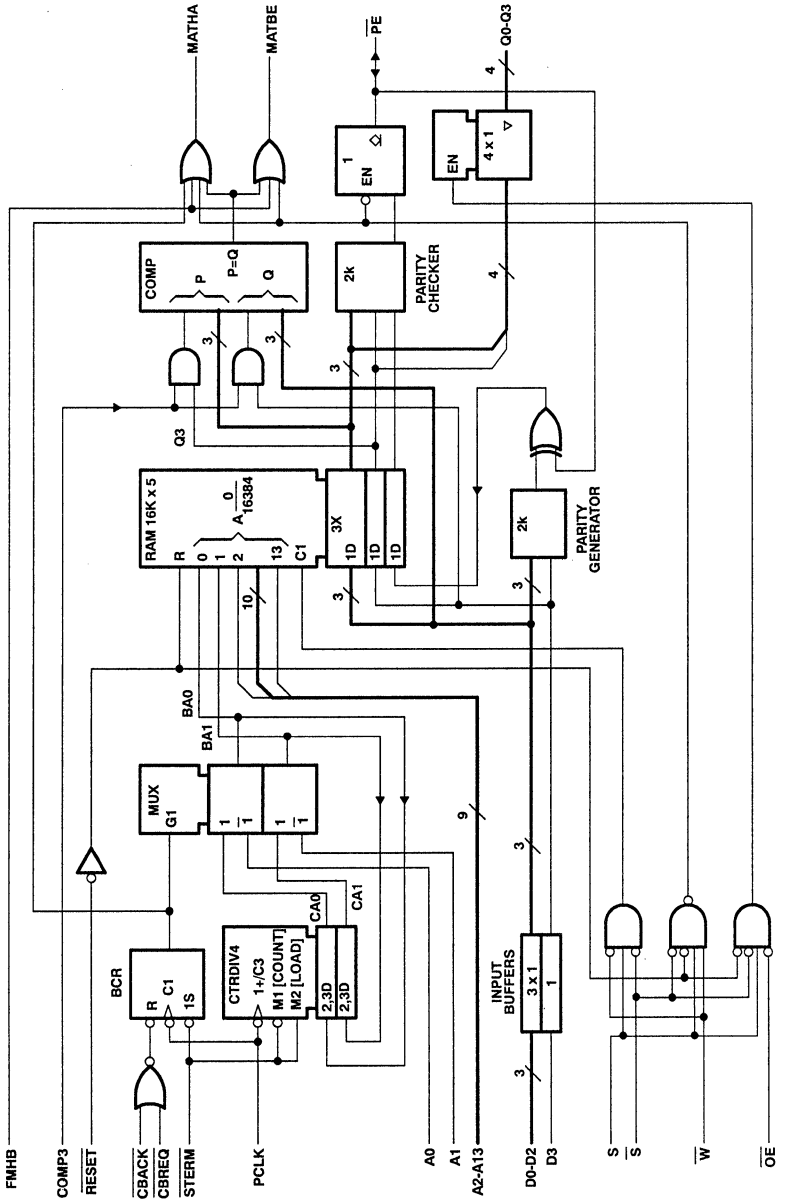
The state of these pins is dependent on inputs shown as don't care (X).

logic symbol†



This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



Terminal Functions

PIN NAME	DESCRIPTION
A0-A13	Address Inputs. Addresses a memory location in the 16K x 5 RAM. When in burst mode, address bits A0 and A1 are driven from the internal 2-bit counter independent of the A0 and A1 pins.
$\overline{\text{CBACK}}$	Cache Burst Acknowledge Input. When $\overline{\text{CBACK}}$ is high, the internal burst control register (BCR) is asynchronously reset to zero causing inputs A0 and A1 to drive the internal A0 and A1 address lines.
$\overline{\text{CBREQ}}$	Cache Burst Request Input. When $\overline{\text{CBREQ}}$ is high, the internal burst control register (BCR) is asynchronously reset to zero causing inputs A0 and A1 to drive the internal A0 and A1 address lines.
D0-D3	Data (Tag) Inputs. Provides input to RAM when selected and $\overline{\text{W}}$ is low. When $\overline{\text{W}}$ is high, the selected device compares D0-D3 to the addressed 4-bit memory location. Bit D3 along with stored bit Q3 can be removed from the comparison by taking the COMP3 pin low.
FMHB	Force Match Halt BERR Input. When this input is taken high, the MATBE and MATHA outputs are unconditionally forced high.
MATBE	Match BERR Output. During the compare mode, MATBE is high when D0-D3 (D0-D2 if COMP3 is low) equals Q0-Q3 (Q0-Q2 if COMP3 is low). MATBE is also high during deselect, write, reset, and when FMHB is high. Since MATBE is an open-drain output, an external pullup resistor of 180 Ω minimum is required. MATBE could be high in compare mode when a parity error exits.
MATHA	Match HALT Output. During the compare mode, MATHA is high when D0-D3 (D0-D2 if COMP3 is low) equals Q0-Q3 (Q0-Q2 if COMP3 is low). MATHA is also high during deselect, write, and reset, when FMHB is high, and when the burst control register (BCR) is set high. Since MATHA is an open-drain output, an external pullup resistor of 180 Ω minimum is required. MATHA could be high in compare mode when a parity error exits.
COMP3	COMP3 Input. When COMP3 is low, bits D3 and Q3 are taken out of the comparison allowing this bit to be used for a copy-back status bit (dirty bit). When COMP3 is high, D3 and Q3 are included in the comparison.
$\overline{\text{OE}}$	Output Enable Input. $\overline{\text{OE}}$ enables (low) or disables (high) Q0-Q3 when selected and $\overline{\text{RESET}}$ is high.
PCLK	Processor Clock Input. The burst control and counter registers are clocked by a high-to-low transition on the PCLK input.
$\overline{\text{PE}}$	Parity Error Output/Input. During compare cycles V_{OL} at $\overline{\text{PE}}$ indicates a parity error in the stored data. During write cycles, $\overline{\text{PE}}$ forces a parity error into the parity bit location specified by A0-A13 when $\overline{\text{PE}}$ is taken to V_{IL}. $\overline{\text{PE}}$ is an open-drain output, therefore, a pullup resistor, 180 Ω minimum, is required. PE is disabled during write, reset, and deselect.
Q0-Q3	Data Outputs. Q0-Q3 will display the contents of the addressed memory location when $\overline{\text{S}}$ and $\overline{\text{OE}}$ are low and S and $\overline{\text{RESET}}$ are high. Q0-Q3 is disabled during deselect, reset, and when $\overline{\text{OE}}$ is high.
$\overline{\text{RESET}}$	Reset Input. Asynchronously clears the 16K x 5 bit RAM array to zero with valid parity independent of the select inputs when $\overline{\text{RESET}}$ is low. By tying a single data input high, a false match will not occur when a D0-D3 input of zero is applied.
S, $\overline{\text{S}}$	Chip Select Inputs. Enables device when $\overline{\text{S}}$ is low and S is high. When $\overline{\text{S}}$ is high or S is low, MATBE and and MATHA are forced high and $\overline{\text{PE}}$ and Q0-Q3 are disabled.
$\overline{\text{STERM}}$	Synchronous Termination Input. On the next PCLK falling edge after $\overline{\text{STERM}}$ goes low (while $\overline{\text{CBACK}}$ and $\overline{\text{CBREQ}}$ are low), the 2-bit counter increments the binary value applied to the A0 and A1 inputs and the burst control register (BCR) is set high. A high level in the burst control register will cause the counter bits to drive the internal A0 and A1 address lines. The burst control register will remain high until $\overline{\text{CBREQ}}$ or $\overline{\text{CBACK}}$ goes high. Taking $\overline{\text{STERM}}$ high during a burst, holds the counter at the present count.
$\overline{\text{W}}$	Write Control Input. Writes D0-D3 and generated parity into the addressed memory location when the device is selected and $\overline{\text{W}}$ is low. When $\overline{\text{W}}$ is low, MATBE and MATHA are forced high and $\overline{\text{PE}}$ is disabled.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... — 1.5 V to 7 V
Input voltage range, any input ..... — 1.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Output diode current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}): D0-D8 ..... ± 25 mA
MATCH, $\overline{PE}$ ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		– 0.5		0.8	V
V_{OH}	High-level output voltage, MATBE, MATHA and $\overline{PE}$ outputs				5.25	V
I_{OH}	High-level output current, Q0–Q3				–8	mA
I_{OL}	Low-level output current	Q0-Q3			8	mA
		MATBE, MATHA, and $\overline{PE}$			27	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the threshold region of the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with – 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.75 V,	I_{OH} = – 8 mA	3.7			V
V_{OL}	Low-level output voltage	MATBE, MATHA or $\overline{PE}$	V_{CC} = 4.75 V,	I_{OL} = 27 mA			0.4	V
		Q0-Q3	V_{CC} = 4.75 V,	I_{OL} = 8 mA			0.4	
I_{OH}	High-level output current	MATBE, MATHA or $\overline{PE}$	V_{CC} = 5.25 V,	V_{OH} = 5.25 V			10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V, $\overline{OE}$ at V_{IH}	V_O = 0 – V_{CC},			±10	μA
I_I	Input current		V_{CC} = 5.25 V,	V_I = 0 – V_{CC}			± 5	mA
I_{CC1}	Supply current (operative)		V_{CC} = 5.25 V, $\overline{S}$ at 0 V,	$\overline{RESET}$ at V_{CC}, S at V_{CC}		115	180	mA
I_{CC2}	Supply current (resest)		V_{CC} = 5.25 V, $\overline{S}$ at 0 V,	$\overline{RESET}$ at 0 V, S at V_{CC}		55	100	mA
I_{CC3}	Supply current (deselect)		V_{CC} = 5.25 V, $\overline{S}$ at V_{CC},	$\overline{RESET}$ at V_{CC}, S at 0 V		100	150	mA
C_i	Input capacitance		f = 1 MHz				5	pF
C_o	Output capacitance		f = 1 MHz				6	pF

All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

	PARAMETER	SN74ACT2156-20			UNIT
		MIN	TYP‡	MAX	
t_{pd1}	Propagation time, address to Q0-Q3		15	23	ns
t_{pd2}	Propagation time, address to $\overline{PE}$ low		14	22	ns
t_{pd3}	Propagation time, $\overline{S}$ low or S high to MATBE and MATHA low		7	13	ns
t_{pd4}	Propagation time, address to $\overline{PE}$ high		14	25	ns
t_{pd5}	Propagation time, $\overline{S}$ high or S low to $\overline{PE}$ high		8	15	ns
t_{pd6}	Propagation time, address to MATBE and MATHA		14	20	ns
t_{pd7}	Propagation time, D0-D3 to MATBE and MATHA		11	15	ns
t_{pd8}	Propagation time, $\overline{S}$ high or S low to MATBE and MATHA high		7	13	ns
t_{pd9}	Propagation time, $\overline{S}$ low or S high to $\overline{PE}$ low		10	16	ns
t_{pd10}	Propagation time, PCLK↓ to MATBE		14	20	ns
t_{pd11}	Propagation time, PCLK↓ to MATHA high		14	20	ns
t_{pd12}	Propagation time, PCLK↓ to Q0–Q3		14	23	ns
t_{pd13}	Propagation time, PCLK↓ to $\overline{PE}$ low		11	20	ns
t_{pd14}	Propagation time, PCLK↓ to $\overline{PE}$ high		15	22	ns
t_{pd15}	Propagation time, $\overline{W}$ low to Q0-Q3 low		9	16	ns
t_{pd16}	Propagation time, $\overline{W}$ high to Q0-Q3		9	16	ns
t_{pd17}	Propagation time, $\overline{W}$ low to MATBE and MATHA high		10	14	ns
t_{pd18}	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		9	12	ns
t_{pd19}	Propagation time, $\overline{RESET}$ low to MATBE and MATHA high		9	15	ns
t_{pd20}	Propagation time, FMHB to MATBE and MATHA		7	12	ns
t_{en1}	Enable time, $\overline{OE}$ low to Q0-Q3		5	12	ns
t_{en2}	Enable time, $\overline{S}$ low or S high to Q0-Q3		9	15	ns
t_{en3}	Enable time, $\overline{RESET}$ high to Q0-Q3 low		14	20	ns
t_{dis1}	Disable time, $\overline{S}$ high or S low to Q0-Q3		5	12	ns
t_{dis2}	Disable time, $\overline{OE}$ high to Q0-Q3		5	12	ns
t_{dis3}	Disable time, $\overline{RESET}$ low to Q0-Q3		8	15	ns
t_{v1}	Valid time, MATBE and MATHA after change of data	2			ns
t_{v2}	Valid time, MATBE and MATHA after change of address	2			ns
t_{v3}	Valid time, MATBE and MATHA low after $\overline{S}$ high or S low	2			ns
t_{v4}	Valid time, $\overline{PE}$ after change of address	2			ns
t_{v5}	Valid time, $\overline{PE}$ low after $\overline{S}$ high or S low	2			ns
t_{v6}	Valid time, MATBE after PCLK↓	4			ns
t_{v7}	Valid time, MATHA after $\overline{CBREQ}$ or $\overline{CBACK}$ high	4			ns
t_{v8}	Valid time, MATHA after PCLK↓	5			ns
t_{v9}	Valid time, Q0-Q3 after PCLK↓	5			ns
t_{v10}	Valid time, $\overline{PE}$ after PCLK↓	3			ns
t_{v11}	Valid time, Q0-Q7 after address	2			ns
t_{v12}	Valid time, Q0-Q7 after $\overline{CBREQ}$ or $\overline{CBACK}$ high	2			ns

See Parameter Measurement Information for load circuit and voltage waveforms.
All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

	PARAMETER	SN74ACT2156-20			UNIT
		MIN	TYP‡	MAX	
t_{w1}	Pulse duration, $\overline{W}$ low without writing $\overline{PE}$	12			ns
t_{w2}	Pulse duration, $\overline{W}$ low writing $\overline{PE}$ (see Note 3)	20			ns
t_{w3}	Pulse duration, $\overline{RESET}$ low	60			ns
t_{w4}	Pulse duration, PCLK high or low	10			ns
t_{su1}	Inactive-state setup time, $\overline{CBREQ}$ before PCLK↓	3			ns
t_{su2}	Inactive-state setup time, $\overline{CBACK}$ before PCLK↓	3			ns
t_{su3}	Setup time, $\overline{STERM}$ setup time before PCLK↓	5			ns
t_{su4}	Setup time, Address valid before write enable high	12			ns
t_{su5}	Setup time, $\overline{S}$ low or S high before $\overline{W}$ high	10			ns
t_{su6}	Setup time, Address before $\overline{W}$ low	0			ns
t_{su7}	Setup time, D0-D3 before $\overline{W}$ high	10			ns
t_{su8}	Setup time, $\overline{PE}$ before $\overline{W}$ high (see Note 3)	8			ns
t_{su9}	Inactive-state setup time, $\overline{RESET}$ before $\overline{W}$ high	15			ns
t_{su10}	Setup time, A0-A1 before PCLK↓	6			ns
t_{su11}	Setup time, $\overline{W}$ high before PCLK↓	−1			ns
t_{h1}	$\overline{STERM}$ hold time after PCLK↓	3			ns
t_{h2}	Hold time, Address after $\overline{W}$ high	3			ns
t_{h3}	Hold time, $\overline{S}$ low or S high after $\overline{W}$ high	0			ns
t_{h4}	Hold time, D0-D3 after $\overline{W}$ high	3			ns
t_{h5}	Hold time, $\overline{PE}$ after $\overline{W}$ high	3			ns
t_{h6}	Hold time, Address after PCLK↓	2			ns
t_{h7}	Hold time, D0-D3 after $\overline{W}$ low (see Note 4)	10			ns

See Parameter Measurement Information for load circuit and voltage waveforms.

All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. The pulse duration requirement (t_{w2}) is only necessary when a parity error exists. A parity error exists when the $\overline{PE}$ output is low prior to writing data with correct parity (i.e., with the $\overline{PE}$ input high during write). The setup time (t_{su8}) aplies only during the write cycle timing when writing a parity error.

4. t_{h7} assures that when $\overline{W}$ is taken low during a compare cycle with MATBE and MATHA high that match will remain high without a glitch low. (As shown in the function table, $\overline{W}$ low forces MATBE and MATHA high).

PARAMETER MEASUREMENT INFORMATION

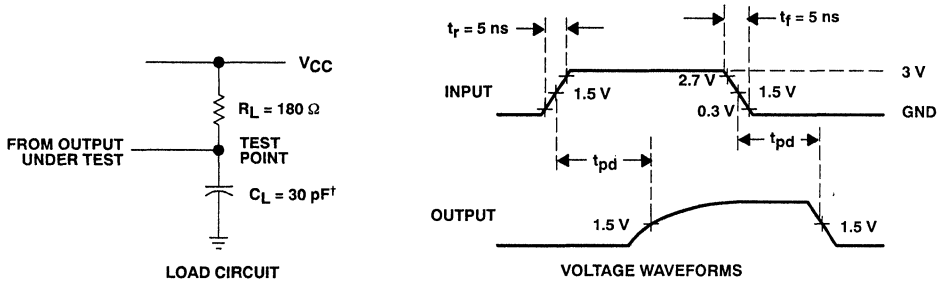


FIGURE 1. OPEN-DRAIN OUTPUTS

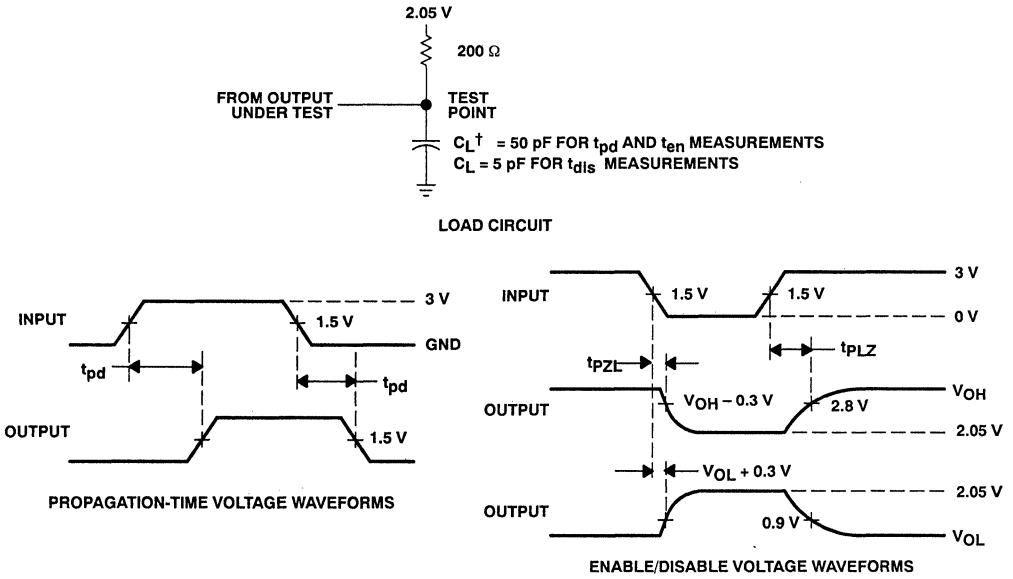


FIGURE 2. ALL OTHER OUTPUTS

C_L includes probe and test fixture capacitance.

PARAMETER MEASUREMENT INFORMATION

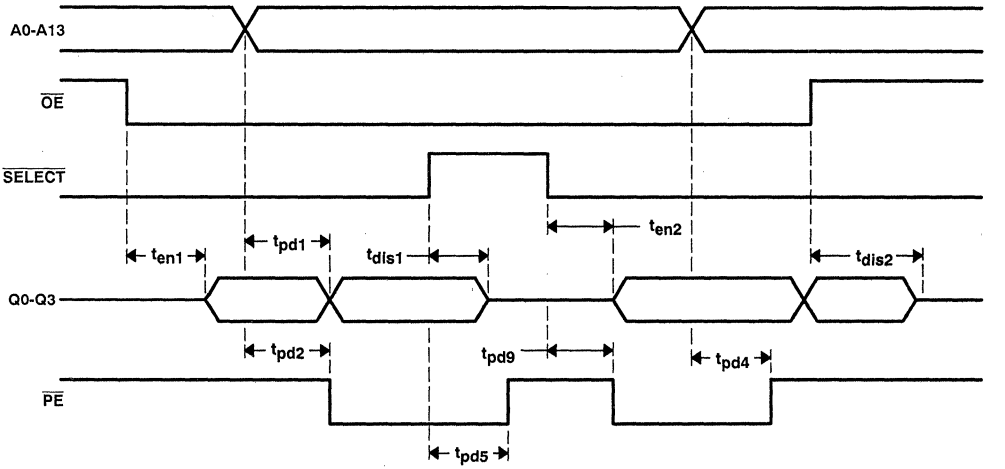


FIGURE 3. READ CYCLE TIMING

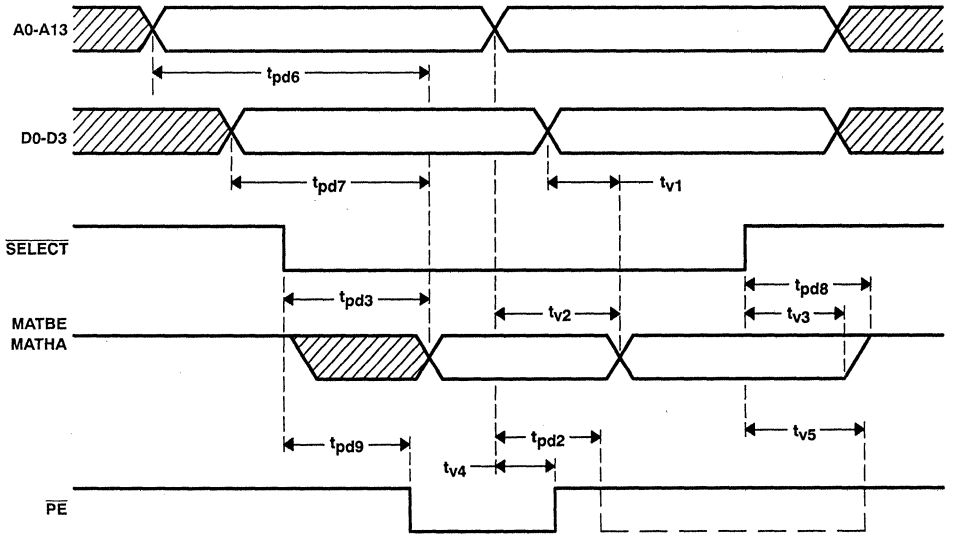


FIGURE 4. COMPARE CYCLE TIMING (WITHOUT BURST REQUEST)

PARAMETER MEASUREMENT INFORMATION

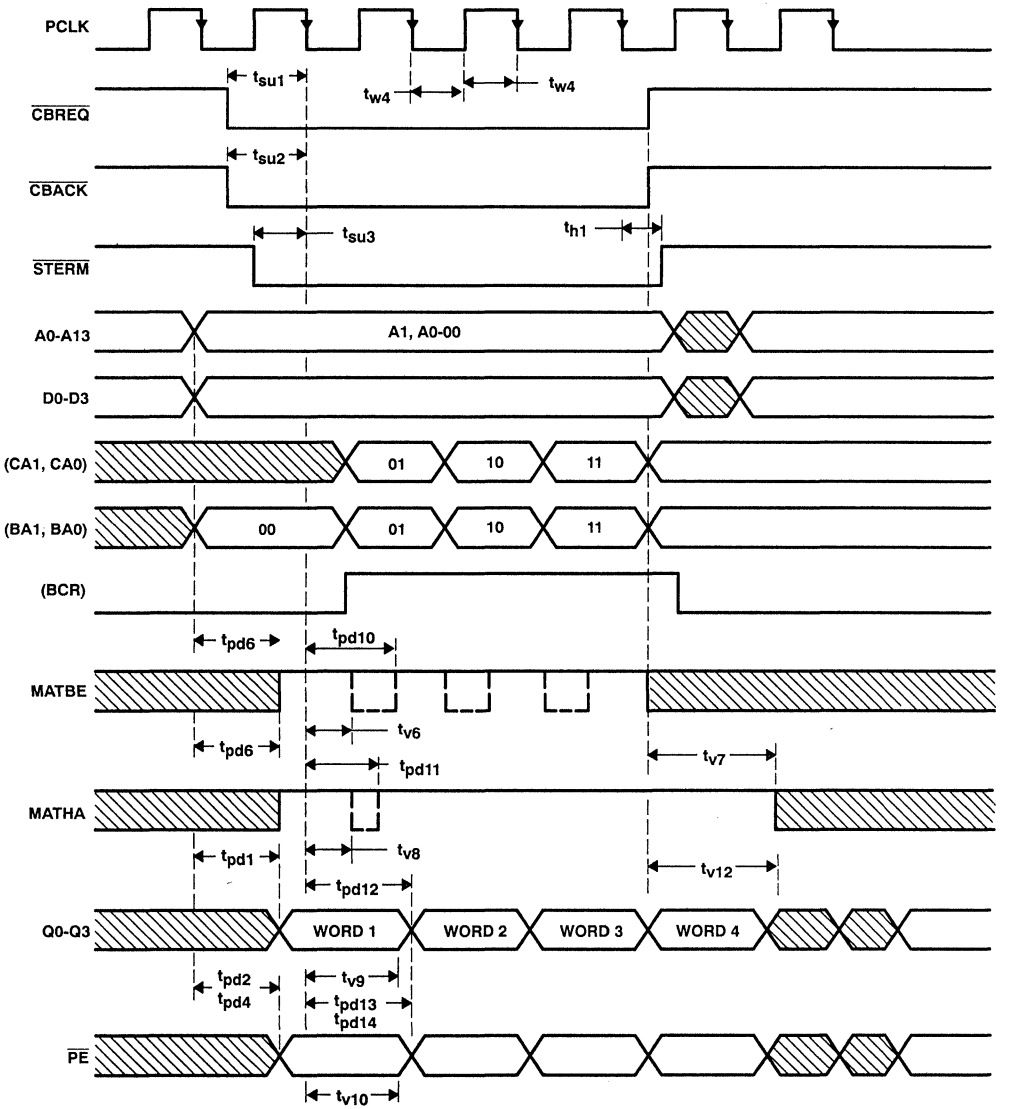


FIGURE 5. BURST COMPARE AND READ CYCLE ($\overline{OE}$ LOW)

PAREMETER MEASUREMENT INFORMATION

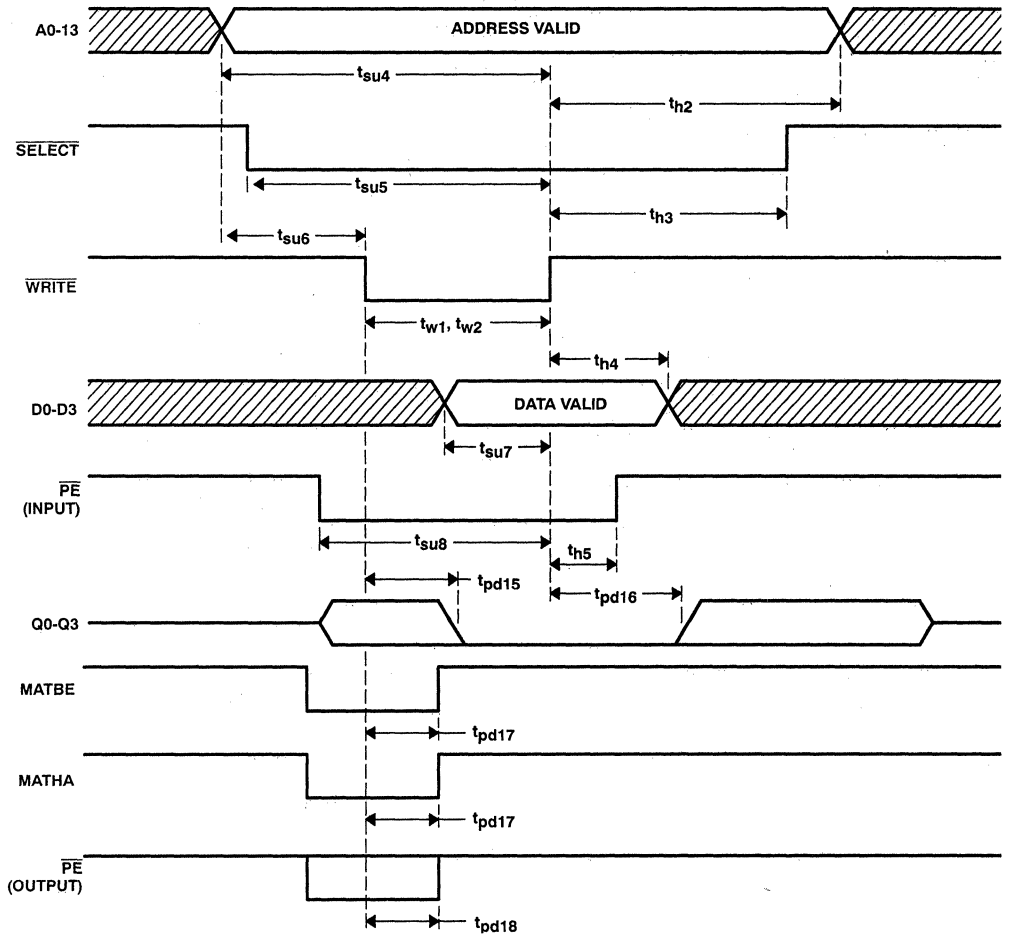


FIGURE 6. WRITE CYCLE TIMING ($\overline{OE}$ LOW)

PARAMETER MEASUREMENT INFORMATION

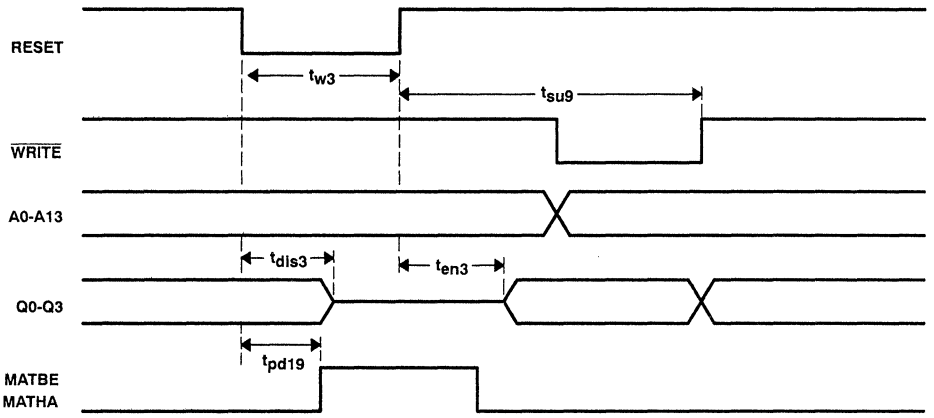


FIGURE 7. RESET CYCLE TIMING ($\overline{OE}$ LOW)

PARAMETER MEASUREMENT INFORMATION

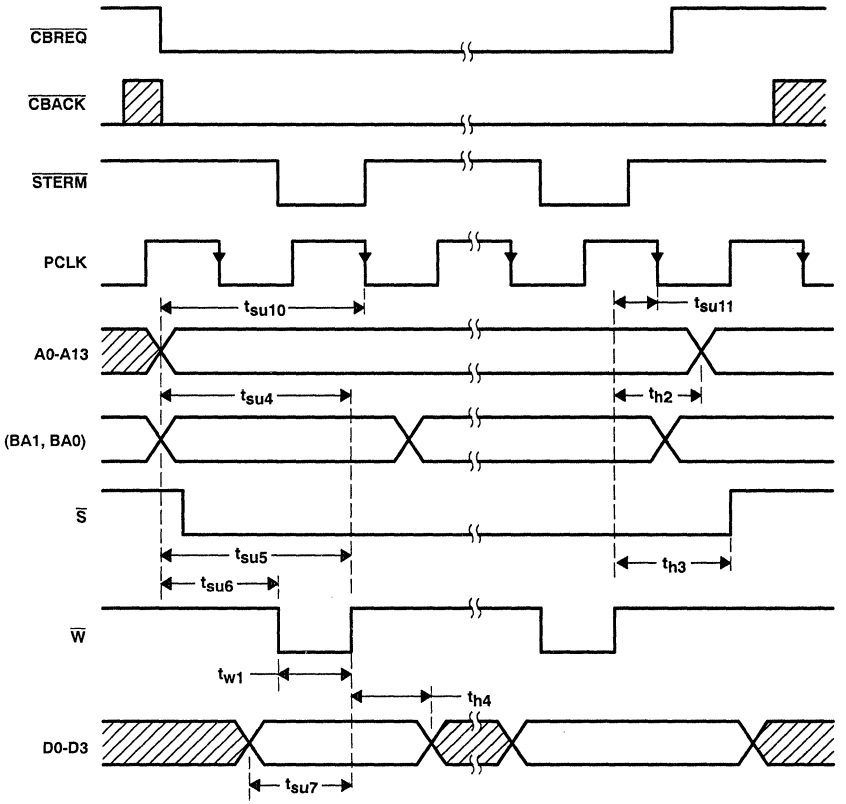


FIGURE 8. BURST MODE WRITE CYCLE TIMING

APPLICATION INFORMATION

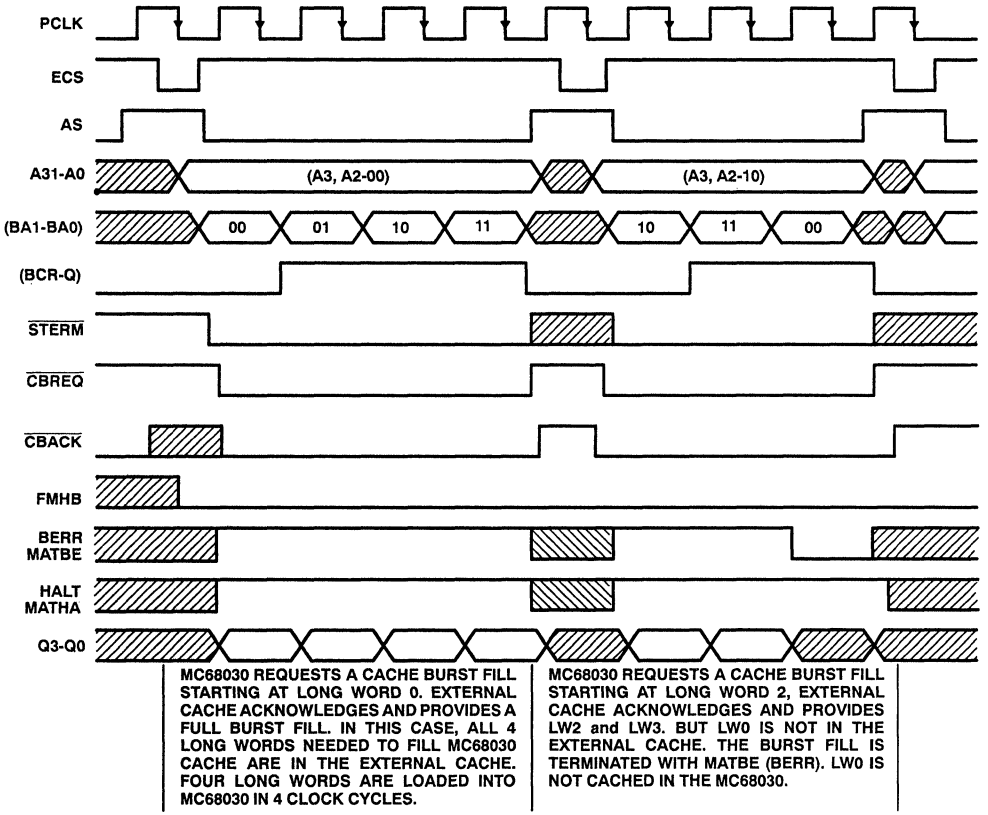


FIGURE 9. MC68030 BURST REQUEST WITH DATA IN EXTERNAL CACHE ($\overline{OE}$ LOW

APPLICATION INFORMATION

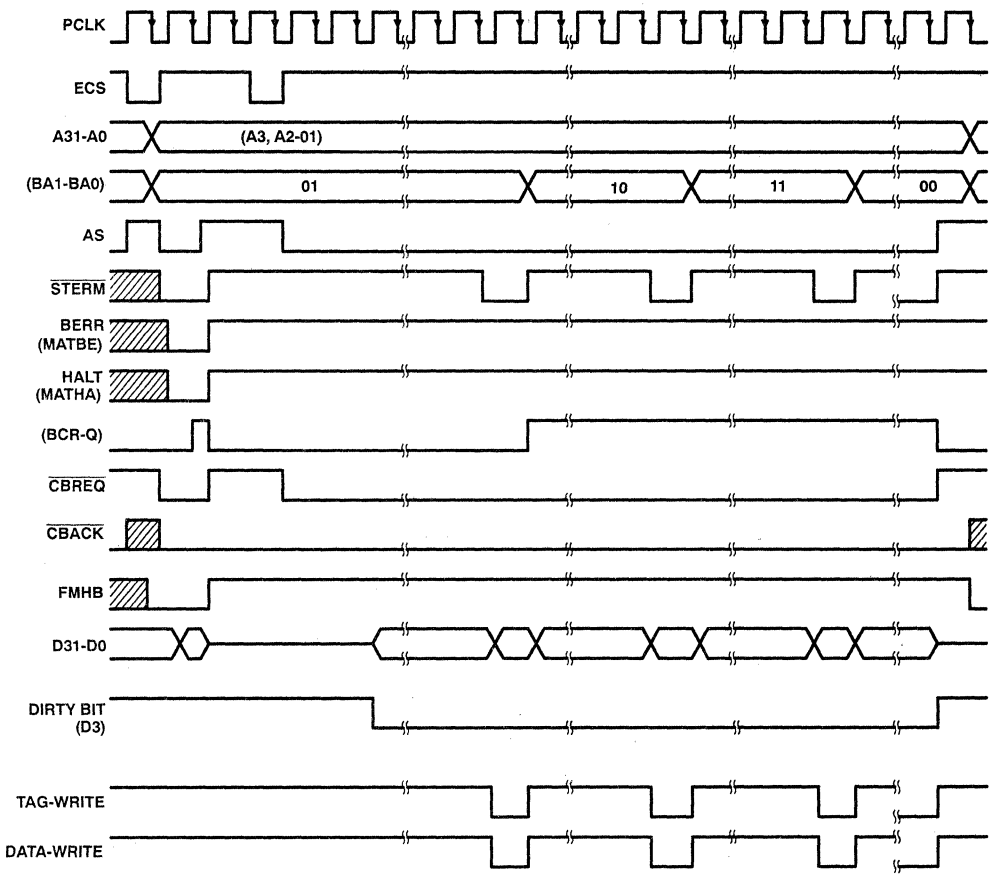


FIGURE 10. MC68030 BURST REQUEST WITH DATA IN MAIN MEMORY

APPLICATION INFORMATION

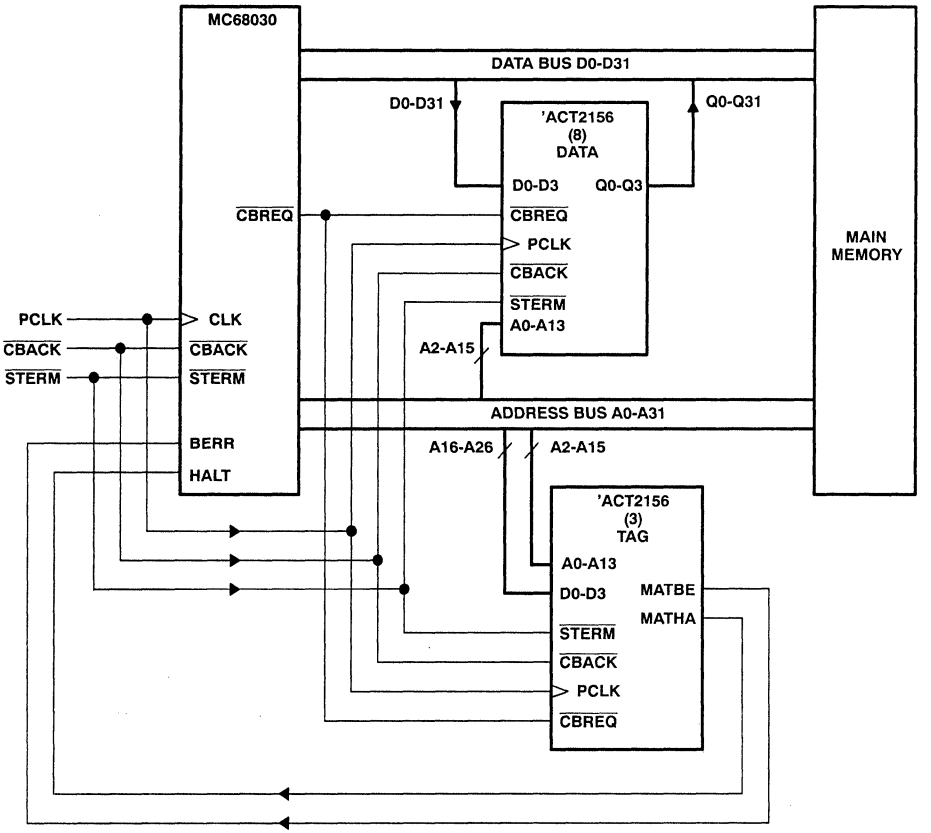


FIGURE 11. SN74ACT2156/MC68030 INTERFACE

APPLICATION INFORMATION

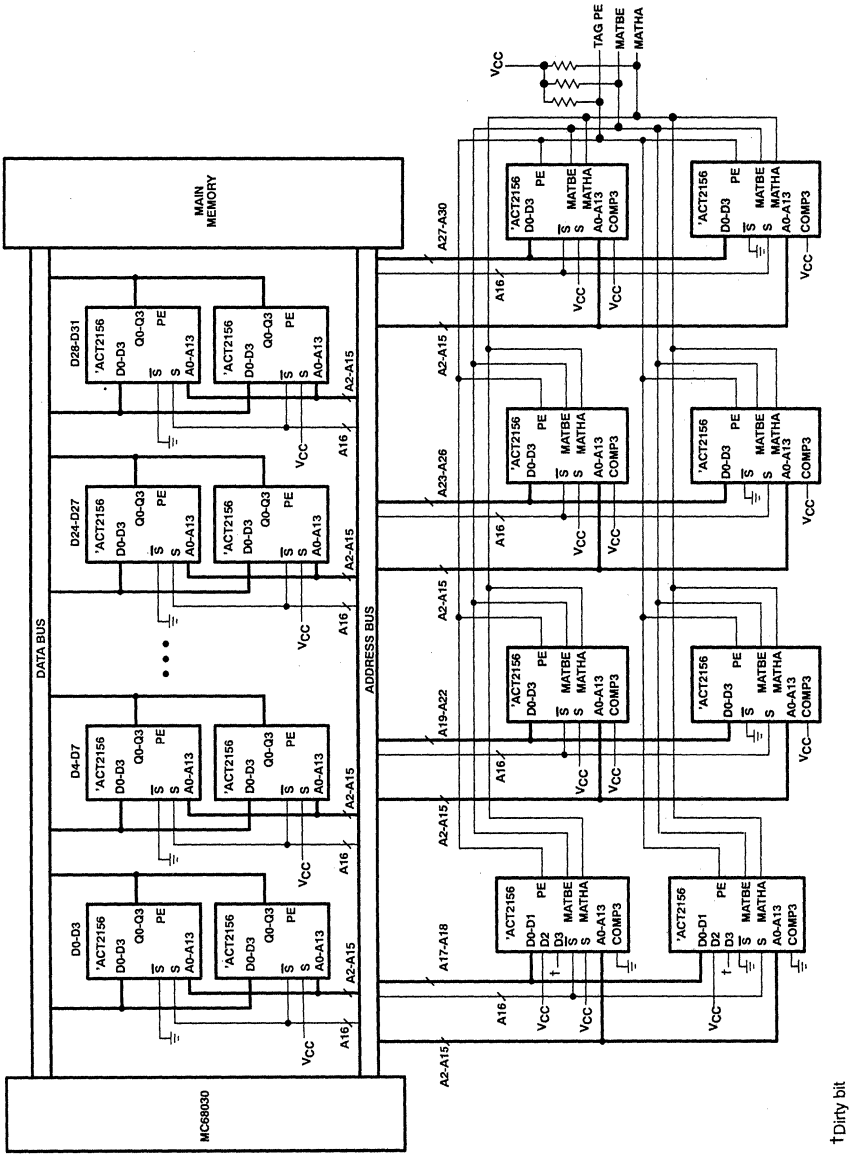


FIGURE 12. CASCADING THE 'ACT2156

APPLICATION INFORMATION

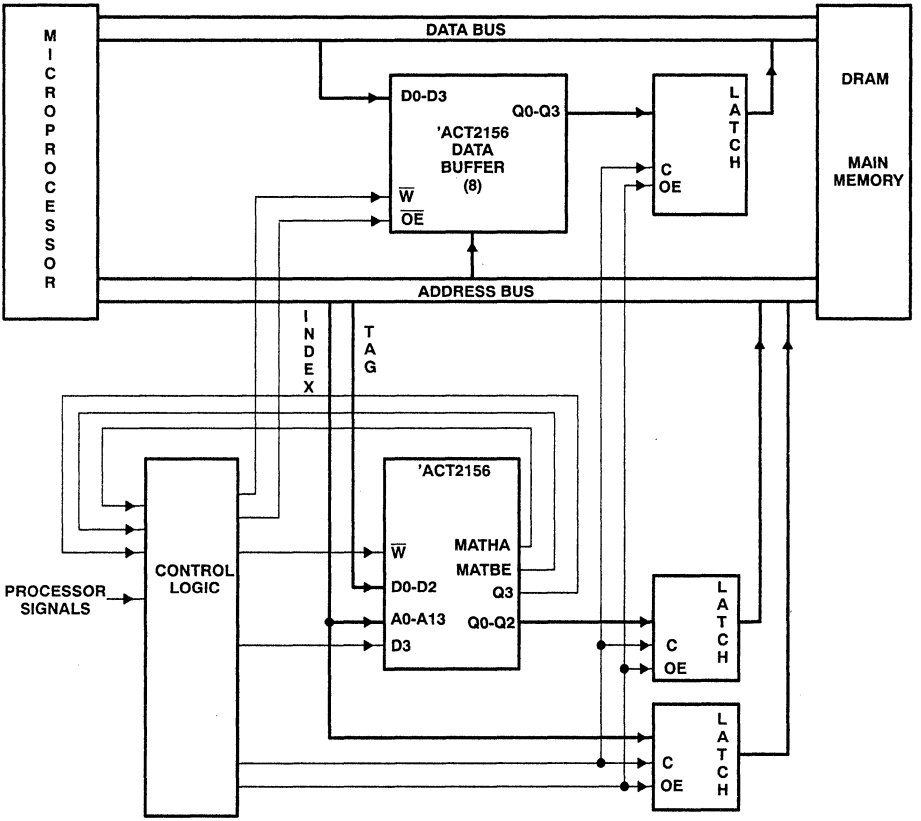


FIGURE 13. COPY-BACK USING THE 'ACT2156

APPLICATION INFORMATION

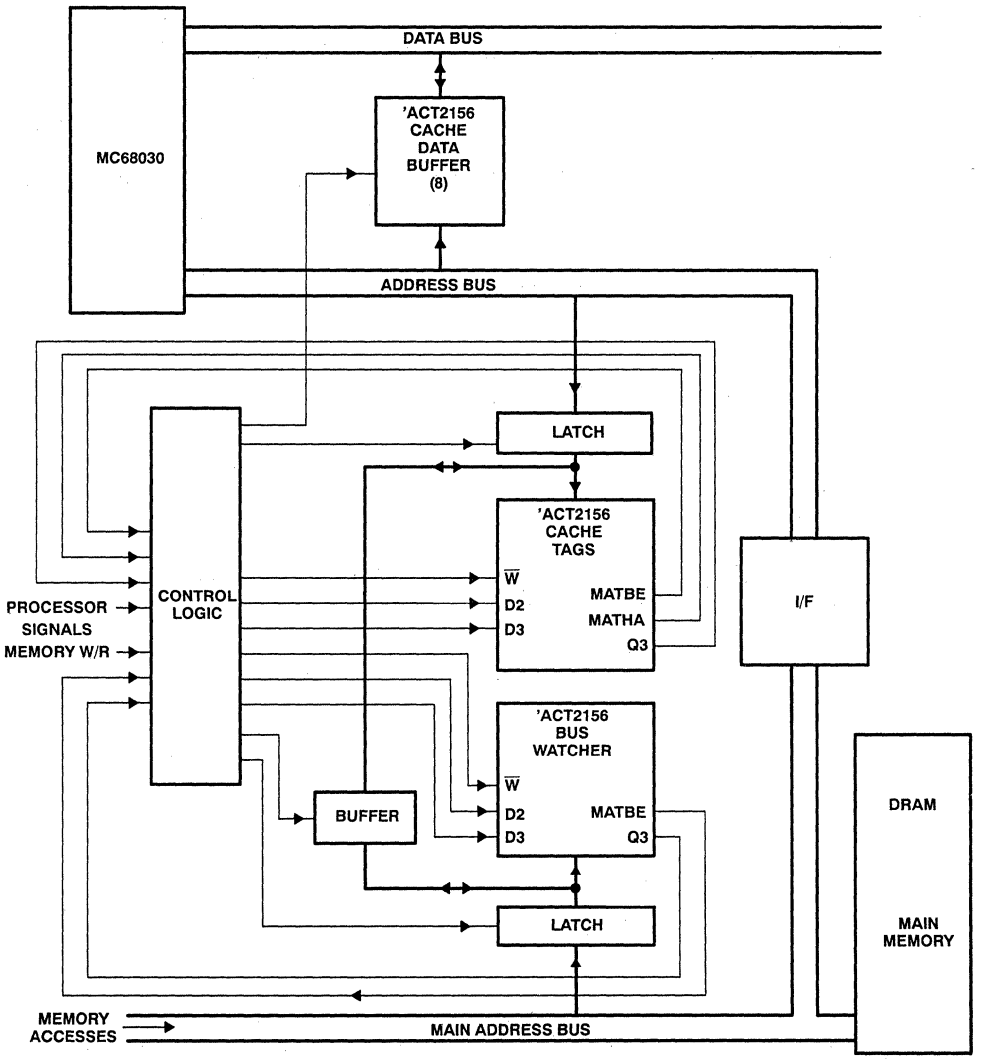
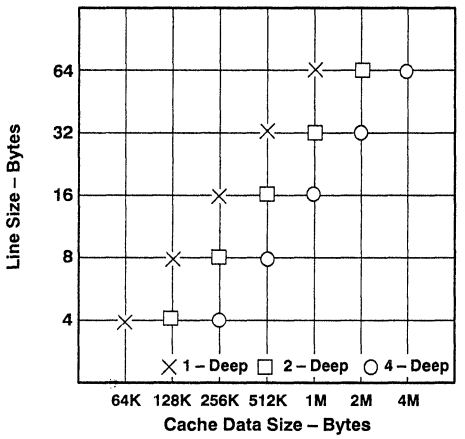


FIGURE 14. BUS WATCHING WITH THE 'ACT2156

APPLICATION INFORMATION

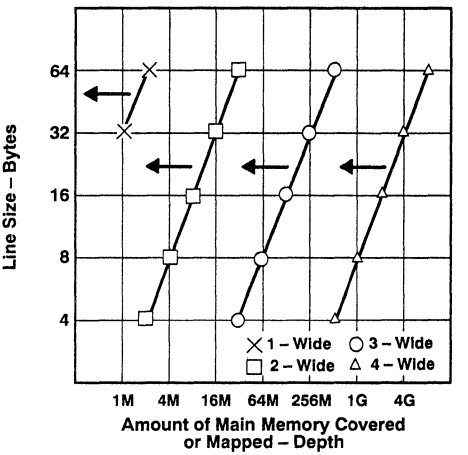
DEPTH CASCADING
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†



† Direct-mapped caches

FIGURE 15

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE‡



‡ One tag/line. Assumes a word length of 32 bits.

FIGURE 16

depth cascading

For two-way caches, each solution shown in Figure 15 is moved to the right one increment doubling the cache size and the number of devices used. Four-way cache designs using the 'ACT2156 will quadruple each solution shown.

width cascading

Memory coverage assumes one bit used as a valid bit (see Figure 16). Each solution for a given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth memory coverage increases, i.e., two deep — twice as much memory. For copy-back caches, each solution shown in Figure 16 must be moved one increment to the left (one tag bit is used as a dirty bit).

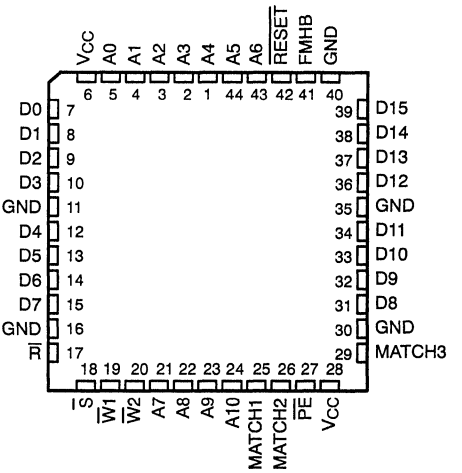
usage explanation and example

Figures 15 and 16 provide a quick means for determining if the 'ACT2156 will provide a good solution and the number of devices needed for implementation. For example, a design requires 256K bytes of cache, memory coverage of 256M, and a line size of 16 bytes (a 16-byte line size means each tag location maps four 32-bit words of cached data). From Figure 15, it is determined that one 'ACT2156 deep will provide a 256K byte cache with a 16-byte line size. From Figure 16, it is determined that four 'ACT2156s cascaded in width will map 256M of memory (or as much as 2G). Therefore, one deep by four wide (four 'ACT2156s) are needed to meet the design's requirements.

D3326, JANUARY 1990–REVISED JUNE 1990

- **Fast Address to Match Delay . . . 20 ns Max**
- **Totem-Pole and Open-Drain Match Outputs**
- **On-Chip Address/Data Comparator**
- **On-Chip Parity Generation and Checking**
- **Direct 68030 Interface**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2157 cache address comparator consists of a high-speed 2K x 18 static RAM array, parity generators, parity checkers, and 18-bit high-speed comparator. It is fabricated using advanced silicon-gate CMOS technology for high-speed and simple interface with bipolar TTL circuits. This cache address comparator is easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}1$, $\overline{W}2$, and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A10 with the applied D0-D15 plus generated byte parity. An equality is indicated by a high level on the MATCH1, MATCH2, and MATCH3 outputs.

The 'ACT2157 is provided with two write inputs, $\overline{W}1$ and $\overline{W}2$. When $\overline{S}$ is low, bytes D0-D7 are written into the addressed location by asserting $\overline{W}1$ (low) and bytes D8-D15 are written by asserting $\overline{W}2$ (low). By asserting both $\overline{W}1$ and $\overline{W}2$ at the same time, D0-D15 is written into the addressed memory location. During a write cycle, parity is generated and stored for each byte written.

'ACT2157 parity protection

Byte parity protection is included in the 'ACT2157 to provide a highly reliable cache directory. For any memory location addressed by A0-A10, $\overline{PE}$ will be low if a parity error occurs in either D0-D7 or D8-D15. $\overline{PE}$ is an open-drain output for easy OR-tying. For test purposes, a parity error can be forced in byte D0-D7 or D8-D15 by forcing $\overline{PE}$ low when $\overline{W}1$ or $\overline{W}2$ are low, respectively. A parity error is forced in both bytes by forcing $\overline{PE}$ low when both $\overline{W}1$ and $\overline{W}2$ are asserted.

reading the data RAM

A read mode is provided with the 'ACT2157 and allows the contents of RAM to be read at the D0-D15 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}1$ and $\overline{W}2$ are high. When using the 'ACT2157 as a data RAM, the FMHB input should be tied high to provide better noise immunity.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 2K x 18 RAM locations are cleared to zero (with valid parity) and the match outputs are forced high. If an input at D0-D15 of zero is compared to any memory location that has not been written into since reset, MATCH1, MATCH2, and MATCH3 will be high

indicating that D0-D15 plus generated parity is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only, one bit needs to be tied high regardless of the address width.

cascading the 'ACT2157

The 'ACT2157 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A10 inputs of each device with the same index and applying the additional address bits to the D0-D15 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, the match outputs are driven high. It should be noted that a fast decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire tying. Figure 11 shows the 'ACT2157 cascaded.

cache coherency through bus watching

When implementing cache designs, the problem of cache coherency is usually a concern. One solution to this problem is to implement bus watching using the 'ACT2157. By storing the same tags in the bus watcher RAM as is stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If cached data is being modified in main memory, the index can be passed to the cache tag and bus watcher RAM for invalidation. Figure 12 shows a typical bus watcher implementation.

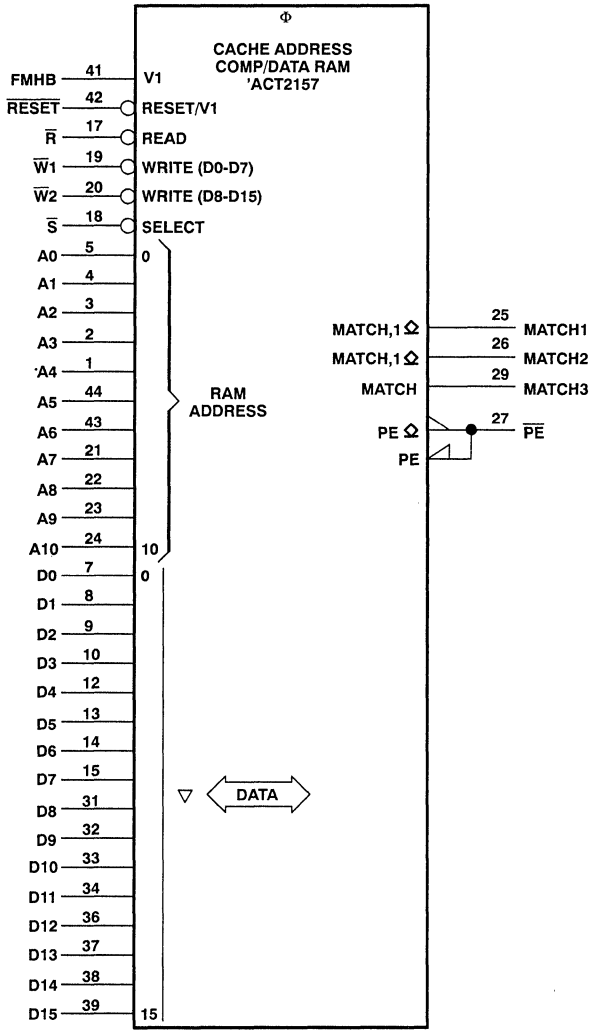
using the 'ACT2157 with the MC68030

The 'ACT2157 has two open-drain match outputs for direct interface with the Motorola MC68030. By tying the outputs MATCH1 and MATCH2 directly to MC68030 inputs BERR and HALT, a two-cycle synchronous read may be easily achieved. A two-cycle access can be accomplished by using control logic that assumes a cache hit will occur every time an access is started for cacheable data. This is accomplished by asserting the MC68030 input signal STERM at the beginning of the access cycle. As long as the requested information is in cache, the BERR and HALT signals remain high. When a miss occurs (MATCH1 and MATCH2 low), BERR and HALT are driven low simultaneously causing the bus cycle to be retried (rerun). The FMHB input of the 'ACT2157 is provided so that MATCH1 and MATCH2 can be forced high. This function is used to prevent continuous rerun when the processor retries an access. FMHB could also be used during noncacheable accesses (see Figure 13).

copy-back caches

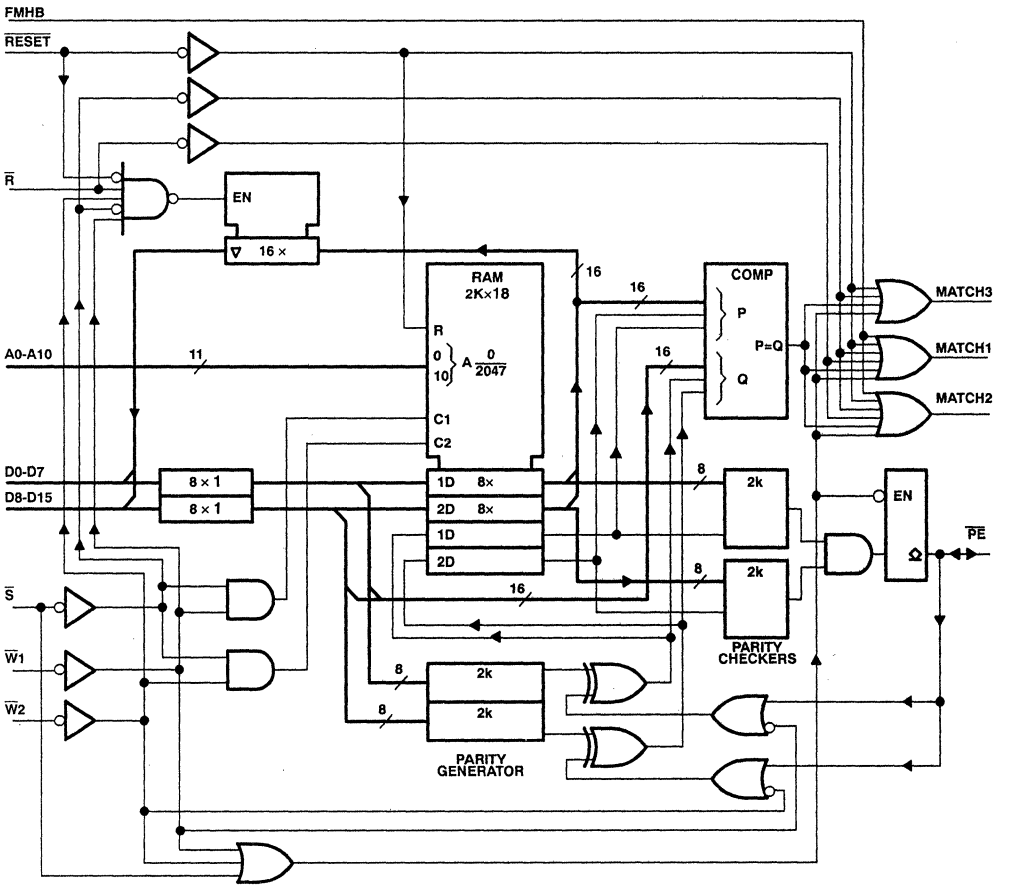
The 'ACT2157 can be used in write-through cache designs where writes to cache are immediately sent to main memory, or in copy-back cache designs where a cache write initially only modifies the cache and can later be copied back to main memory. Copy-back caches have an advantage in that the number of writes to main memory are reduced, thereby reducing bus traffic. To implement a copy-back cache, a dirty bit is needed that indicates whether or not the data is modified from that in main memory. The dirty bit is set to 1 when the cache data is modified. Data is only copied back if the dirty bit is set, otherwise it is simply overwritten. The read feature of the 'ACT2157 allows it to be used in copy-back cache designs. It should be noted, however, that the dirty bit must be stored in an external RAM. Figure 14 shows the 'ACT2157 in a copy-back application.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



FUNCTION TABLE

INPUT						I/O	OUTPUTS				FUNCTION
$\overline{W1}$	$\overline{W2}$	$\overline{R}$	$\overline{S}$	$\overline{RESET}$	FMHB	D0-D15	MATCH1	MATCH2	MATCH3	$\overline{PE}$	
L	H	X	L	H	X	Input	H	H	H	Input	Write D0-D7, low on $\overline{PE}$ forces parity error
H	L	X	L	H	X	Input	H	H	H	Input	Write D8-D15, low on $\overline{PE}$ forces parity error
L	L	X	L	H	X	Input	H	H	H	Input	Write D0-D15, low on $\overline{PE}$ forces parity errors
H	H	L	L	H	X	Output	H	H	H	H	Read
H	H	L	L	H	X	Output	H	H	L	L	Read with parity error
H	H	H	L	H	L	Input	H	H	H	H	D0-D15 equals stored DO-D15
H	H	H	L	H	L	Input	L	L	L	H	Not equal
H	H	H	L	H	L	Input	L	L	L	L	Parity error
X	X	X	X	X	H	X	H	H	†	†	Force MATCH1 and MATCH2 unconditionally high
X	X	X	H	H	X	Hi-Z	H	H	H	H	Device disabled
X	X	X	X	L	X	Hi-Z	H	H	H	H	Memory reset

† The state of these pins is dependent on inputs shown as irrelevant (X).

TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	5	Address inputs. Addresses 1 of the 2K 18-bit random access memory locations. Must be stable for the duration of the write cycle.
A1	4	
A2	3	
A3	2	
A4	1	
A5	44	
A6	43	
A7	21	
A8	22	
A9	23	
A10	24	
D0	7	Data (tag) inputs/outputs. D0-D15 are inputs during the compare and write modes. D0-D15 are outputs during the read mode.
D1	8	
D2	9	
D3	10	
D4	12	
D5	13	
D6	14	
D7	15	
D8	31	
D9	32	

TERMINAL FUNCTIONS (Concluded)

PIN NAME	PIN NO.	DESCRIPTION
D10 D11 D12 D13 D14 D15	33 34 36 37 38 39	Data (tag) inputs/outputs. D0-D15 are inputs during the compare and write modes. D0-D15 are outputs during the read mode.
FMHB	41	Force Match Halt Berr input. When FMHB is high, MATCH1 and MATCH2 are unconditionally forced high.
GND	11,16,30,35,40	Ground
MATCH1 MATCH2 MATCH3	25 26 29	When MATCH1, MATCH2, and MATCH3 are high during a compare cycle, D0-D15 plus generated parity equal the contents of the 18-bit memory location addressed by A0-A10. MATCH1, MATCH2, and MATCH3 are driven high during deselect, reset, read, and write. MATCH1 and MATCH2 are also forced high when FMHB is high. The MATCH outputs will be low if a parity error exists in compare mode. Only MATCH3 will be low if a parity error exists in read mode. MATCH1 and MATCH2 are open-drain outputs and MATCH3 is a totem-pole output.
$\overline{PE}$	27	Parity Error output/input. A low level at $\overline{PE}$ indicates a parity error in the addressed data. During a write cycle a parity error can be forced into one or both bytes (depending on the state of $\overline{W}1$ and $\overline{W}2$) by taking $\overline{PE}$ low. $\overline{PE}$ is an open-drain output.
$\overline{R}$	17	Read input. When $\overline{R}$ and $\overline{S}$ are low and $\overline{W}1$ and $\overline{W}2$ are high, addressed data is output to the D0-D15 pins. During read, the match outputs are high unless a parity error exits.
$\overline{RESET}$	42	Reset input. Asynchronously clears entire RAM array to zero and forces the match outputs and $\overline{PE}$ high when $\overline{RESET}$ is low. $\overline{RESET}$ functions independent of the $\overline{S}$ input.
$\overline{S}$	18	Chip Select input. Enables device when $\overline{S}$ is low. Deselects device and forces the match outputs and $\overline{PE}$ high when $\overline{S}$ is high.
V_{CC}	6, 28	Supply voltage
$\overline{W}1$ $\overline{W}2$	19 20	Write control inputs. $\overline{W}1$ writes D0-D7 plus generated parity into RAM and forces the match outputs high when $\overline{W}1$ and $\overline{S}$ are low. $\overline{W}2$ writes D8-D15 plus generated parity into RAM and forces the match outputs high when $\overline{W}2$ and $\overline{S}$ are low. By taking $\overline{W}1$ and $\overline{W}2$ low, D0-D15 plus generated byte parity is written into the RAM and the match outputs are forced high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... −1.5 V to 7 V
Input voltage (any input) ..... −1.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}): D0-D15, MATCH3 ..... ± 25 mA
MATCH1, MATCH2, $\overline{PE}$ ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC} + 0.5	V
V_{IL}	Low-level input voltage (see Note 2)		− 0.5		0.8	V
V_{OH}	High-level output voltage	MATCH1, MATCH2, and $\overline{PE}$ outputs			5.25	V
I_{OH}	High-level output current, D0-D15 and Q15				− 8	mA
I_{OL}	Low-level output current	MATCH1, MATCH2			48	mA
		$\overline{PE}$			24	
		D0-D15, MATCH3			8	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with − 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	D0-D15, MATCH3	V_{CC} = 4.75 V,	I_{OH} = − 8 mA	3.7			V
V_{OL}	Low-level output voltage	MATCH1, MATCH2	V_{CC} = 4.75 V,	I_{OL} = 48 mA			0.4	V
		$\overline{PE}$	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.4	
		D0-D15, MATCH3	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.4	
I_{OH}	High-level output current	MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 5.25 V,	V_{OH} = 5.25 V			10	µA
I_I	Input current		V_{CC} = 5.25 V,	V_I = 0 to V_{CC}			±5	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V, $\overline{S}$ at V_{IH}	V_O = 0 to V_{CC},			± 10	mA
I_{CC1}	Supply current (operating)		V_{CC} = 5.25 V, $\overline{S}$ at 0 V	$\overline{RESET}$ at 3 V,		135	190	mA
I_{CC2}	Supply current (reset)		V_{CC} = 5.25 V, $\overline{S}$ at 0 V	$\overline{RESET}$ at 0 V,		10	25	mA
I_{CC3}	Supply current (deselected)		V_{CC} = 5.25 V, $\overline{S}$ at V_{CC}	$\overline{RESET}$ at 3 V,		100	150	mA
C_I	Input capacitance		f = 1 MHz				5	pF
C_O	Output capacitance		f = 1 MHz				6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

compare cycle

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address to MATCH1, MATCH2, and MATCH3		15	20	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$		21	28	ns
$t_{a(S)}$	Access time from $\overline{S}$ to MATCH1, MATCH2, and MATCH3		11	14	ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH1, MATCH2, and MATCH3		9	14	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH1, MATCH2, and MATCH3 high		6	12	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH1, MATCH2, and MATCH3 high		6	12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}1$ and $\overline{W}2$ low to MATCH1, MATCH2, and MATCH3 high		6	12	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}1$ and $\overline{W}2$ low to $\overline{PE}$ high		7	11	ns
$t_{p(FMHB-M)}$	Propagation time, FMHB to MATCH1 and MATCH2		5	10	ns
$t_{p(WH-M)}$	Propagation delay, $\overline{W}1$ and $\overline{W}2$ high to MATCH‡		14		ns
$t_{p(WH-PE)}$	Propagation delay, $\overline{W}1$ and $\overline{W}2$ high to $\overline{PE}$‡		14		ns
$t_{v(A-M)}$	Valid time, MATCH1, MATCH2, and MATCH3 change of address	2			ns
$t_{v(D-M)}$	Valid time, MATCH1, MATCH2, and MATCH3 after change of data	1			ns
$t_{v(S-M)}$	Valid time, MATCH1, MATCH2, and MATCH3 (low) after $\overline{S}$ high	1			ns
$t_{v(A-P)}$	Valid time, $\overline{PE}$ after change of address	2			ns

read cycle

PARAMETER			MIN	TYP†	MAX	UNIT
$t_{a(A-D)}$	Read access time from address to D0-D15			20	27	ns
$t_{en(S-D)}$	Enable time from $\overline{S}$ low to D0-D15			12	20	ns
$t_{en(R-D)}$	Enable time, $\overline{R}$ low to D0-D15			11	18	ns
t_{dis}	D0-D15 output disable time from high or low level from $\overline{R}$, $\overline{S}$, $\overline{W}1$, and $\overline{W}2$			8	15	ns
$t_{p(R-M)}$	Propagation time, $\overline{R}$ low	MATCH1 and MATCH2 high		6	10	ns
		MATCH3 high or low		16	22	
$t_{v(A-D)}$	Valid time, D0-D15 after change of address		2			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The MATCH and $\overline{PE}$ outputs will glitch at the end of a write cycle after $\overline{W}1$ and $\overline{W}2$ return high. These specs assure that the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}1$ and $\overline{W}2$ return high.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{w(RSTL)}$	Pulse duration, $\overline{RESET}$ low	40			ns
$t_{w(WL)}$	Pulse duration, $\overline{W1}$ and $\overline{W2}$ low, without writing $\overline{PE}$	11			ns
$t_{w(WL)PE}$	Pulse duration, $\overline{W1}$ or $\overline{W2}$ low, writing $\overline{PE}$ (see Note 3)	18			ns
$t_{su(A)}$	Setup time, address before $\overline{W1}$ and $\overline{W2}$ low	0			ns
$t_{su(D)}$	Setup time, data before $\overline{W1}$ and $\overline{W2}$ high	10			ns
$t_{su(P)}$	Setup time, $\overline{PE}$ before $\overline{W1}$ or $\overline{W2}$ high (see Note 3)	7			ns
$t_{su(S)}$	Setup time, $\overline{S}$ low before $\overline{W1}$ or $\overline{W2}$ high	10			ns
$t_{su(RST)}$	Inactive state setup time, $\overline{RESET}$ before $\overline{W1}$ or $\overline{W2}$ high	15			ns
$t_{h(A)}$	Hold time, address after $\overline{W1}$ and $\overline{W2}$ high	0			ns
$t_{h(WH-D)}$	Hold time, data after $\overline{W1}$ and $\overline{W2}$ high	2			ns
$t_{h(WL-D)}$	Hold time, data after $\overline{W1}$ and $\overline{W2}$ low with MATCH high (see Note 4)	11			ns
$t_{h(P)}$	Hold time, $\overline{PE}$ after $\overline{W1}$ or $\overline{W2}$ high	2			ns
$t_{h(S)}$	Hold time, $\overline{S}$ low before $\overline{W1}$ or $\overline{W2}$ high	0			ns
t_{AVWH}	Address valid to write enable high	11			ns

NOTES: 3. The pulse-duration requirement specified by $t_{w(WL)PE}$ is only necessary when a parity error exists, (i.e., $\overline{PE}$ output is low) prior to writing data with correct parity (i.e., $\overline{PE}$ input is high during write). Parameter $t_{su(P)}$ applies only during the write cycle timing when writing a parity error.

4. $t_{h(D-WL)}$ ensures that when $\overline{W1}$ or $\overline{W2}$ is taken low during a compare cycle with the match outputs high that the match outputs will remain high without a glitch low. (As shown in the function table, $\overline{W1}$ and $\overline{W2}$ low forces the match outputs high). $t_{h(WL-D)}$ is ensured indirectly by $t_{v(D-M)}$ and $t_{p(W-MH)}$.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH TRANSITION OF $\overline{PE}$ OUTPUT FOR VARIOUS LOADS

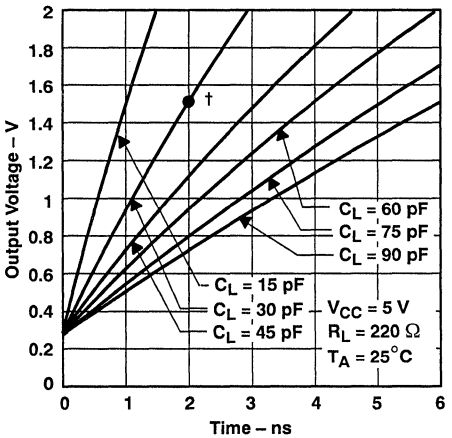


FIGURE 1

LOW-TO-HIGH TRANSITION OF MATCH1 AND MATCH2 OUTPUTS FOR VARIOUS LOADS

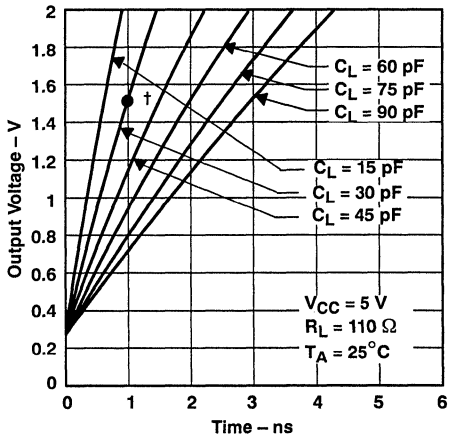
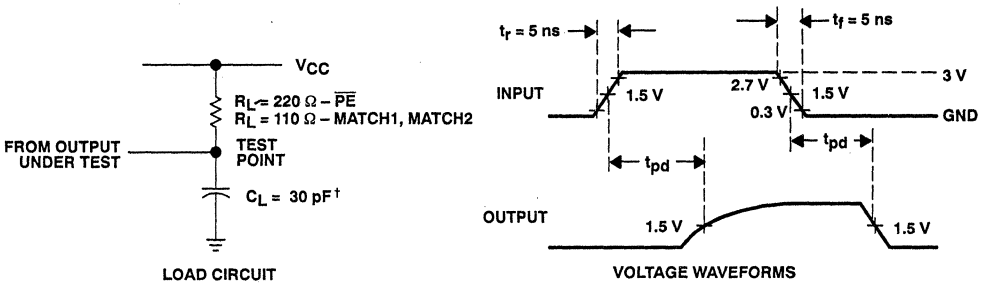


FIGURE 2

† Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

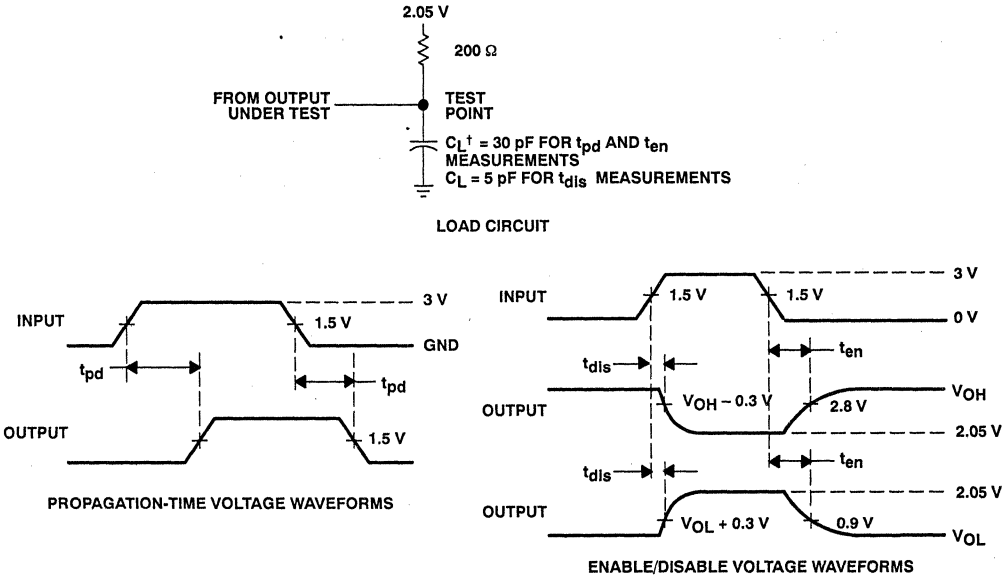
Figure 1 is provided as a tool to determine how propagation delay specifications for a 24-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 2-ns increase in a specified propagation delay. Figure 2 can be evaluated accordingly for a 48-mA open-drain output.

PARAMETER MEASUREMENT INFORMATION



† C_L includes probe and test fixture capacitance.

FIGURE 3. OPEN-DRAIN OUTPUTS



† C_L includes probe and test fixture capacitance.

FIGURE 4. ALL OTHER OUTPUTS

PARAMETER MEASUREMENT INFORMATION

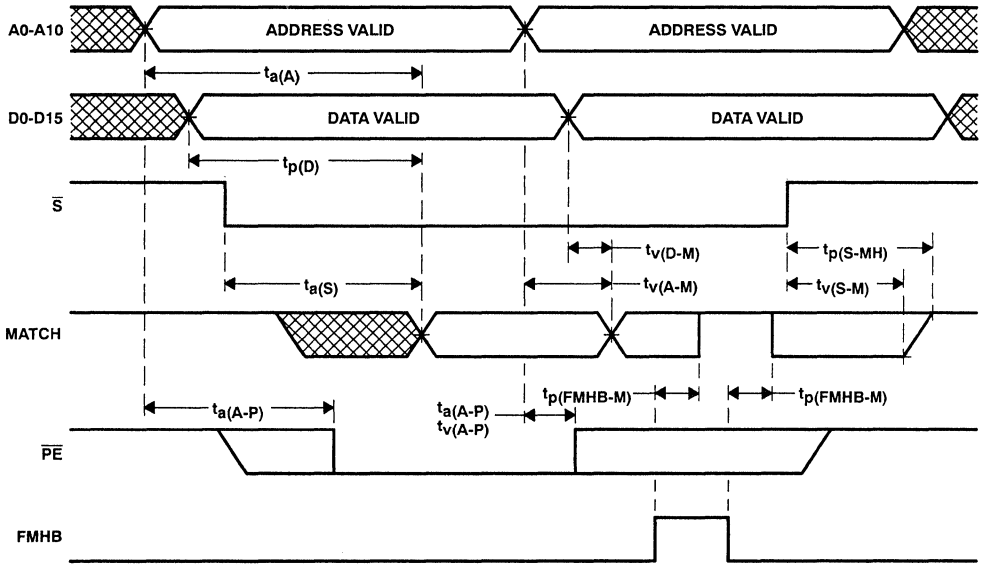


FIGURE 5. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

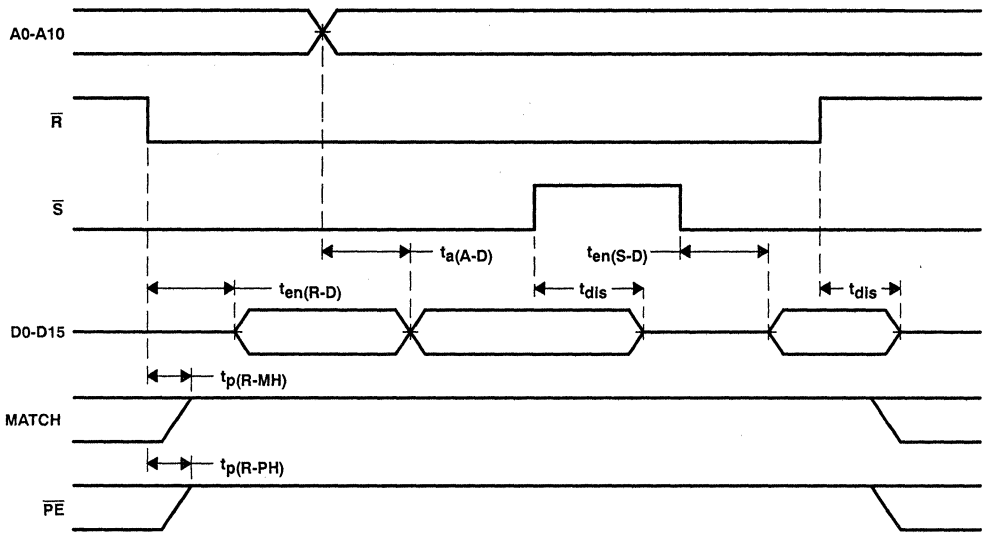


FIGURE 6. READ CYCLE TIMING

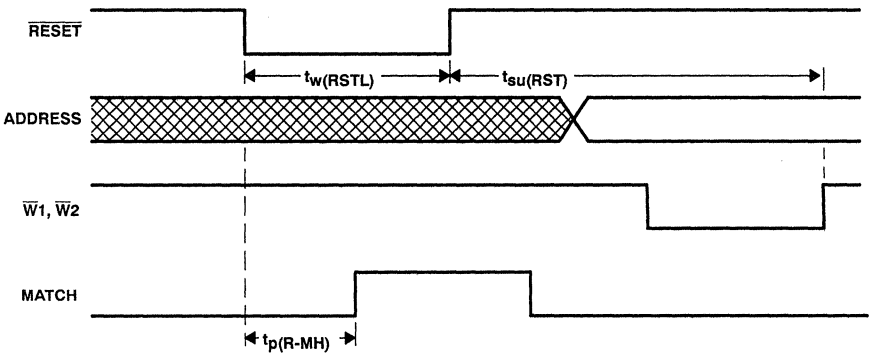


FIGURE 7. RESET CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

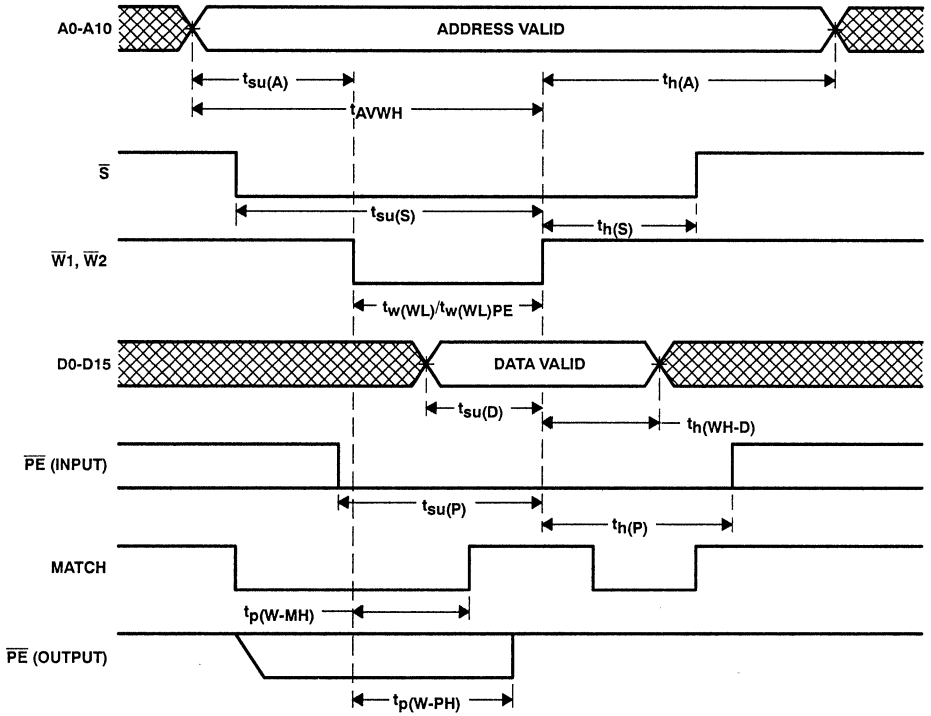
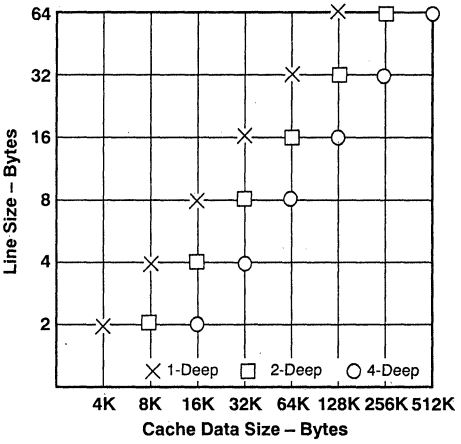


FIGURE 8. WRITE CYCLE TIMING

APPLICATION INFORMATION

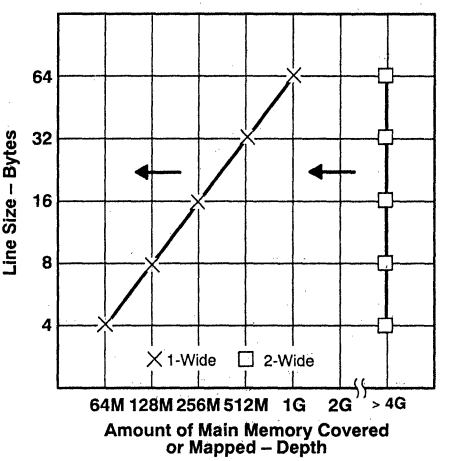
DEPTH CASCADING
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†



† Direct-Mapped Caches – One tag per line

FIGURE 9

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE†



† One tag/line, assumes a word length of 32 bits

FIGURE 10

depth cascading

For two-way caches, each solution shown is moved to the right one increment doubling the cache size, and the number of devices used. Four-way cache designs using the 'ACT2157 will quadruple each solution shown within Figure 9.

width cascading

Memory coverage assumes one bit used as a valid bit (see Figure 10). Each solution for given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth, memory coverage increases; i.e., two deep maps twice as much memory.

usage explaination and example

Figures 9 and 10 provide a quick means for determining if the 'ACT2157 will provide a good solution and the number of devices needed for implementation. For example, a design requires 16K bytes of direct-mapped cache, memory coverage of 128M, and a line size of 4 bytes. (A 4-byte line size means each tag location maps one 32-bit words of cached data.) From Figure 9, it is determined that two 'ACT2157s will provide a 16K-byte cache with a 4-byte line. From Figure 10, it is determined that one 'ACT2157 will map 128M of memory, provided it is cascaded once, in the depth direction (i.e., two deep). Therefore, two deep by one wide is equivalent to two 'ACT2157s. Two devices provide a perfect solution.

APPLICATION INFORMATION

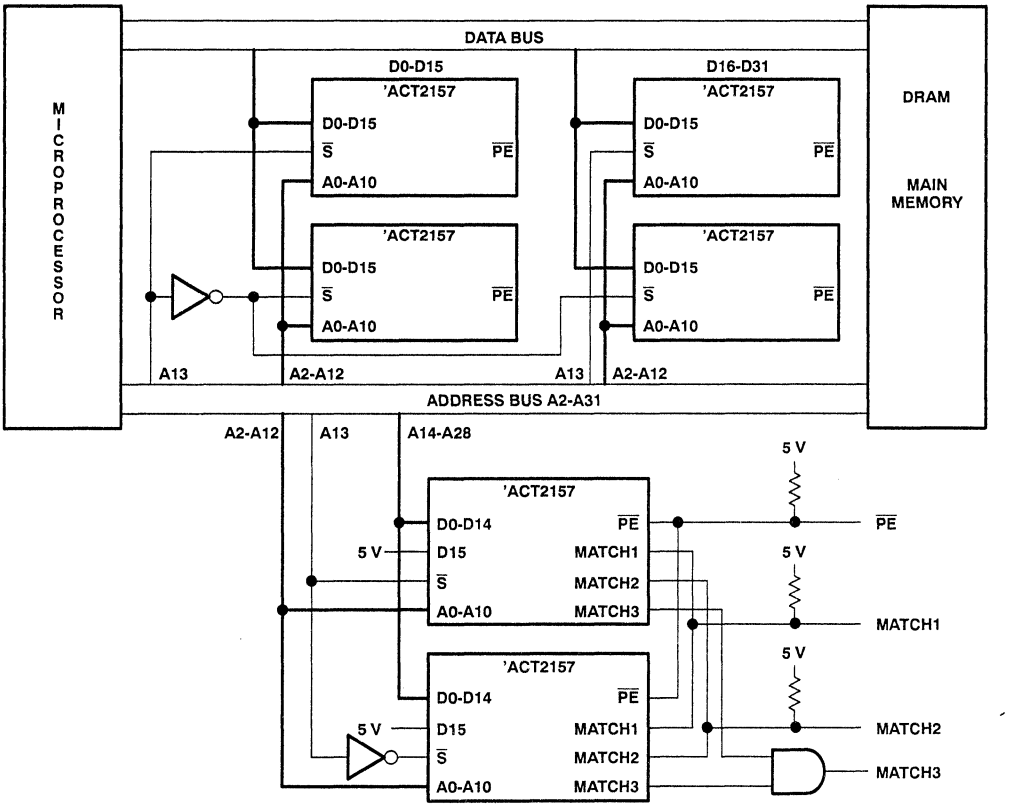


FIGURE 11. cascading the 'ACT2157

APPLICATION INFORMATION

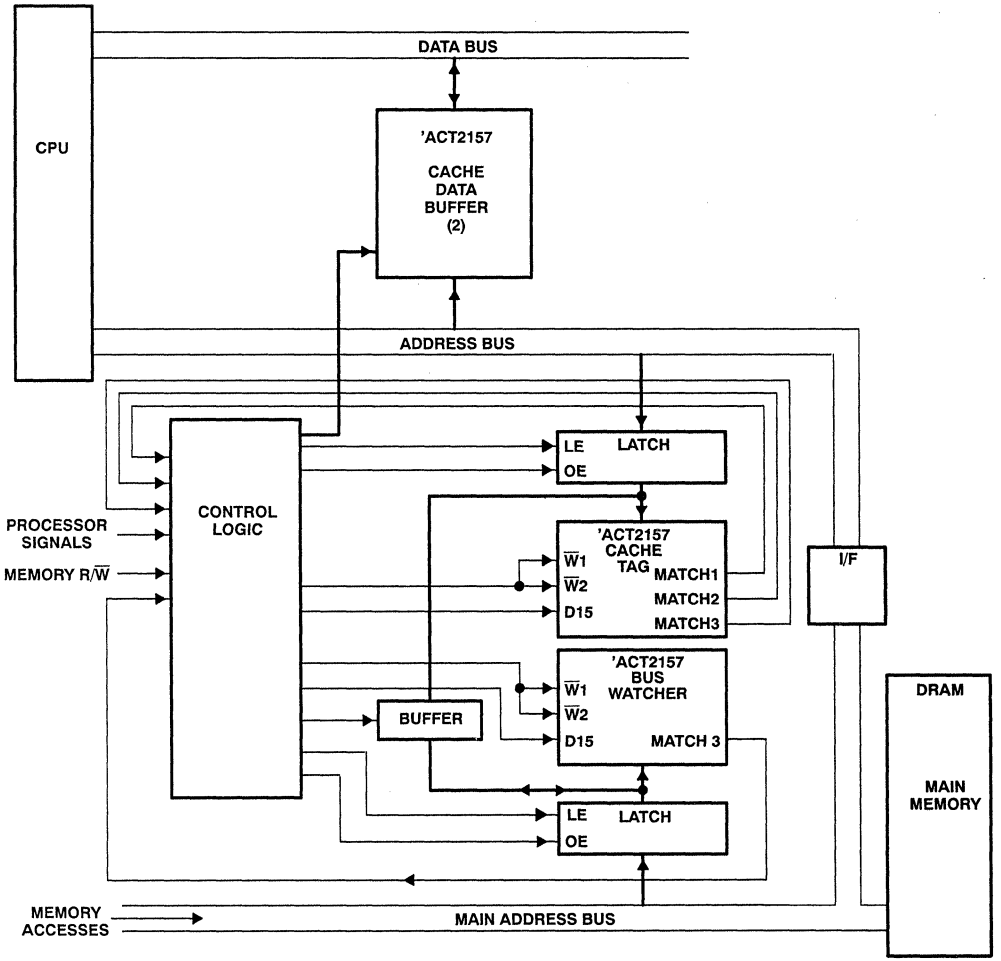


FIGURE 12. BUS WATCHING USING THE 'ACT2157

APPLICATION INFORMATION

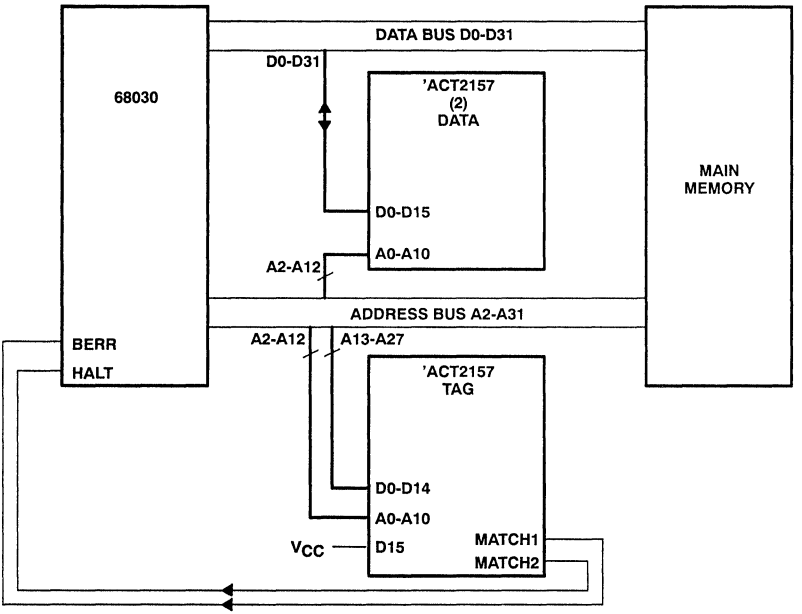


FIGURE 13. 'ACT2157/68030 INTERFACE

APPLICATION INFORMATION

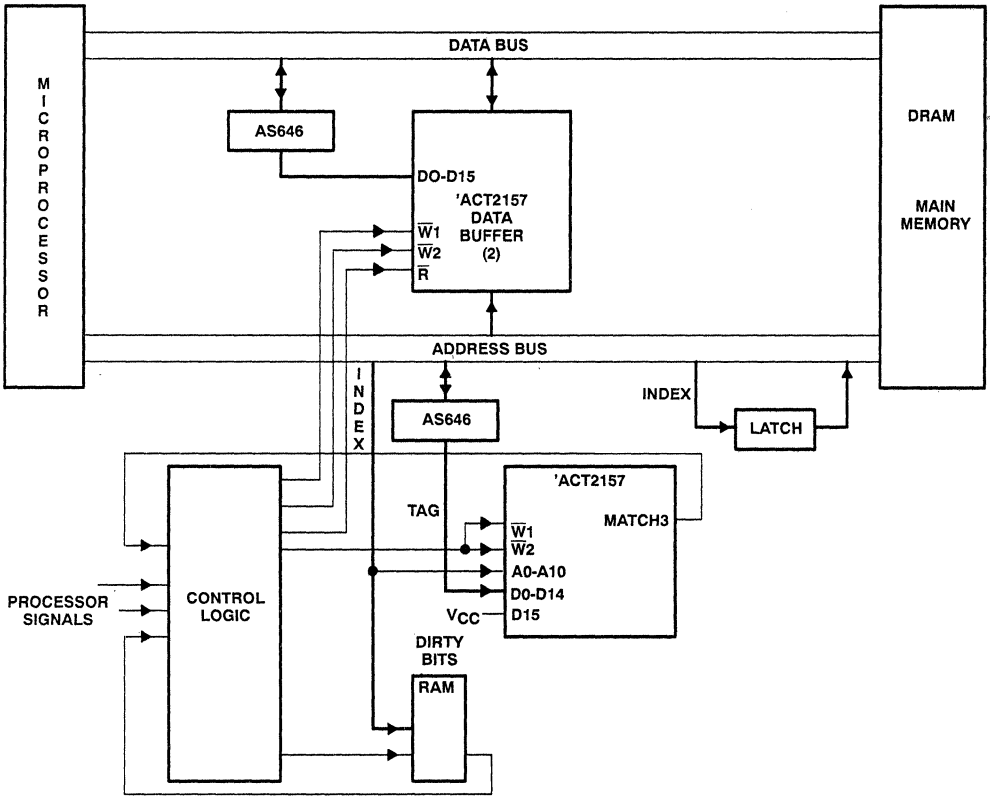
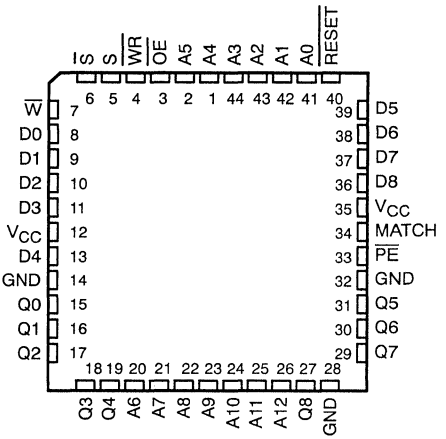


FIGURE 14. COPY-BACK USING THE 'ACT2157

D3281, MAY 1990–REVISED JUNE 1990

- **Fast Address to MATCH Delay 22 ns Max**
- **8K × 10 Internal Static RAM**
- **On-Chip Address/Data Comparator**
- **Read Feature with Separate I/O**
- **Word Reset Function for Single Entry Invalidation**
- **On-Chip Parity Generator and Checking**
- **Easily Expandable in Width and Depth**
- **Choice of Open-Drain ('ACT2159) or Totem-Pole ('ACT2158) MATCH Output**
- **Fully TTL Compatible**

FN PACKAGE
(TOP VIEW)



description

The 'ACT2158 and 'ACT2159 cache address comparators consist of a high-speed 8K x 10 static RAM array, parity generator, parity checker, and 10-bit high-speed comparator. They are fabricated using advanced silicon gate CMOS technology for high speed and simple interface with bipolar TTL circuits. A single 'ACT2158 or 'ACT2159 can provide comparison for 8192 addresses of 22 bits each. In addition, these devices are easily cascaded for greater address width and/or depth.

Significant reductions in cache memory component count, board area, and power dissipation can be achieved with these devices. The 'ACT2158 has a totem-pole MATCH output while the 'ACT2159 has an open-drain MATCH output for wire AND-tying. These devices operate from a single 5-V power supply.

The SN74ACT2158 and SN74ACT2159 are characterized for operation from 0°C to 70°C.

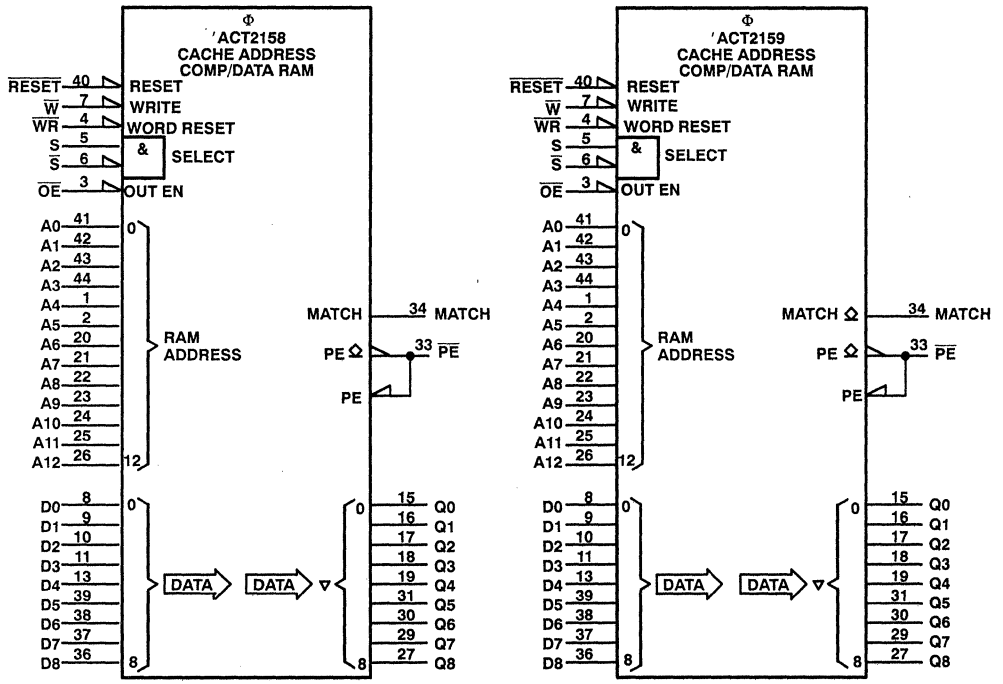
FUNCTION TABLE

INPUTS						OUTPUTS			FUNCTION
$\overline{W}$	$\overline{OE}$	S	$\overline{S}$	$\overline{RESET}$	$\overline{WR}$	MATCH	$\overline{PE}$	Q0–Q8	
L	X	H	L	H	H	L	IN	HI-Z	Write
H	L	H	L	H	H	Active	H†	Output	Read
H	X	H	L	H	H	L	L	Hi-Z or Active	Parity Error
						L	H		Not Equal
						H	L		Undefined Error
						H	H		Equal
H	X	H	L	L	X	L	H	‡	Memory Reset (Selected)
H	X	L	X	L	X	H	H	HI-Z	Memory Reset (Deselected)
H	X	X	H	L	X	H	H	HI-Z	Memory Reset (Deselected)
H	X	H	L	H	L	L	IN	‡	Word Reset
X	X	L	X	H	X	H	H	HI-Z	Device Disabled
X	X	X	H	H	X	H	H	HI-Z	Device Disabled

† If a parity error exists in the addressed data, $\overline{PE}$ will be low.
‡ The state of these pins is dependent on input $\overline{OE}$.

These devices are covered by U.S. Patents 4,831,625; 4,858,182; 4,860,262; 4,884,270; and additional patents pending.

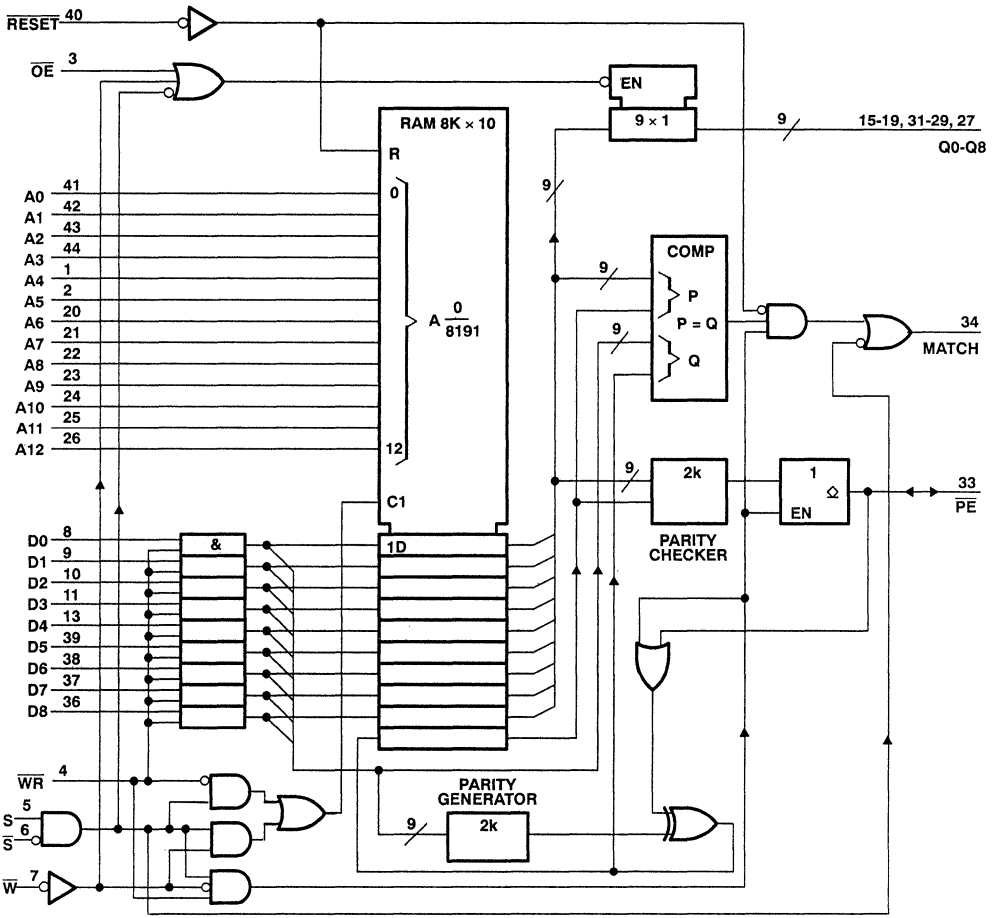
logic symbols†



† These symbols are in accordancea with IEEE Std 91-1984.

ADVANCE INFORMATION

logic diagram (positive logic)



ADVANCE INFORMATION

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Terminal Functions

PIN NAME	DESCRIPTION
A0-A12	Address inputs. Addresses 1 of 8192 by 10-bit random access memory locations. Address must be stable for the duration of the write cycle.
D0-D8	Data inputs. During write, the applied 9-bit data word plus internally generated parity is stored in the addressed memory location. During compare, D0 through D8 plus generated parity is compared with the addressesd memory location.
MATCH	When D0 through D8 plus generated parity equal the contents of the 10-bit memory location addressed by A0 through A12, the MATCH output is high during a compare cycle. MATCH is also driven high during deselect. MATCH is low during reset (device selected), write, and word reset. Since the 'ACT2159 MATCH output is open-drain, an external pull-up resistor of 220 Ω minimum is required.
$\overline{PE}$	Parity Error input/output. When the device is selected and $\overline{W}$ is high, a low on the $\overline{PE}$ output indicates a parity error in the addressed data. A parity error in the addressed data can be forced during a write or word reset cycle by applying a low at the $\overline{PE}$ pin. The $\overline{PE}$ output is disabled during reset, word reset, write, and deselect. $\overline{PE}$ is an open-drain output and an external pull-up resistor of 220 Ω minimum is required.
Q0-Q8	Data outputs. When the device is selected, $\overline{W}$ is high, and $\overline{OE}$ is low, the addressed memory location can be read at the Q0 through Q8 outputs. When the device is deselected, $\overline{OE}$ is high, and during write, Q0 through Q8 are disabled.
$\overline{RESET}$	Reset input. When low, asynchronously clears entire RAM array to zero and, if the device is selected, forces MATCH low. $\overline{RESET}$ causes valid parity to be written into each memory location.
$\overline{OE}$	Output Enable input. When the device is selected, $\overline{OE}$ is low, and $\overline{W}$ is high, addressed data is output to Q0 througoh Q8. $\overline{OE}$ high disables the Q0 through Q8 outputs.
S, $\overline{S}$	Chip Select inputs. When $\overline{S}$ is low and S is high, the device is enabled. When $\overline{S}$ is high or S is low, the device is disabled and MATCH and $\overline{PE}$ are forced high. The device can be reset when $\overline{S}$ is high or S is slow.
$\overline{W}$	Write control input. When the device is selected and $\overline{W}$ is low, D0 through D8 plus generated odd parity is written into the addressed memory location.
$\overline{WR}$	Word Reset input. When $\overline{WR}$ is low on a selected device, the addressed memory location is cleared to zero with valid parity.

operation as an address comparataor

When selected and in the compare mode, these cache address comparators compare the contents of the memory loction addressed by A0 through A12 with data D0 through D8 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level $\overline{PE}$ output indicates a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for wire OR-tying. During a write cycle, data on D0 through D8 plus generated odd parity are written into the 10-bit memory loction addressed by A0 through A12. During write, a parity error may be forced for diagnostics purposes by holding $\overline{PE}$ low.

single-entry invalidation

In cache tag systems, it is often necessary to invalidate a tag memory location when data in the cache becomes inconsistent with the data in main memory or in additional caches. The word reset function allows any addressed memory location to be cleared to zero (with valid parity) by taking the $\overline{WR}$ input low. By tying one of the data inputs high, that particular bit can be used as an internal valid bit. Whenever data is compared to a memory location cleared by $\overline{WR}$ (or by the master RESET), a miss will occur. If a data input is not tied high, a false match will occur when a data word of zero is compared to a reset location. The $\overline{WR}$ input is independent of the data at the D0 through D8 inputs.

reading the internal RAM

A read mode is provided that allows the 'ACT2158 and 'ACT2159 to be used in copy-back cache systems, for providing cache tag system diagnostics, or as a high-speed SRAM with parity generation and checking. The read mode is selected when $\overline{OE}$ is low, $\overline{W}$ is high, $\overline{S}$ is low, and S is high. The contents of the internal RAM are read at the Q0 through Q8 outputs.

initialization

A master reset input is provided for initialization. When $\overline{\text{RESET}}$ is taken low, all 8K × 10 RAM locations are cleared to zero (with valid parity). If the device is selected, the MATCH output is forced low. A data word of zero will compare to every addressed location that has not been written into since reset, causing MATCH and $\overline{\text{PE}}$ to be high. By tying a single data input high, this bit will function as a valid bit and a match will not occur unless valid data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

cascading the 'ACT2158 and 'ACT2159

The 'ACT2158 and 'ACT2159 are easily cascaded in both the width and depth directions. When cascading in the width direction, the same address bits A0 through A12 are tied to the address pins of each chip. The remaining address bits are individually tied to the data inputs D0 through D8 of each device. Two devices cascaded in width will provide comparison for 30 bits of address with one data input tied high for a valid bit. When cascading in the depth direction, two deep for 16K of addresses, address bit A13 is tied to the $\overline{\text{S}}$ pin of the first device and to the S pin of the second device. The rest of the address bits, A14-A22 for one device wide, are tied to the D0 through D8 inputs. When cascading more than two devices deep, a fast decoder must be used to determine which device is selected. When a device is deselected, the MATCH output of that device is forced high to allow for proper gating. When cascading in depth and/or width, a composite MATCH output is needed. When using the 'ACT2158, a high-speed gate such as the SN74AS20 or the SN74AS30 should be used to achieve fast MATCH times. The 'ACT2159 has an open-drain MATCH output, which provides for wire-AND tying. Figure 6 is an example of cascading the 'ACT2159 in both width and depth.

cache coherency through bus watching

When implementing cache designs, the problem of cache coherency is always a concern. One solution to this problem is to implement bus watching using the 'ACT2158 or 'ACT2159. By storing the same tags in the bus-watcher RAM as are stored in the cache-tag RAM, the bus watcher will indicate a hit every time a cached address pases down the main address bus. If data is being modified in main memory, the index can be passed to the cache-tag RAM for invalidation. Figure 8 shows a possible bus-watcher implementation.

absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1) ..... −1.5 to 7 V
Input voltage range, any input ..... −1.5 to 7 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ±25mA
Output clamp current, I_{OK} (V_I < 0 or V_I > V_{CC}) ..... ±25mA
Continuous output current, I_O (V_O = 0 to V_{CC}): Q0-Q8, MATCH (2158) ..... ±25mA
MATCH (2159), PE ..... ±50mA
Continuous current through V_{CC} or GND pins ..... ±200mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

ADVANCE INFORMATION

recommended operating conditions (see important notice)

			SN74ACT2158-22 SN74ACT2159-22			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2159) and $\overline{PE}$				5.25	V
I_{OH}	High-level output current	MATCH ('ACT2158)			−8	mA
		Q0-Q8			−4	
I_{OL}	Low-level output current	MATCH and $\overline{PE}$			24	mA
		Q0-Q8			8	
T_A	Operating free-air temperature		0		70	°C

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the threshold region of the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with −1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN74ACT2158-22 SN74ACT2159-22			UNIT
					MIN	TYP†	MAX	
I_{OH}	High-level output current	MATCH ('ACT2159)	V_{CC} = 5.25 V,	V_{OH} = 5.25 V			10	μA
		$\overline{PE}$					10	
V_{OH}	High-level output voltage	MATCH ('ACT2158)	V_{CC} = 4.75 V,	I_{OH} = – 8 mA	2.4			V
		Q0-Q8	I_{OH} = – 4 mA		2.4			
V_{OL}	Low-level output voltage	PE and MATCH	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.4	V
		Q0-Q8	V_{CC} = 4.75 V,	I_{OL} = 8 mA			0.4	
I_I	Input current		V_I = 0 to 5.25 V				±5	μA
I_{OZ}	Off–state output current		V_{CC} = 5.25 V,	V_O = 0 to V_{CC}			±10	μA
I_{CC1}	Supply current (operative)		V_{CC} = 5.25 V, S at V_{CC},	$\overline{RESET}$ at V_{CC}, $\overline{S}$ at 0 V		140	190	mA
I_{CC2}	Supply current (reset)		V_{CC} = 5.25 V, S at V_{CC},	$\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		70	135	mA
I_{CC3}	Supply current (deselect)		V_{CC} = 5.25 V, S at 0 V,	$\overline{RESET}$ at V_{CC}, $\overline{S}$ at V_{CC}		100	160	mA
C_I	Input capacitance		f = 1 MHz				5	pF
C_O	Output capacitance		f = 1 MHz				6	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

compare cycle

PARAMETER		SN74ACT2158-22 SN74ACT2159-22			UNIT
		MIN	TYP†	MAX	
$t_{a(A)}$	Access time, address to MATCH		18	22	ns
$t_{a(A\text{-}PE)}$	Access time, address to $\overline{PE}$		19	25	ns
$t_{a(S\text{-}M)}$	Access time, select to MATCH		9	15	ns
$t_{pd(D\text{-}M)}$	Propagation delay time, data to MATCH		9	15	ns
$t_{pd(RST\text{-}M)}$	Propagation delay time, $\overline{RESET}$ low to MATCH low		9	15	ns
$t_{pd(S\text{-}M)}$	Propagation delay time, deselect to MATCH high		8	12	ns
$t_{pd(W\text{-}M)}$	Propagation delay time, $\overline{W}$ or $\overline{WR}$ low to MATCH low		8	12	ns
$t_{pd(W\text{-}PE)}$	Propagation delay time, $\overline{W}$ low to $\overline{PE}$ high		5	10	ns
$t_{pd(S\text{-}PE)}$	Propagation delay time, select and deselect to $\overline{PE}$		12	18	ns
$t_{v(A)}$	MATCH valid time after change of address	3			ns
$t_{v(D)}$	MATCH valid time after change of data	3			ns
$t_{v(S)}$	MATCH valid time (low) after deselect	2			ns
$t_{v(A\text{-}PE)}$	Valid time, $\overline{PE}$ valid time after change of address	2			ns
$t_{v(S\text{-}PE)}$	Valid time, PE valid time after deselect	2			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ See Parameter Measurement Information for load circuits and voltage waveforms.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)†

read cycle

PARAMETER			SN74ACT2158-22 SN74ACT2159-22			UNIT
			MIN	TYP‡	MAX	
$t_{a(A-Q)}$	Read access time, address to Q0 through Q8			17	24	ns
$t_{v(A-Q)}$	Q0 through Q8 valid time after change of address		4			ns
t_{en}	Enable time, Q0-Q8 valid from	$\overline{OE}$		9	14	ns
		$\overline{W}$, S, $\overline{S}$		12	18	
t_{dis}	Disable time, Q0 through Q8 output high or low level	$\overline{OE}$, S, $\overline{S}$, $\overline{W}$		9	14	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)†

PARAMETER			SN74ACT2158-22 SN74ACT2159-22			UNIT
			MIN	TYP‡	MAX	
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low		60			ns
$t_{w(WRL)}$	Pulse duration, $\overline{WR}$ low		15			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	Without writing $\overline{PE}$	15			ns
		Writing $\overline{PE}$ (see Note 2)	20			
$t_{su(A-WL)}$	Setup time, address before $\overline{W}$ or $\overline{WR}$ low		0			ns
$t_{su(D)}$	Setup time, data before $\overline{W}$ high		12			ns
$t_{su(PE)}$	Setup time, $\overline{PE}$ before $\overline{W}$ high (see Note 2)		10			ns
$t_{su(S)}$	Setup time, S and $\overline{S}$ before $\overline{W}$ high		12			ns
$t_{su(RH)}$	Setup time, $\overline{RESET}$ inactive before $\overline{W}$ high		15			ns
$t_{h(A)}$	Hold time, address after $\overline{W}$ or $\overline{WR}$ high		1			ns
$t_{h(D)}$	Hold time, data after $\overline{W}$ high		1			ns
$t_{h(PE)}$	Hold time, $\overline{PE}$ after $\overline{W}$ high		1			ns
$t_{h(S)}$	Hold time, S and $\overline{S}$ after $\overline{W}$ high		0			ns
$t_{v(A-WH)}$	Valid time, address valid before $\overline{W}$ high		15			ns
$t_{v(A-WRH)}$	Valid time, address valid before $\overline{WR}$ high		15			ns

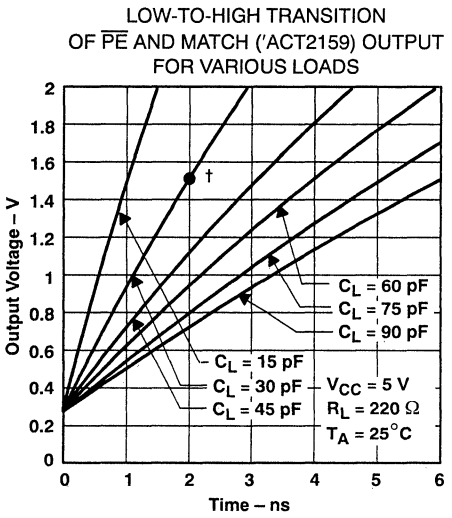
† See Parameter Measurement Information for load circuits and voltage waveforms.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: The pulse-duration requirement specified by $t_{w(WL)PE}$ is only necessary when a parity error exists, (i.e., $\overline{PE}$ output is low) prior to writing data with correct parity (i.e., $\overline{PE}$ input is high during write). Parameter $t_{su(PE)}$ applies only during the write cycle timing when writing a parity error.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS



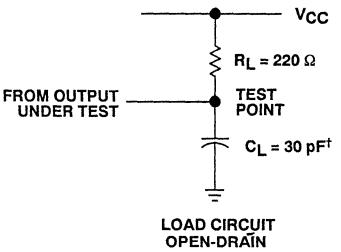
† Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

FIGURE 1

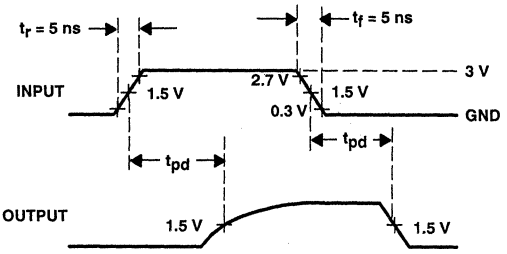
Figure 1 is provided as a tool to determine how propagation delay specifications for a 24-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 2-ns increase in a specified propagation delay.

ADVANCE INFORMATION

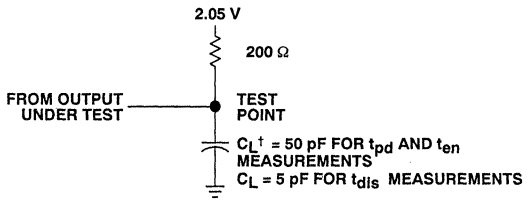
PARAMETER MEASUREMENT INFORMATION



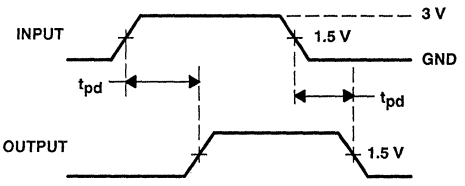
LOAD CIRCUIT
OPEN-DRAIN



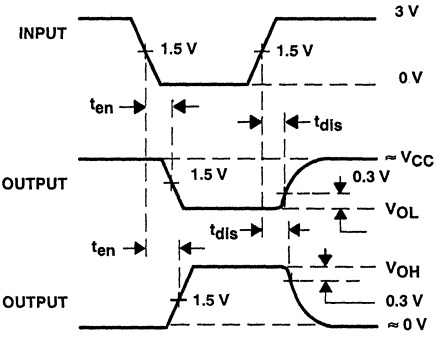
VOLTAGE WAVEFORMS
OPEN-DRAIN



LOAD CIRCUIT
TOTEM–POLE AND 3-STATE



TOTEM–POLE
PROPAGATION-TIME VOLTAGE WAVEFORMS



3-STATE ENABLE/DISABLE VOLTAGE WAVEFORMS

† C_L includes probe and test fixture capacitance.

FIGURE 2

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

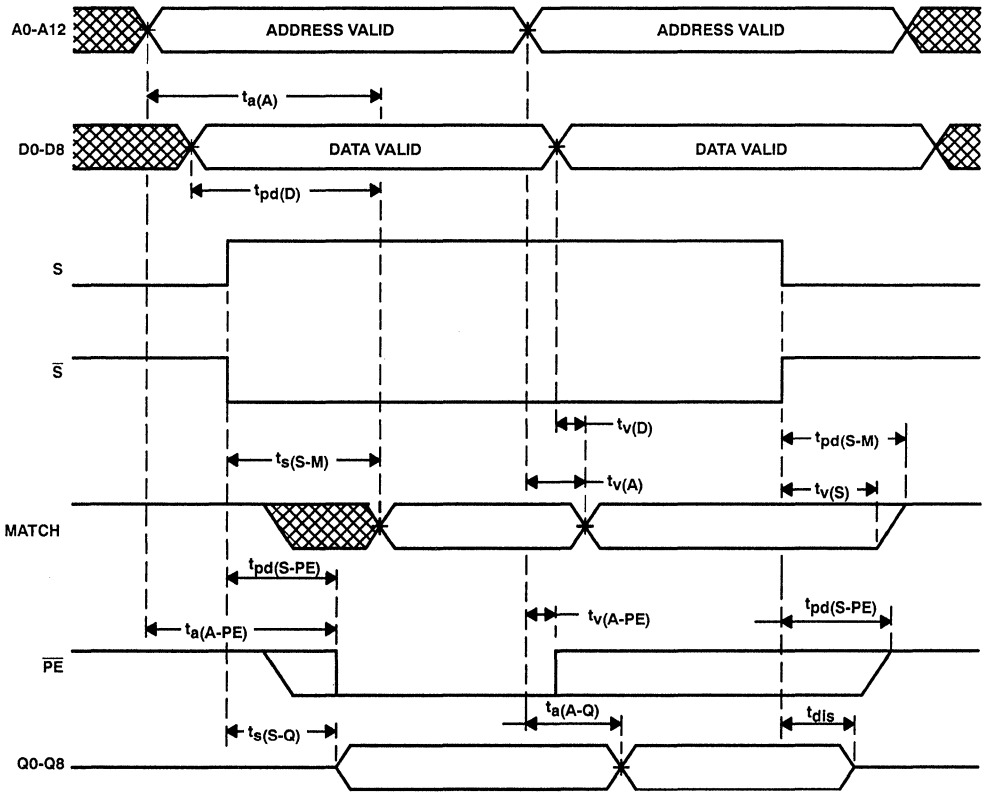
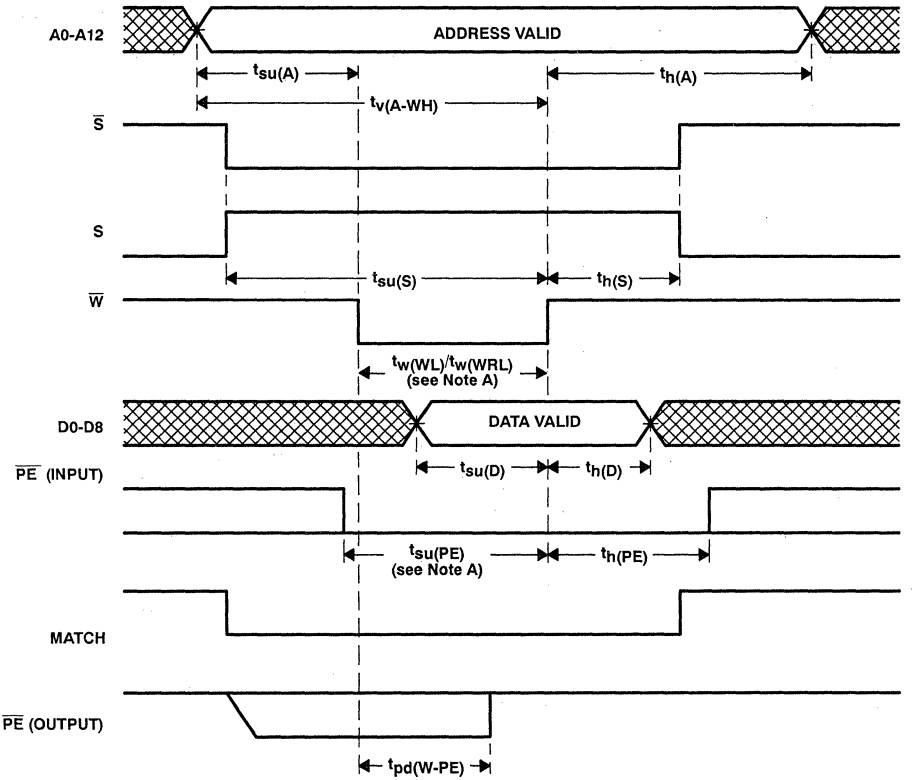


FIGURE 3. COMPARE CYCLE TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: Parameters $t_{w(WRL)}$ and $t_{su(PE)}$ apply only during the write cycle when writing a parity error.

FIGURE 4. WRITE CYCLE TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

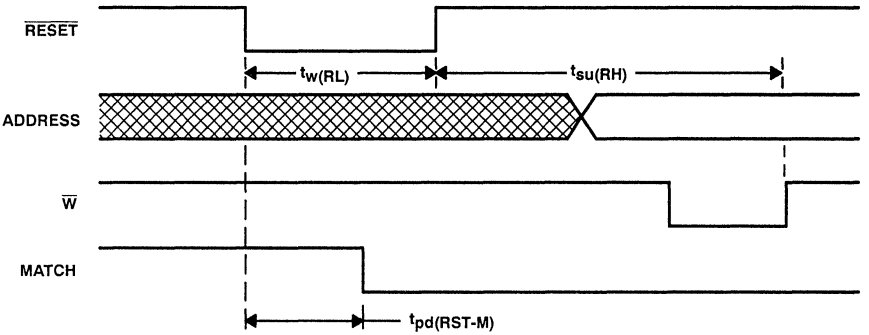


FIGURE 5. RESET CYCLE TIMING

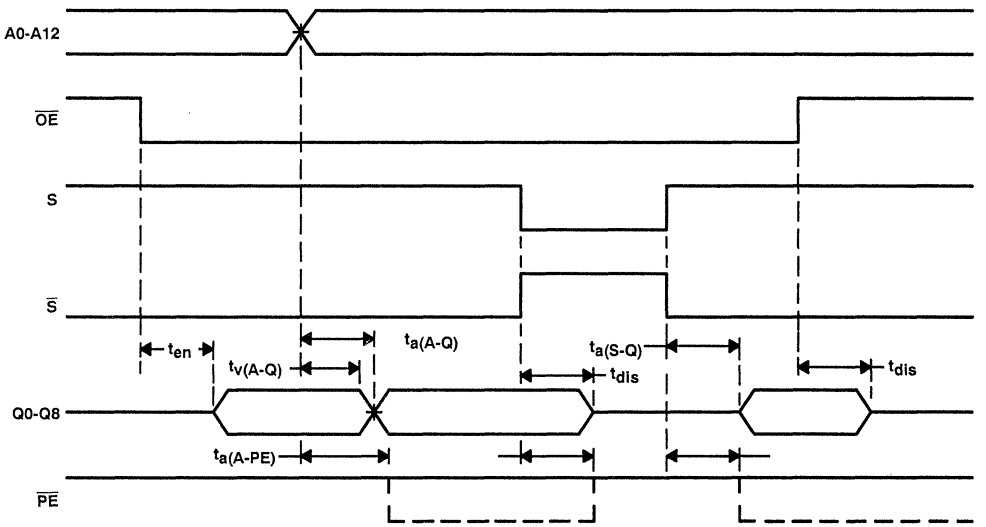
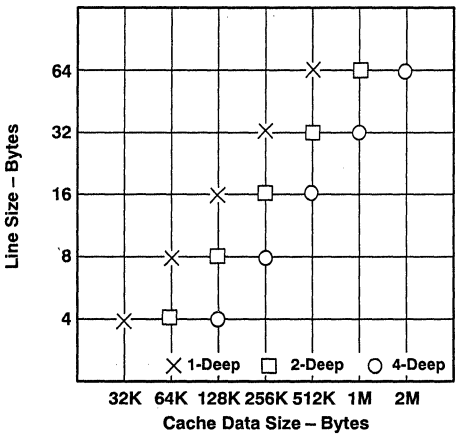


FIGURE 6. READ CYCLE TIMING

ADVANCE INFORMATION

APPLICATION INFORMATION

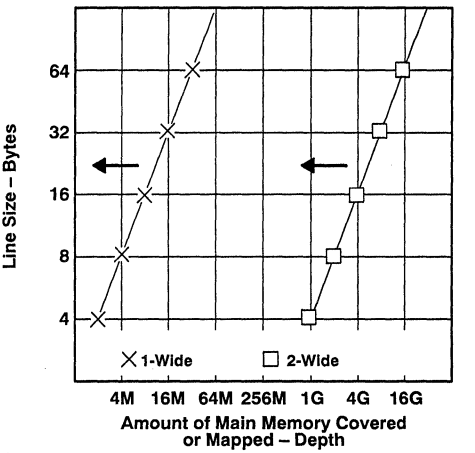
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†



† Direct-Mapped Caches

FIGURE 7

NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE†



† One Tag/line, Assumes a word length of 32 Bits

FIGURE 8

depth cascading

For two-way caches, each solultion shown is moved to the right one increment doubling the cache size and the number of devices used. Four-way cache designs using the 'ACT2158 or 'ACT2159 will quadruple each solution shown within Figure 7.

width cascading

Memory coverage assumes one bit used as a valid bit. Each solution for a given line size (see Figure 8) can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth, memory coverage increases; i.e., two deep – twice as much memory.

usage explanation and example

Figures 7 and 8 provide a quick means for determining if the 'ACT2158 or 'ACT2159 will provide a good solution and the number of devices needed for implemention. For example, a design requires 256K bytes of direct mapped cache, memory coverage of 256M, and a line size of 16 bytes; a 16-byte line size means each tag location maps four 32-bit words of cached data. From Figure 7, it is determined that two 'ACT2158s or 'ACT2159s will provide a 256K byte cache with a 16-byte line size. From Figure 8, it is determined that two 'ACT2158s or 'ACT2159s cascaded in width will map 256M of memory (or as much as 4G). Therefore, two deep by two wide or four 'ACT2158s or 'ACT2159s are needed to meet the design requirements.

ADVANCE INFORMATION

APPLICATION INFORMATION

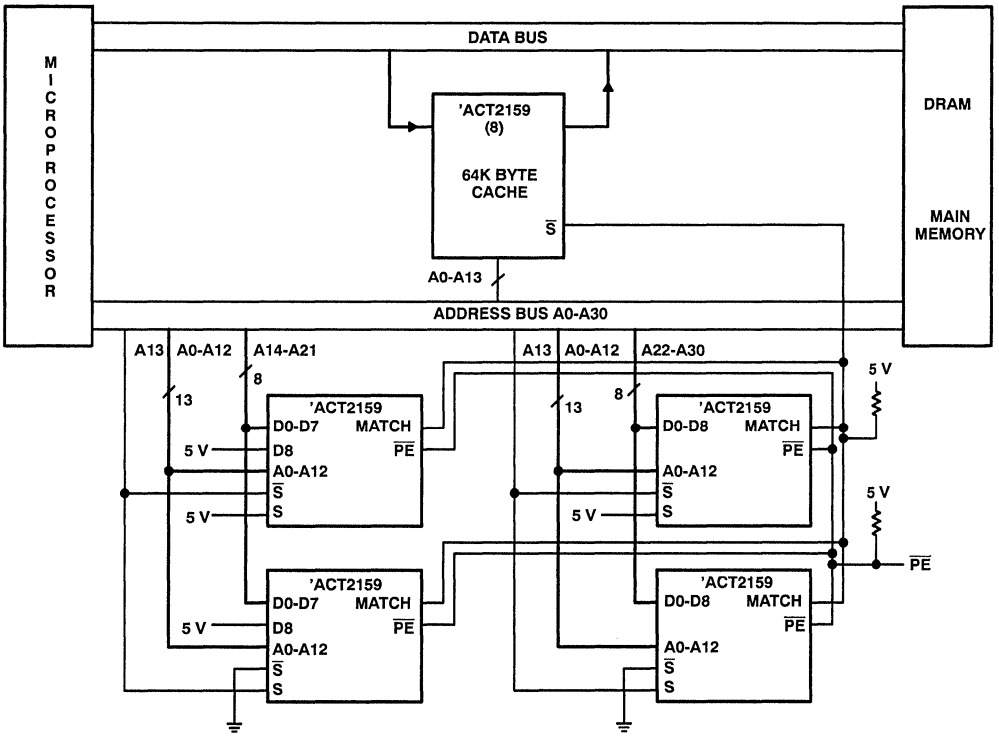


FIGURE 9. CASCADING THE 'ACT2159

ADVANCE INFORMATION

APPLICATION INFORMATION

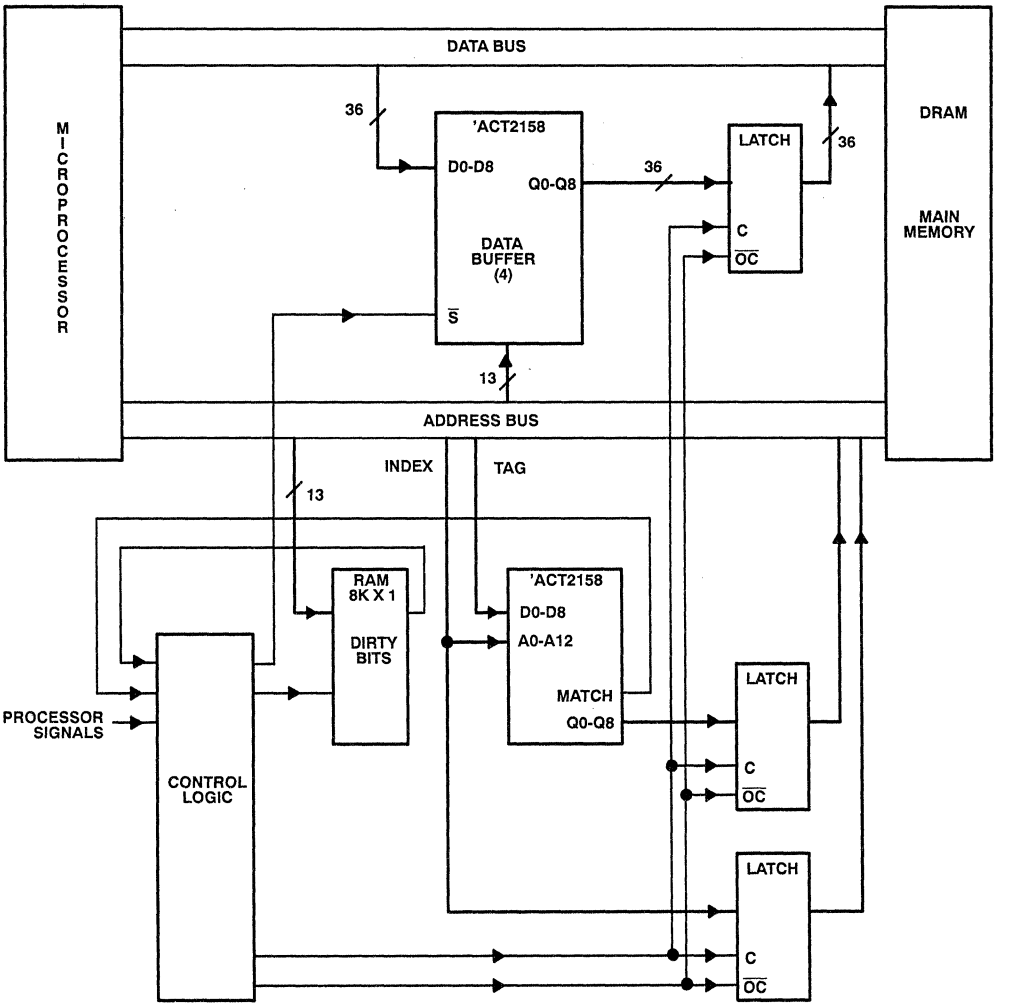


FIGURE 10. COPY-BACK SCHEME USING THE 'ACT2158

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APPLICATION INFORMATION

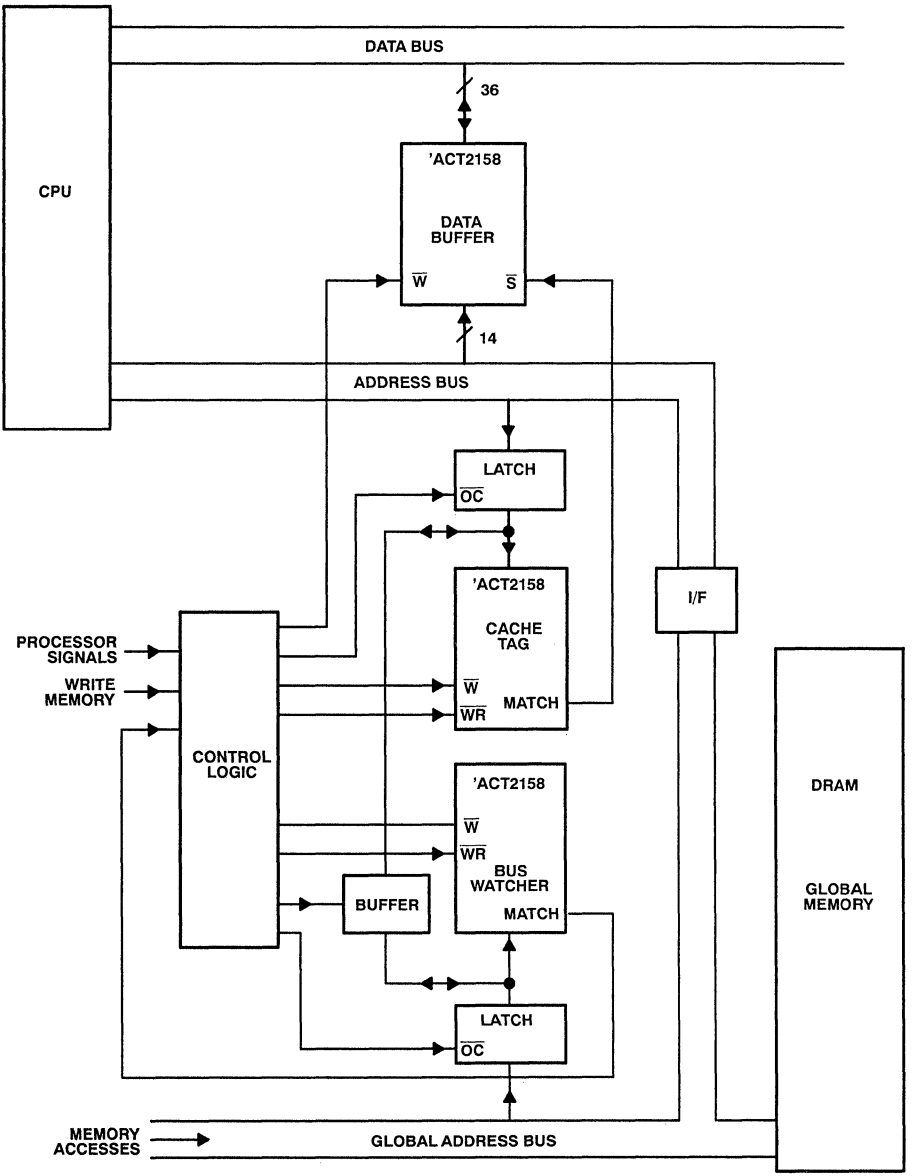
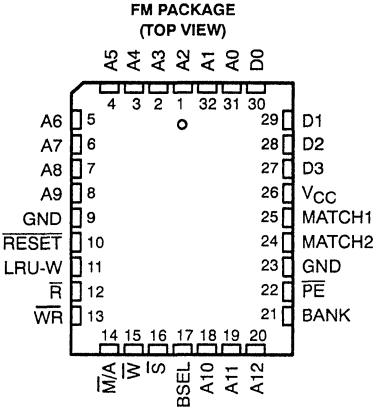


FIGURE 11. BUS WATCHING USING THE 'ACT2158

ADVANCE INFORMATION

D3365, JANUARY 1990–REVISED JUNE 1990

- **Address to Match Time . . . 17 ns Max**
- **2-Way Architecture Significantly Improves Hit Rate**
- **Implements LRU Replacement Allgorithm**
- **Useful for Bus Watching**
- **On-Chip Parity Generator and Checker**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**



description

The SN74ACT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74ACT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74ACT2160 is fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74ACT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'ACT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

ADVANCE INFORMATION

This device is covered by U.S. Patents 4,831,625; 4,837,743; 4,858,182; 4,860,262; 4,884,270; and additional patents pending.

address comparison

The 'ACT2160 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the cache tag RAMs

The manual/auto ($\overline{M}$/A) input on the 'ACT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. When writing a tag with $\overline{M}$/A low, the BANK output will not indicate which bank is being selected by the BSEL input. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'ACT2160 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

With a match output high indicating a match, the LRU RAM will also be updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address with $\overline{M}$/A high will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address with $\overline{M}$/A high will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur.

parity generation and checking

The 'ACT2160 contains parity generation and checking circuitry. When the $\overline{PE}$ output goes low, a parity error exists in one of the two tag RAMs.

During a write cycle, address bits or data on D0-D3 plus generated odd parity are written into the 5-bit memory location in either bank 1 or bank 2 that is addressed by A0-A12. Also during write, a parity error may be forced for diagnostic purposes by holding the $\overline{R}$ input low. The addressed parity bits are included in the comparator

circuitry of the 'ACT2160 so if a parity error occurs, the corresponding match output will be forced low. The bank written to is selected automatically or manually via the BSEL input depending on the state of the $\overline{M}$/A input. The LRU bit is not parity protected. The BANK outputs of the 'ACT2160s that are cascaded in width could be externally exclusive ORed to provide protection for the LRU bits.

operation as a data RAM

The 'ACT2160 can be used as a two-way 8K x 4 data RAM with parity generation and checking. By tying the manual/auto ($\overline{M}$/A) pin low, the BSEL input can be used to select which bank is being written to or read from. Through the use of the select pin, the 'ACT2160 can be cascaded for a deeper data RAM. Inputs $\overline{WR}$ and LRU-W should be tied high when using the 'ACT2160 as a data RAM.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all three 8K RAM locations are cleared to zero (with valid parity) and the MATCH1 and MATCH2 outputs are forced high. If a D0-D3 input of zero is compared to any memory location that has not been written into since reset, MATCH1 and/or MATCH2 will be high indicating that D0-D3 plus generated parity is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width. After reset, $\overline{PE}$ will be high for every addressed memory location indicating no parity error in the RAM data. After power-up, the 'ACT2160 must be initialized by resetting the device to ensure that all memory locations are at a known state. The 'ACT2160 could also be initialized by writing to every memory location (both banks) with $\overline{M}$/A low.

single-entry invalidation

In cache tag systems, it is often necessary to invalidate a tag memory location when data in the cache becomes inconsistent with the data in main memory or in additional caches. The word-reset function on the 'ACT2160 allows any addressed memory location to be cleared to zero with valid parity by taking the word reset pin ($\overline{WR}$) low. By tying one of the D0-D3 input pins high, that particular bit can be used as a valid bit. Whenever D0-D3 is compared to a memory location cleared by $\overline{WR}$ (or by the master $\overline{RESET}$), a miss will occur. If a D0-D3 input pin is not tied high, a false match will occur whenever a D0-D3 of zero is compared to a reset location. Word reset is independent of the input at the D0-D3 pins. The $\overline{M}$/A input must be low for a word reset to occur when $\overline{WR}$ is taken low. Word reset can also be accomplished by holding $\overline{WR}$ low and taking $\overline{M}$/A low to reset the addressed location. At the same time that an addressed location is reset, the addressed LRU bit is updated so that the next write to the same address with $\overline{M}$/A high will be to the reset location. Input BSEL determines which bank $\overline{WR}$ affects. When cascading in width, all devices must receive the word-reset pulse for proper LRU RAM update.

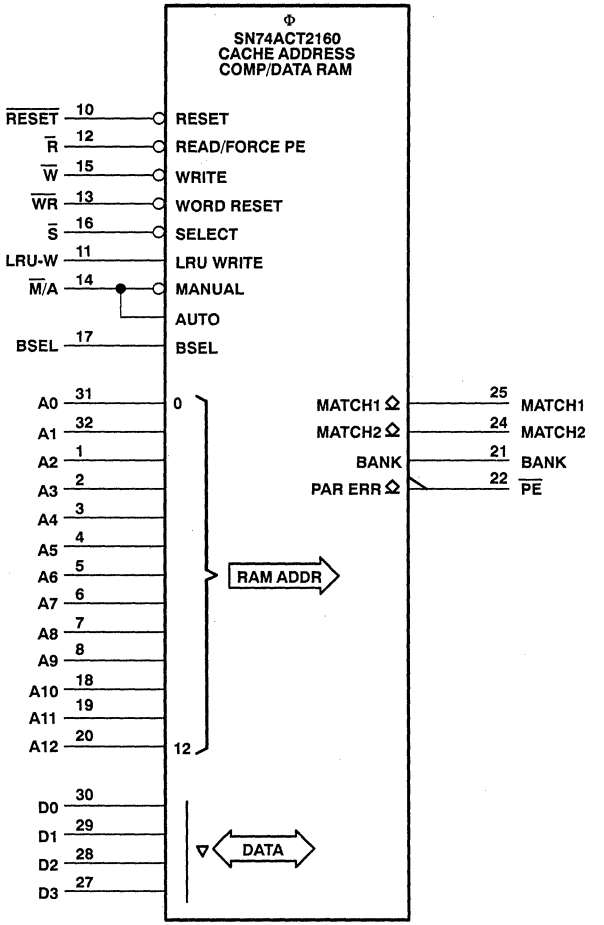
cascading the SN74ACT2160

The 'ACT2160 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A12 inputs of each device with the same index and applying the additional address bits to the D0-D3 inputs. The select ($\overline{S}$) input allows this device to be easily cascaded in depth. When a device is deselected, the MATCH1 and MATCH2 outputs are driven high. A decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire-ANDing. Figure 16 shows the 'ACT2160 cascaded.

cache coherency through bus watching

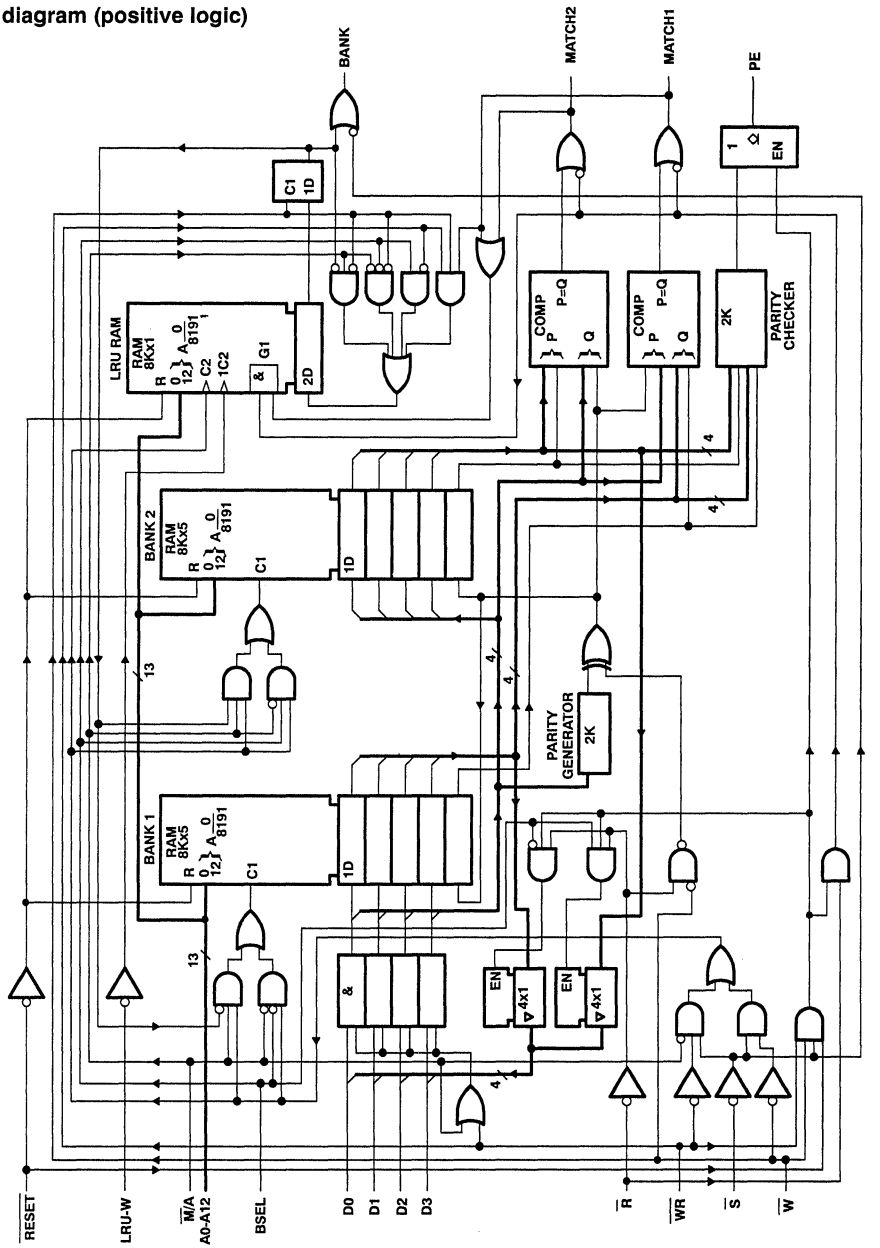
When implementing cache designs, cache coherency is usually a concern. A solution to this problem is to implement bus watching using the 'ACT2160. By storing the same tags in the bus watcher RAM as are stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 17 shows a possible bus-watcher implementation.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



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Terminal Functions

PIN NAME	DESCRIPTION
A0-A12	Address inputs. Addresses a memory location in each of the three 8K RAM arrays. Address must be stable for the duration of the write cycle.
BSEL	Bank Select input. This input is used in conjunction with the manual/auto, read and word reset functions. When BSEL is low, bank 1 is selected. When BSEL is taken high, bank 2 is selected. When $\overline{M}$/A is high, the BSEL input does not affect writing.
BANK	Bank output. The BANK output is used during a write to indicate which bank D0-D3 is being written into when $\overline{M}$/A is high. BANK is low for bank 1 and high for bank 2. BANK is forced high during reset and deselect. BANK is used to indicate which cache SRAM bank the system data should be written into. When $\overline{W}$ is taken low, the output of the LRU RAM is latched causing BANK to remain stable. When $\overline{W}$ returns high, the latch returns transparent and the BANK output will switch if the LRU bit was changed. BANK is a totem-pole output.
D0-D3	Data (tag) inputs and outputs. Provides input to RAM bank 1 or bank 2 depending on the state of the $\overline{S}$, $\overline{W}$, BSEL, $\overline{M}$/A, and $\overline{WR}$ pins. When in the compare mode, D0-D3 plus generated parity are compared to the addressed 5-bit memory location in bank 1 and bank 2. D0-D3 also function as outputs (see the $\overline{R}$ pin description).
LRU-W	Least Recently Used Write timing signal. In the compare mode, a falling edge on LRU-W will initiate an LRU write pulse if MATCH1 and/or MATCH2 are high. If a falling edge at LRU-W occurs before MATCH1 or MATCH2 are valid based on t_{pd1} and t_{su1}, the LRU write may not occur or a false LRU write could occur. LRU-W will only initiate a LRU write pulse on a falling edge. LRU-W has no effect during any other mode of operation.
$\overline{M}$/A	Manual/Auto input. The $\overline{M}$/A input determines the bank select mode for writing data. When $\overline{M}$/A is low, the bank to be written into is selected manually via the BSEL input. When the $\overline{M}$/A input is high, the bank selection is done automatically. An internal 8K x 1 RAM is used to keep track of the bank to be written into using the least recently used (LRU) replacement algorithm. After the device is reset, the first write is into bank 1. The next time data is written to the same address, it will be stored in bank 2. Successive writes to the same address automatically alternate between bank 1 and bank 2. $\overline{M}$/A can also be used to perform the word reset function. With $\overline{WR}$ low, the addressed location in the selected bank will be reset when $\overline{M}$/A is taken low.
MATCH1 MATCH2	Match outputs. When MATCH1 or MATCH2 are high during a compare cycle, D0-D3 plus generated parity equal the contents of one of two memory locations addressed by A0-A12. MATCH1 is high when D0-D3 matches D0-D3 stored in bank 1. MATCH2 is high when D0-D3 matches D0-D3 stored in bank 2. The match outputs are high during deselect, write, read, word reset, and reset. The logic level at the match outputs is fed back to the internal LRU circuitry. If a match output is high indicating a match when LRU-W is taken low, the LRU bit is adjusted so that the next write into that address will be into the other bank (LRU concept). If a match occurs with both banks (MATCH1 and MATCH2 high) and LRU-W is taken low, bank 2 will be written into when $\overline{M}$/A is low and bank 1 will be written into when $\overline{M}$/A is high. Since this device features open-drain match outputs, an external pullup resistor of 180 Ω minimum is required. If a parity error is present in bank 1 or bank 2 during compare, the corresponding match output will be forced low.
$\overline{PE}$	Parity Error output. During compare cycles, a low level at $\overline{PE}$ indicates a parity error in one of the 8K X 5 RAMs. A parity error will force the corresponding match output low. $\overline{PE}$ is an open-drain output and an external pullup resistor is required. $\overline{PE}$ is disabled during write, reset, word reset, and deselect.
$\overline{R}$	Read input. When $\overline{R}$ is low and the device is selected, D0-D3 are enabled as outputs. The output data (tag) is determined by A0-A12 and the BSEL input. Outputs D0-D3 are disabled during write, word reset, reset, deselect, and when $\overline{R}$ is high. During write cycles, a parity error can be forced into the memory location addressed by A0-A12 of the selected bank when $\overline{R}$ is taken low.
$\overline{RESET}$	Reset input. Asynchronously clears all three RAM arrays to zero with valid parity independent of the select pin when $\overline{RESET}$ is low. By tying a single data input high, a false match will not occur when a tag of zero is applied after initialization.
$\overline{S}$	Chip select input. Enables device when $\overline{S}$ is low. When $\overline{S}$ is high, MATCH1 and MATCH2 are forced high. $\overline{PE}$ and D0-D3 are disabled when $\overline{S}$ is high and BANK is forced high.
$\overline{WR}$	Word Reset input. The $\overline{WR}$ input allows any addressed memory location to be cleared to zero with valid parity. This is achieved by taking $\overline{WR}$ low while in the manual mode ($\overline{M}$/A low). The desired bank is selected using the BSEL input. When $\overline{WR}$ is asserted, the addressed LRU bit is adjusted so that the next write to that address (with $\overline{M}$/A high) is into the reset memory location. By tying a single D0-D3 input high, this bit will act as a valid bit assuring that a false match will not occur with a reset memory location.
$\overline{W}$	Write control input. When the device is selected and $\overline{W}$ is low, D0-D3 and generated parity are written into the addressed memory location in either bank 1 or bank 2. The RAM bank to be written into can be selected automatically or manually depending on the $\overline{M}$/A input.

FUNCTION TABLES

write mode

INPUTS							OUTPUTS				I/O	
$\overline{W}$	$\overline{R}$	$\overline{S}$	M/$\overline{A}$	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK†	D0-D3	FUNCTION
L	H	L	L	L	H	H	H	H	H	L‡	Input	Write into bank 1
L	H	L	L	H	H	H	H	H	H	L‡	Input	Write into bank 2
L	H	L	H	X	H	X	H	H	H	H or L‡	Input	LRU write (bank 1 or 2)
L	L	L	L	L	H	H	H	H	H	L‡	Input	Write parity error into bank 1
L	L	L	L	H	H	H	H	H	H	L‡	Input	Write parity error into bank 2
L	L	L	H	X	H	H	H	H	H	H or L‡	Input	Write parity error (LRU)
L	H	L	L	X	H	L§	H	H	H	L§	Hi-Z	Write zero into selected bank

read mode

INPUTS							OUTPUTS				I/O	
$\overline{W}$	$\overline{R}$	$\overline{S}$	M/$\overline{A}$	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	FUNCTION
H	L	L	X	L	H	H	H	H	H	H or L	Output	Read bank 1
H	L	L	X	H	H	H	H	H	H	H or L	Output	Read bank 2
H	L	L	X	X	H	H	H	H	L	H or L	Output	Parity error in bank 1 or 2
H	H	L	X	X	H	H	H or L	H or L	EN	H or L	Hi-Z	Disable/compare

compare mode

INPUTS							OUTPUTS				I/O	
$\overline{W}$	$\overline{R}$	$\overline{S}$	M/$\overline{A}$	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	FUNCTION
							H	L	H	H or L		Match bank 1, miss bank 2
							L	H	H	H or L		Match bank 2, miss bank 1
H	H	L	X	X	H	H	H	H	H	H or L		Match bank 1 and 2
				or			L	L	H	H or L	Input	Miss bank 1 and 2
H	H	L	H	X	H	X	L	L	L	H or L		Parity error bank unknown
							L	H	L	H or L		Parity error bank 1, match bank 2
							H	L	L	H or L		Parity error bank 2, match bank 1

reset, word reset, and deselect mode

INPUTS							OUTPUTS				I/O	
$\overline{W}$	$\overline{R}$	$\overline{S}$	M/$\overline{A}$	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	FUNCTION
H	X	L	X	X	L	X	H	H	H	L	Hi-Z	Memory reset-selected
H	X	H	X	X	L	X	H	H	H	H	Hi-Z	Memory reset-deselect
H	X	L	L	L	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 1
H	X	L	L	H	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 2
H	X	L	H	X	H	L	H or L	H or L	EN	H or L	Hi-Z	Word reset disabled/compare mode
X	X	H	X	X	H	X	H	H	H	H	Hi-Z	Device disabled

EN denotes enabled, H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined output

† The BANK output is transparent when $\overline{W}$ is high and latched when $\overline{W}$ is low.

‡ When writing with $\overline{M}$/A high, the BANK output indicates which bank D0-D3 is being written into. When writing with $\overline{M}$/A low, the BANK output will be forced low and will not indicate which bank is being written into. After writing with $\overline{M}$/A low, the BANK output will indicate the correct LRU bit state.

§ The state of BANK after $\overline{W}$ and $\overline{M}$/A or $\overline{W}$ and $\overline{WR}$ return high is indeterminate. This operation is not recommended.

¶ The BANK output is forced low during word reset. After a word reset in bank 2, the BANK output will be high.

ADVANCE INFORMATION

FUNCTION TABLES (continued)

LRU write

$\overline{S}$	$\overline{WR}$	$\overline{W}$	LRU-W†	MATCH1	MATCH2	QI‡	LRU WRITE	QN§	FUNCTION
L	H	↓	X	H	H	L	YES	H	Write to bank 1, selected by LRU circuitry
L	H	↓	X	H	H	H	YES	L	Write to bank 2, selected by LRU circuitry
↓	H	L	X	H	H	X	NO	–	No write occurs
L	H	H	↓	H	L	X	YES	H	Match bank 1
L	H	H	↓	L	H	X	YES	L	Match bank 2
L	H	H	↓	H	H	X	YES	L	Match bank 1 and 2
L	↓	H	X	H	L	X	YES	L	Word reset bank 1
L	↓	H	X	L	H	X	YES	H	Word reset bank 2
L	↓	H	X	H	H	X	YES	L	Word reset bank 1 and bank 2
L	↓	H	X	L	L	X	NO	–	No word reset
↓	L	H	X	H	H	X	NO	–	No word reset
H	X	X	X	H	H	X	NO	–	Device disabled

H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined level, ↓ denotes the falling edge of the signal.
† LRU-W is falling-edge-triggered and has effect only during the compare mode.
‡ QI is the state of the LRU RAM output before a LRU write occurs.
§ QN is the state of the LRU RAM output after a LRU write occurs.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 1.5 V to 7 V
Input voltage range, any input ..... – 1.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) : D0-D3, BANK ..... ± 25 mA
MATCH1, MATCH2, PE ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (see Note 2)		– 0.5		0.8	V
V_{OH}	High-level output voltage, MATCH1, MATCH2, and $\overline{PE}$				5.25	V
I_{OH}	High-level output current, D0-D3 and BANK				– 8	mA
I_{OL}	Low-level output current	D0-D3, BANK			8	mA
		MATCH1, MATCH2, $\overline{PE}$			27	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the threshold region of the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{RESET}$ pin is at its minimum high level (2.2 V). In systems with – 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{RESET}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN74ACT2160-17			UNIT
				MIN	TYP†	MAX	
V_{OH}	High-level output voltage	D0-D3, BANK	V_{CC} = 4.75 V, I_{OH} = – 8 mA	3.7			V
V_{OL}	Low-level output voltage	D0-D3, BANK	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4	V
		MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, I_{OL} = 27 mA			0.4	
I_{OH}	High-level output current	MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, V_{OH} = 5.25 V			10	µA
I_I	Input current		V_{CC} = 5.25 V, V_I = 0 to V_{CC}			±5	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{S}$ at V_{IH}			±10	µA
I_{CC1}	Supply current (operating)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at 0 V		130	180	mA
I_{CC2}	Supply current (reset)		V_{CC} = 5.25 V, $\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		30	75	mA
I_{CC3}	Supply current (deselected)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at V_{CC}		80	150	mA
C_I	Input capacitance‡		f = 1 MHz			5	pF
C_O	Output capacitance‡		f = 1 MHz			5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the capacitance at an input, output, or I/O pin.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		SN74ACT2160-17			UNIT
		MIN	TYP†	MAX	
t_{pd1}	Propagation time from address to MATCH1 and MATCH2		15	17	ns
t_{pd2}	Propagation time from D0-D3 to MATCH1 and MATCH2		9	15	ns
t_{pd3}	Propagation time from $\overline{S}$ low to MATCH1 and MATCH2		7	12	ns
t_{pd4}	Propagation time from $\overline{S}$ high to MATCH1 and MATCH2 high		7	10	ns
t_{pd5}	Propagation time from address to $\overline{PE}$		20	25	ns
t_{pd6}	Propagation time from $\overline{S}$ to $\overline{PE}$		15	20	ns
t_{pd7}	Propagation time from $\overline{S}$ to BANK		7	15	ns
t_{pd8}	Propagation time from address to BANK		15	22	ns
t_{pd9}	Propagation time from LRU-W↓ to BANK		12	18	ns
t_{pd10}	Propagation time from address to D0-D3		17	25	ns
t_{pd11}	Propagation time from BSEL to D0-D3		7	12	ns
t_{pd12}	Propagation time from $\overline{W}$ high to BANK		7	12	ns
t_{pd13}	Propagation time from $\overline{W}$ low to MATCH1 and MATCH2 high		6	10	ns
t_{pd14}	Propagation time from $\overline{W}$ low to $\overline{PE}$ high		7	11	ns
t_{pd15}	Propagation time from $\overline{RESET}$ low to MATCH1 and MATCH2 high		6	10	ns
t_{pd16}	Propagation time from word reset to MATCH1 and MATCH2 high		6	10	ns
t_{pd17}	Propagation delay, $\overline{W}$ high to MATCH‡		14	20	ns
t_{pd18}	Propagation delay, $\overline{W}$ high to $\overline{PE}$‡		14	20	ns
t_{pd19}	Propagation delay, $\overline{RESET}$ high to MATCH‡		14	20	ns
t_{pd20}	Propagation delay, $\overline{RESET}$ high to $\overline{PE}$‡		60	100	ns
t_{en1}	Enable time from $\overline{S}$ low to D0-D3		9	14	ns
t_{en2}	Enable time from $\overline{R}$ low to D0-D3		7	12	ns
t_{en3}	Enable time from $\overline{RESET}$ high to D0-D3		9	14	ns
t_{dis1}	Disable time from $\overline{R}$ high to D0-D3		7	12	ns
t_{dis2}	Disable time from $\overline{S}$ high to D0-D3		7	12	ns
t_{dis3}	Disable time from $\overline{RESET}$ low to D0-D3		9	14	ns
t_{v1}	Valid time, MATCH1 and MATCH2 after change of data	2			ns
t_{v2}	Valid time, MATCH1 and MATCH2 after change of address	1			ns
t_{v3}	Valid time, MATCH1 and MATCH2 low after $\overline{S}$ high	0			ns
t_{v4}	Valid time, $\overline{PE}$ after change of address	2			ns
t_{v5}	Valid time, $\overline{PE}$ low after $\overline{S}$ high	0			ns
t_{v6}	Valid time, D0-D3 after change of address	1			ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The MATCH and $\overline{PE}$ outputs will glitch at the end of a write or reset cycle after $\overline{W}$ or $\overline{RESET}$ returns high. These specs indicate when the MATCH and $\overline{PE}$ outputs are stable after $\overline{W}$ returns high. This specification assumes that the address and/or data inputs are not changed immediately after $\overline{W}$ or $\overline{RESET}$ high.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			SN74ACT2160-17			UNIT
			MIN	TYP†	MAX	
t_{w1}	Pulse duration, LRU-W	High	10			ns
		Low	10			
t_{w2}	Pulse duration, $\overline{W}$ low		12			ns
t_{w3}	Pulse duration, $\overline{RESET}$ low		60			ns
t_{w4}	Pulse duration, word reset	$\overline{WR}$ low with $\overline{M}$/A low	12			ns
		$\overline{M}$/A low with $\overline{WR}$ low	12			
t_{su1}	Setup time, MATCH1 and MATCH2 valid before LRU-W↓		5			ns
t_{su2}	Setup time, address valid before $\overline{W}$ high	$\overline{M}$/A high	27			ns
		$\overline{M}$/A low	12			
t_{su3}	Setup time, $\overline{S}$ low before $\overline{W}$	$\overline{W}$ high, $\overline{M}$/A = L	12			ns
		$\overline{W}$ low, $\overline{M}$/A = H	8			
t_{su4}	Setup time, address before $\overline{W}$ low	$\overline{M}$/A high	15			ns
		$\overline{M}$/A low	0			
t_{su5}	Setup time, BSEL before $\overline{W}$ low with $\overline{M}$/A low		0			ns
t_{su6}	Setup time, $\overline{M}$/A before $\overline{W}$ low		2			ns
t_{su7}	Setup time, D0-D3 before $\overline{W}$ high		10			ns
t_{su8}	Setup time, $\overline{R}$ low before $\overline{W}$ high (see Note 3)		10			ns
t_{su9}	Setup time, $\overline{RESET}$ inactive before $\overline{W}$ high		30			ns
t_{su10}	Setup time, address before word reset	$\overline{WR}$ and $\overline{M}$/A low	0			ns
t_{su11}	Setup time, BSEL before word reset	$\overline{WR}$ and $\overline{M}$/A low	2			ns
t_{su12}	Setup time, $\overline{S}$ low before word reset	$\overline{WR}$ and $\overline{M}$/A low	0			ns
t_{su13}	Setup time, word reset	$\overline{M}$/A low before $\overline{WR}$ low	0			ns
		$\overline{WR}$ low before $\overline{M}$/A low	0			
t_{h1}	Hold time, address after LRU-W↓ (see Note 4)		9			ns
t_{h2}	Hold time, $\overline{S}$ low after LRU-W↓		5			ns
t_{h3}	Hold time, address after $\overline{W}$ high		2			ns
t_{h4}	Hold time, $\overline{S}$ low after $\overline{W}$ high		0			ns
t_{h5}	Hold time, BSEL after $\overline{W}$ high		2			ns
t_{h6}	Hold time, $\overline{M}$/A after $\overline{W}$ high		2			ns
t_{h7}	Hold time, D0-D3 after $\overline{W}$ high		5			ns
t_{h8}	Hold time, $\overline{R}$ low after $\overline{W}$ high (see Note 3)		1			ns
t_{h9}	Hold time, address after word reset	$\overline{WR}$ or $\overline{M}$/A high	2			ns
t_{h10}	Hold time, BSEL after word reset	$\overline{WR}$ or $\overline{M}$/A high	2			ns
t_{h11}	Hold time, $\overline{S}$ low after word reset	$\overline{WR}$ or $\overline{M}$/A high	0			ns
t_{h12}	Hold time, word reset	$\overline{M}$/A low after $\overline{WR}$ high	0			ns
		$\overline{WR}$ low after $\overline{M}$/A high	0			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

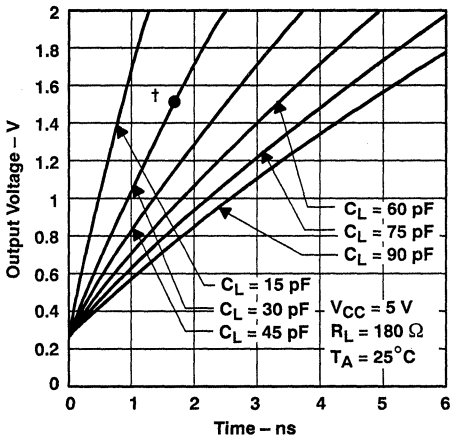
NOTES: 3. Parameters t_{su8} and t_{h8} apply only during the write cycle timing when writing a parity error. It should be noted that if $\overline{R}$ is low when $\overline{W}$ is high, D0-D3 are enabled as outputs.

4. Minimum t_{h1} is the time interval after LRU-W goes low during which the address must remain valid to ensure that an internal LRU write occurs.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

LOW-TO-HIGH TRANSITION
OF MATCH1, MATCH2, AND $\overline{PE}$ OUTPUTS
FOR VARIOUS LOADS
OUTPUT VOLTAGE vs TIME

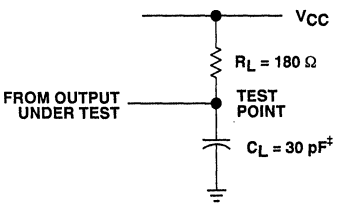


† Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

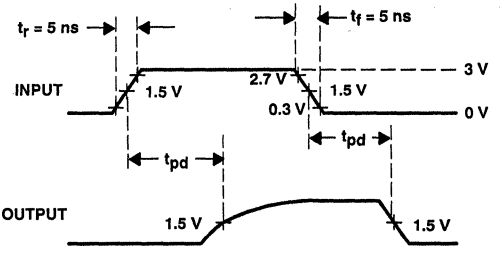
FIGURE 1

Figure 1 is provided as a tool to determine how propagation delay specifications for a 27-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause about a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 1.7-ns increase in a specified propagation delay.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

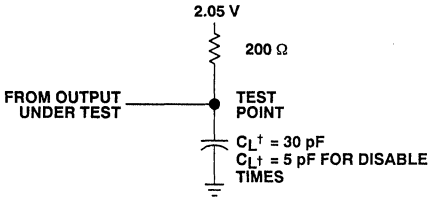


VOLTAGE WAVEFORMS

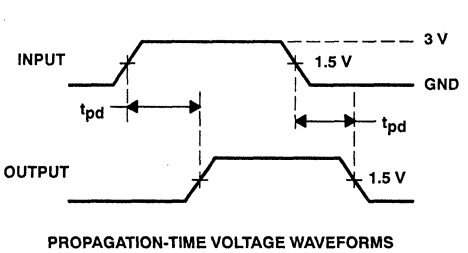
‡ C_L includes probe and test fixture capacitance.

FIGURE 2. OPEN-DRAIN OUTPUTS

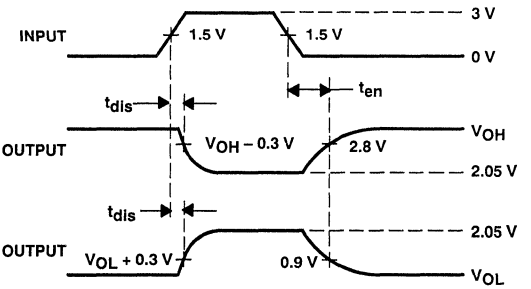
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



PROPAGATION-TIME VOLTAGE WAVEFORMS



ENABLE/DISABLE VOLTAGE WAVEFORMS

† C_L includes probe and test fixture capacitance.

FIGURE 3. ALL OTHER OUTPUTS

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

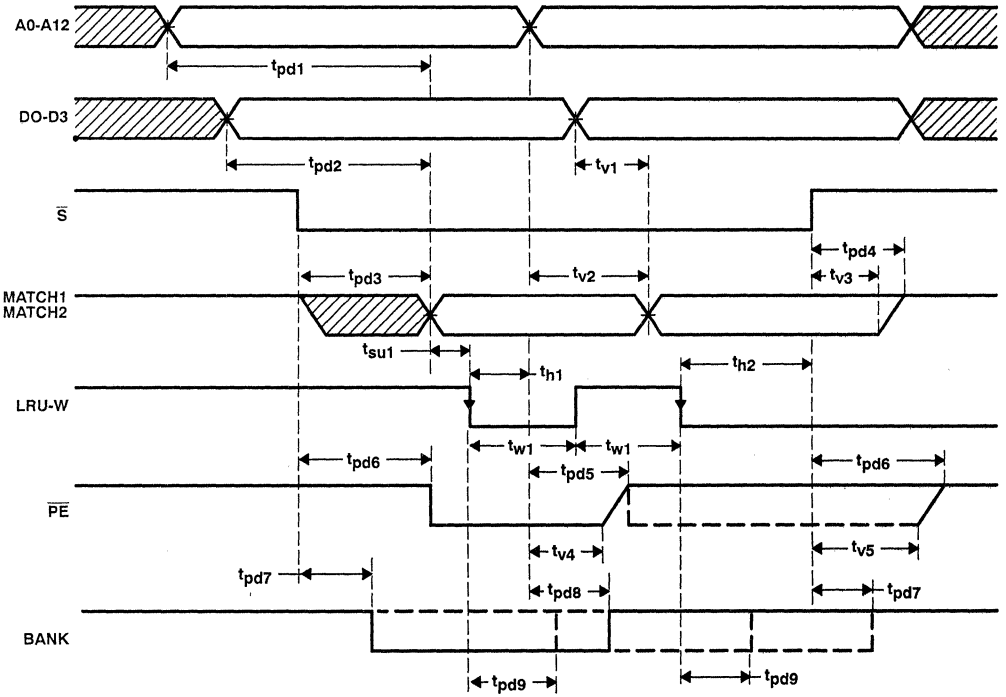


FIGURE 4. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

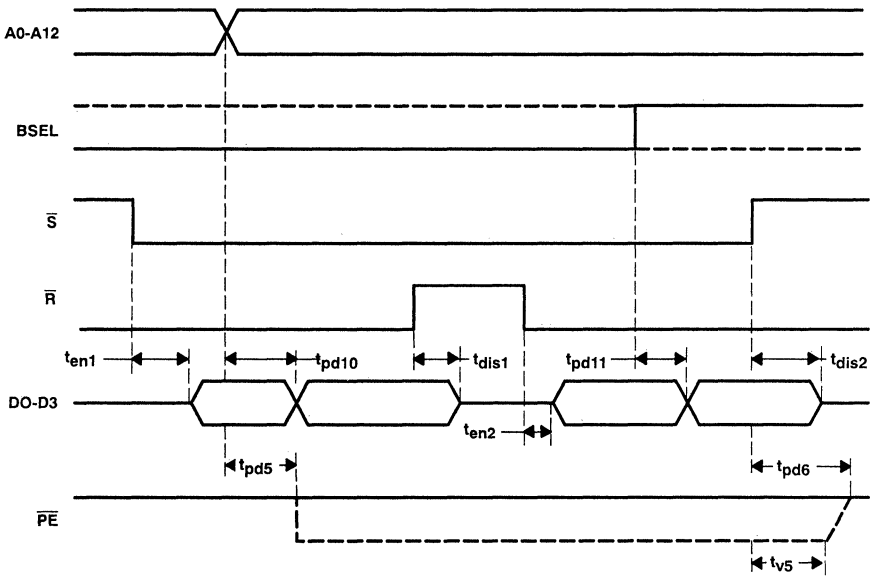


FIGURE 5. READ CYCLE TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

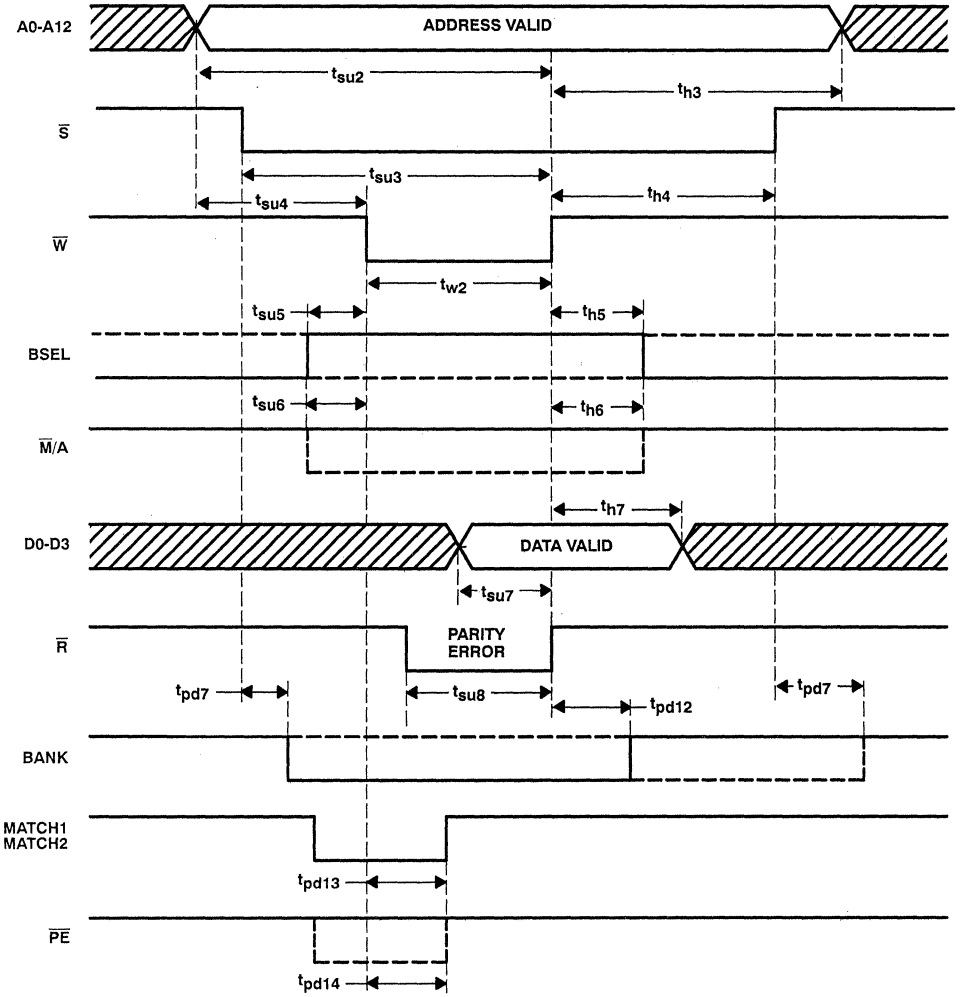


FIGURE 6. WRITE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

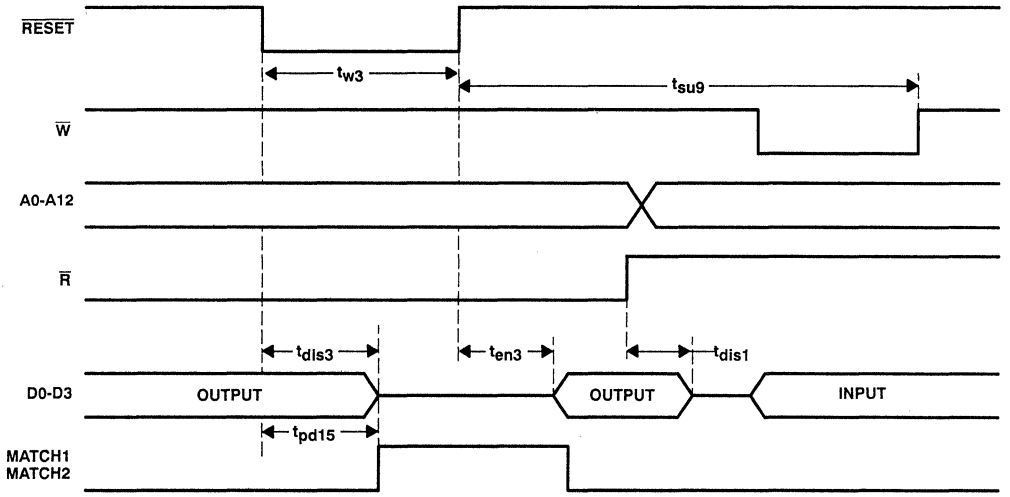


FIGURE 7. RESET CYCLE TIMING

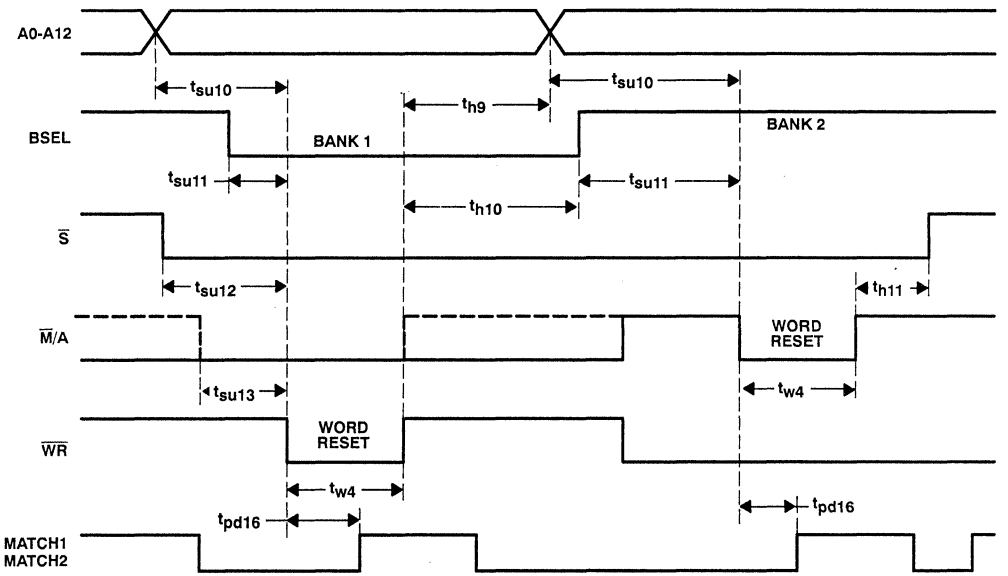


FIGURE 8. WORD RESET TIMING

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

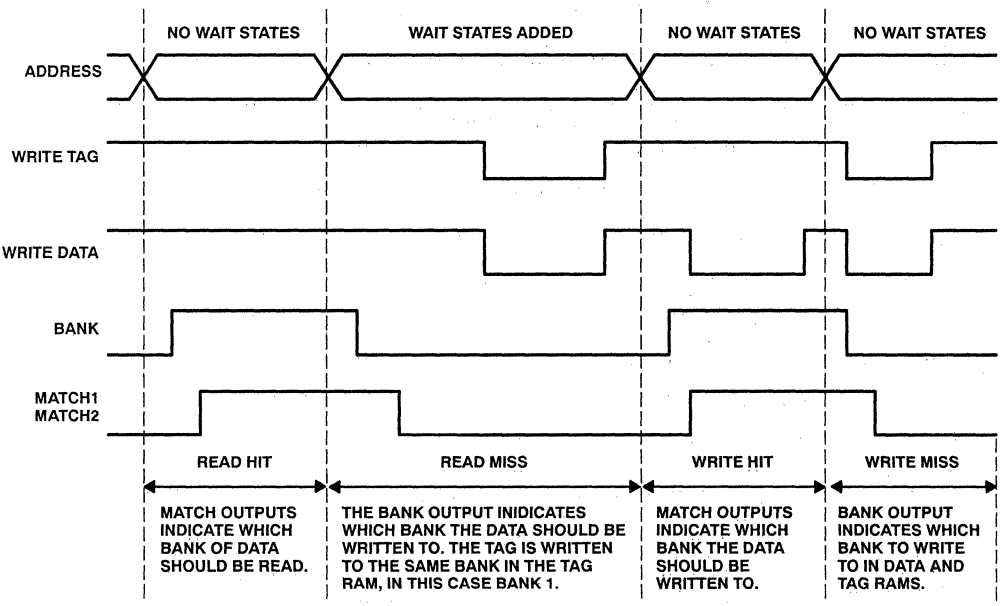


FIGURE 9. CACHE CYCLES

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

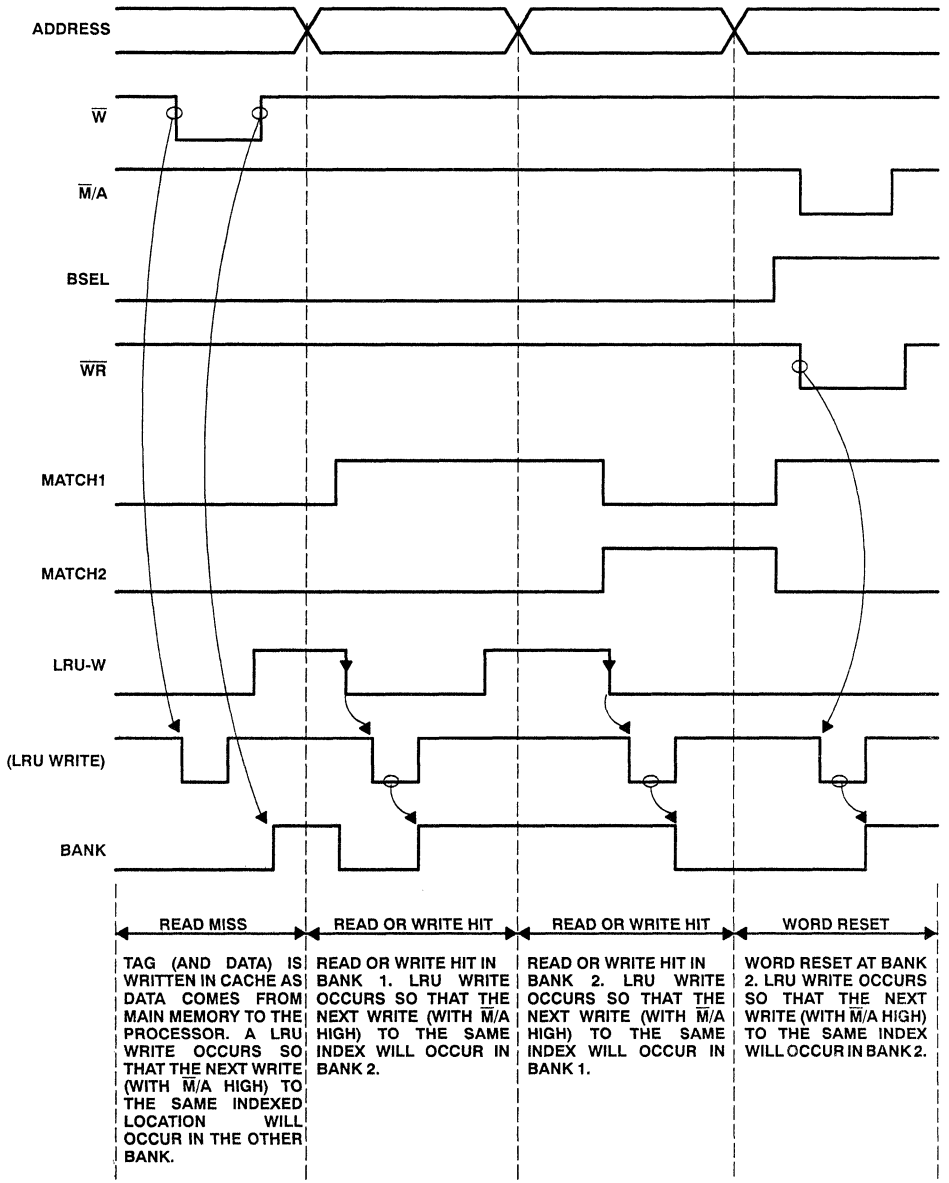
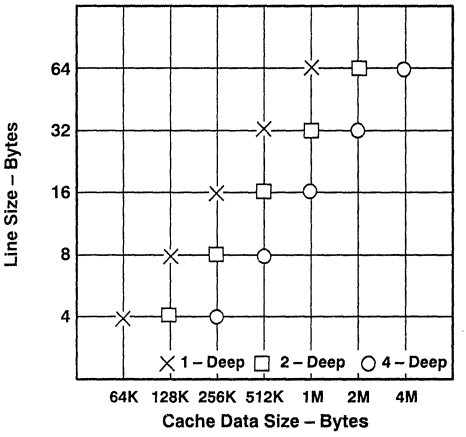


FIGURE 10. LRU WRITE TIMING DIAGRAM

APPLICATION INFORMATION

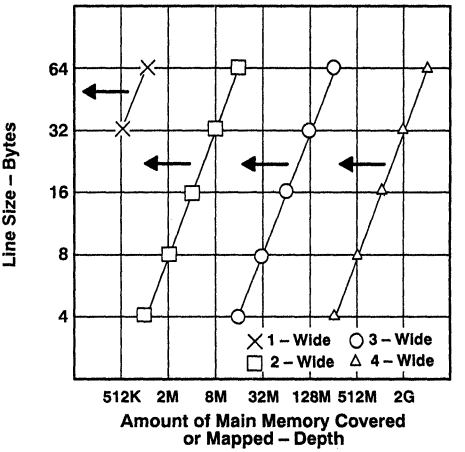
DEPTH CASCADING
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†



† Direct-mapped caches

FIGURE 11

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE‡



‡ One tag/line. Assumes a word length of 32 bits.

FIGURE 12

depth cascading

For four-way caches, each solution shown in Figure 11 is moved to the right one increment doubling the cache size and the number of devices used.

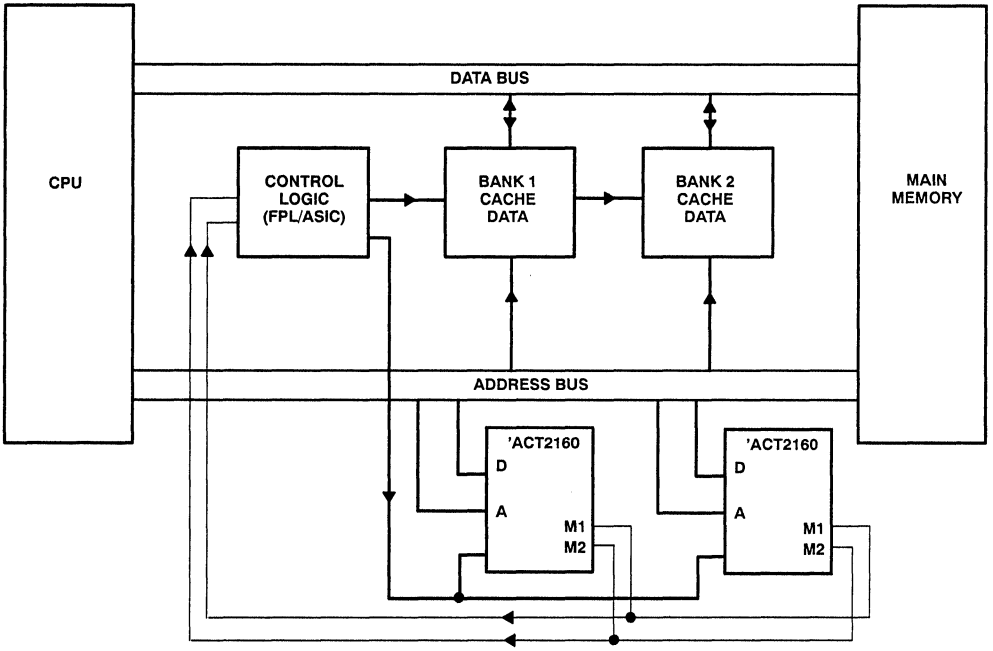
width cascading

Memory coverage assumes one bit used as a valid bit (See Figure 12). Each solution for a given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth memory coverage increases, i.e., two deep — twice as much memory.

usage explanation and example

Figures 11 and 12 provide a quick means for determining if the 'ACT2160 will provide a good solution and the number of devices needed for implementation. For example, a design requires 256K bytes of two-way cache, memory coverage of 256M, and a line size of 16 bytes (a 16-byte line size means each tag location maps four 32-bit words of cached data). From Figure 11, it is determined that one 'ACT2160 deep will provide a 256K byte cache with a 16-byte line size. From Figure 12, it is determined that four 'ACT2160s cascaded in width will map 256M of memory (or as much as 1G). Therefore, one deep by four wide (four 'ACT2160s) are needed to meet the design's requirements.

APPLICATION INFORMATION



CACHE SIZE† (BYTES)	LINE SIZE† (BYTES)
64K	4
128K	8
256K	16
512K	32
1M	64

† Assumes 1 tag per line & 8K of tag depth. The cache size line size relationship shown can be changed by cascading the 'ACT2160 in depth.

FIGURE 13. TWO-WAY CACHE USING THE 'ACT2160

ADVANCE INFORMATION

APPLICATION INFORMATION

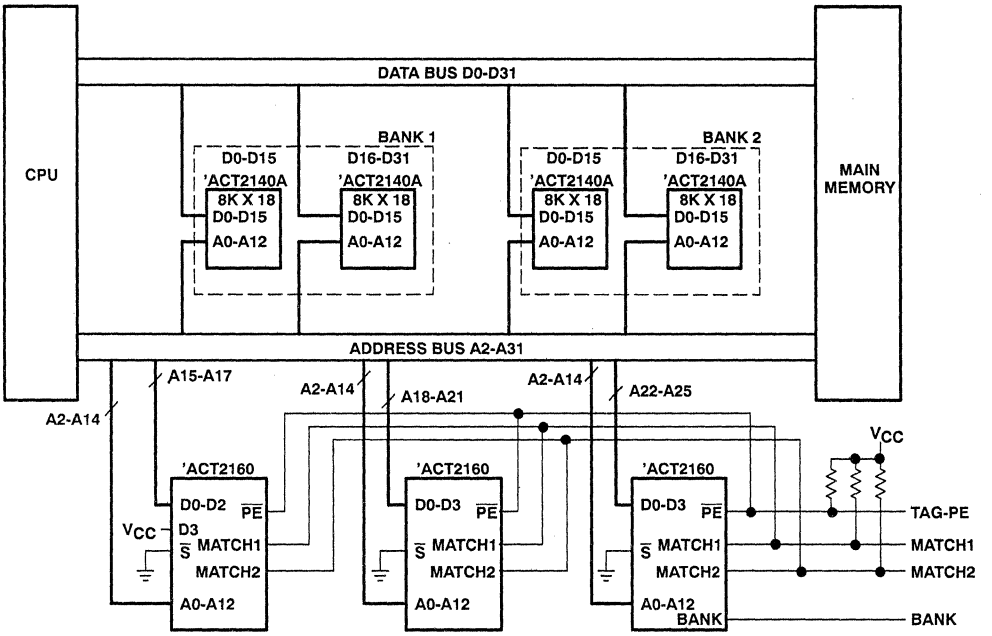


FIGURE 14. 64K BYTE TWO-WAY SET ASSOCIATIVE CACHE, LINE SIZE = 4 BYTES

ADVANCE INFORMATION

APPLICATION INFORMATION

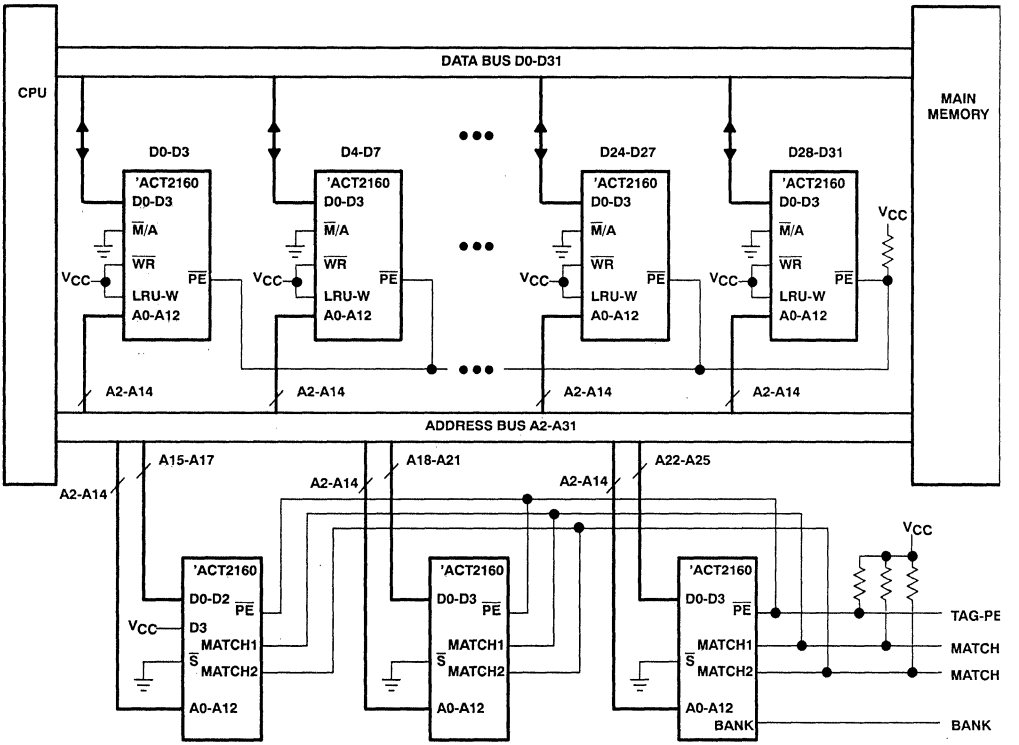


FIGURE 15. 64K BYTE TWO-WAY ASSOCIATIVE CACHE, LINE SIZE = 4 BYTES

ADVANCE INFORMATION

ADVANCE INFORMATION

APPLICATION INFORMATION

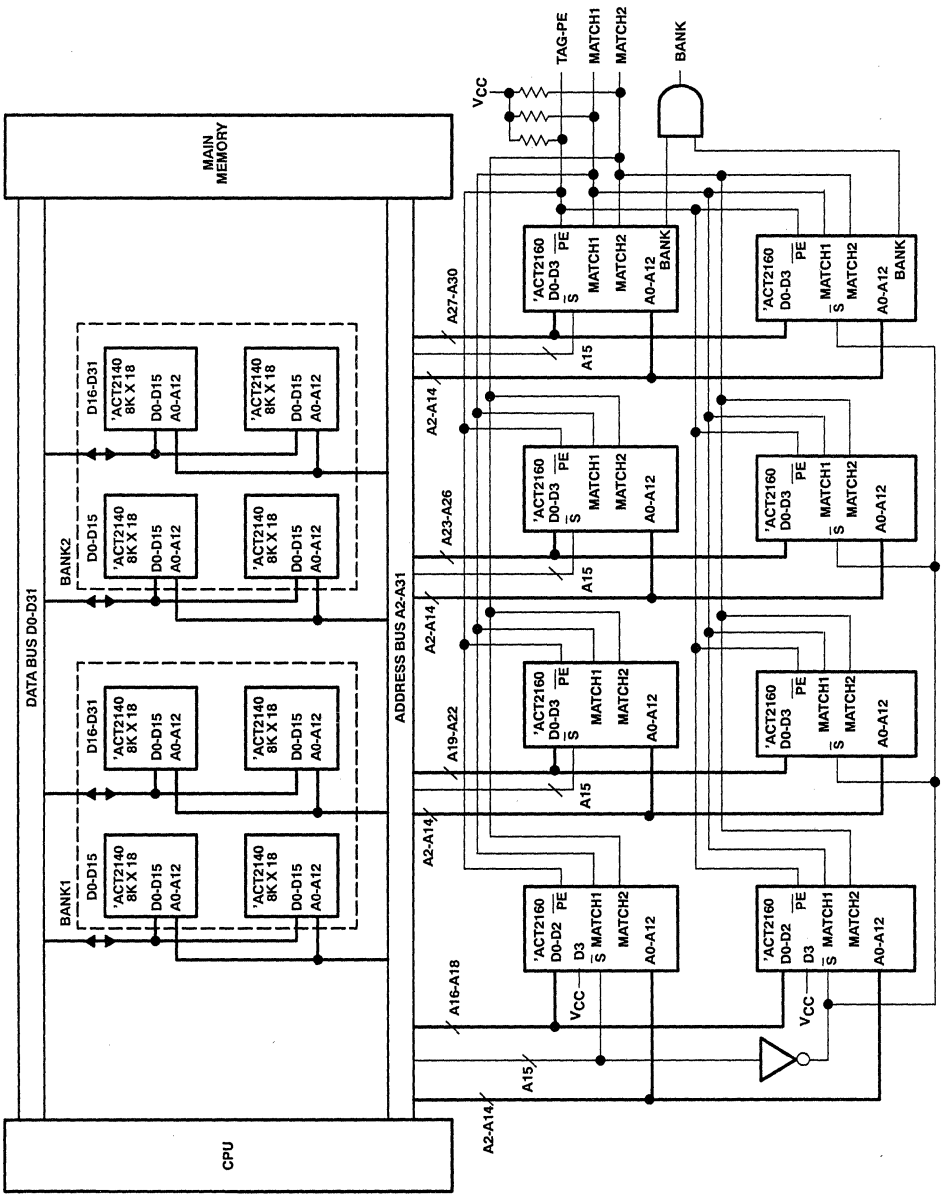


FIGURE 16. 128K BYTE CACHE, LINE SIZE = 4 BYTES

APPLICATION INFORMATION

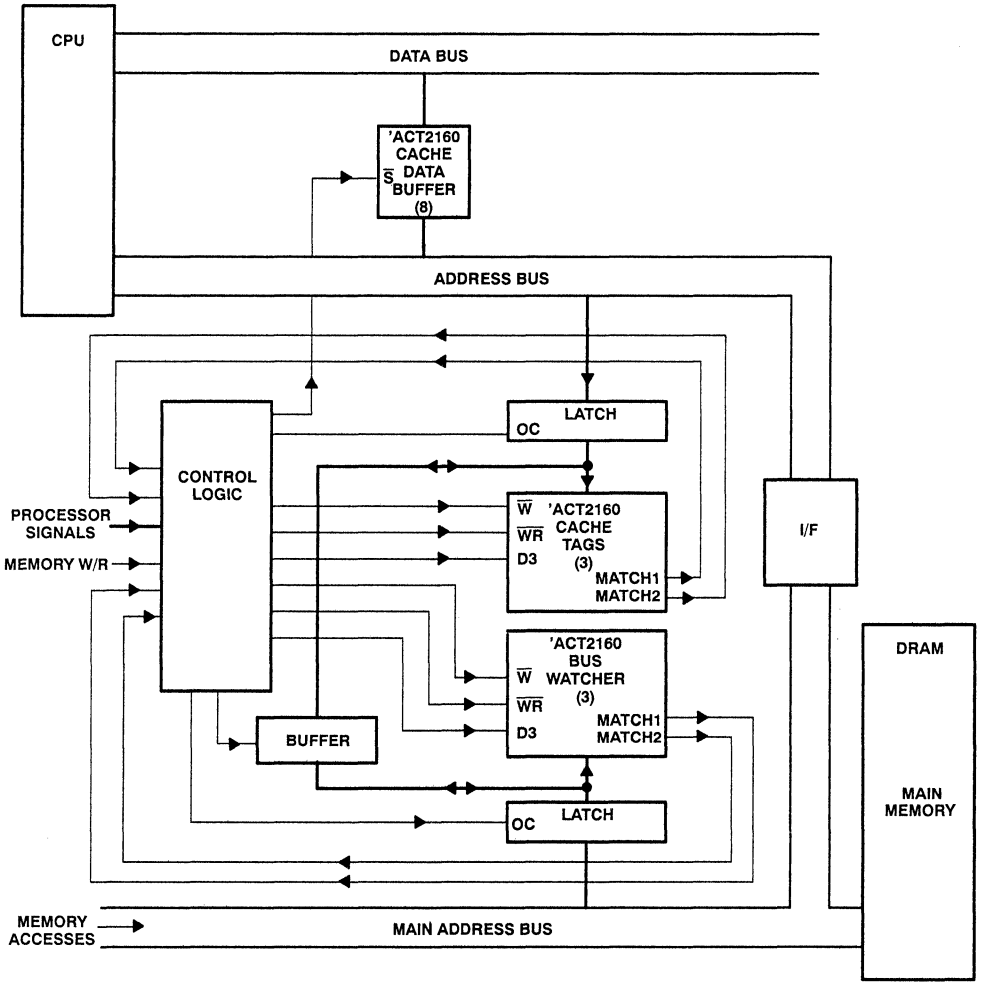


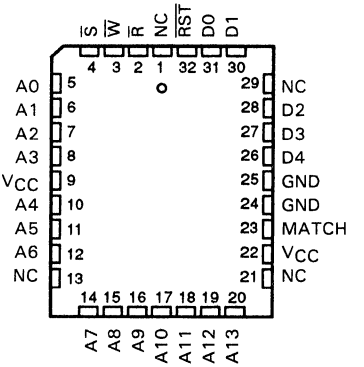
FIGURE 17. BUS WATCHING WITH THE 'ACT2160

ADVANCE INFORMATION

D3298, SEPTEMBER 1989—REVISED JUNE 1990

- **Fast Address to Match Delay**
  20 ns Max — 'ACT2163
  18 ns Max — 'ACT2164
- **Common I/O with Read Feature**
- **On-Chip Address/Data Comparator**
- **Easily Expanded in Depth and Width**
- **'ACT2163 Has Totem-Pole Match Output**
- **'ACT2164 Has Open-Drain Match Output Tested with 75-pF Load**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

FM PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN74ACT2163 and SN74ACT2164 cache address comparators each consists of a high-speed 16K × 5 static RAM array and a 5-bit high-speed comparator. They are fabricated using advanced silicon-gate CMOS technology for high speed and simple interface with bipolar TTL circuits. The 'ACT2163 and 'ACT2164 cache address comparators are easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A13 with the data D0-D4. An equality is indicated by a high level on the MATCH output. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D4 is written in the 5-bit memory addressed by A0-A13.

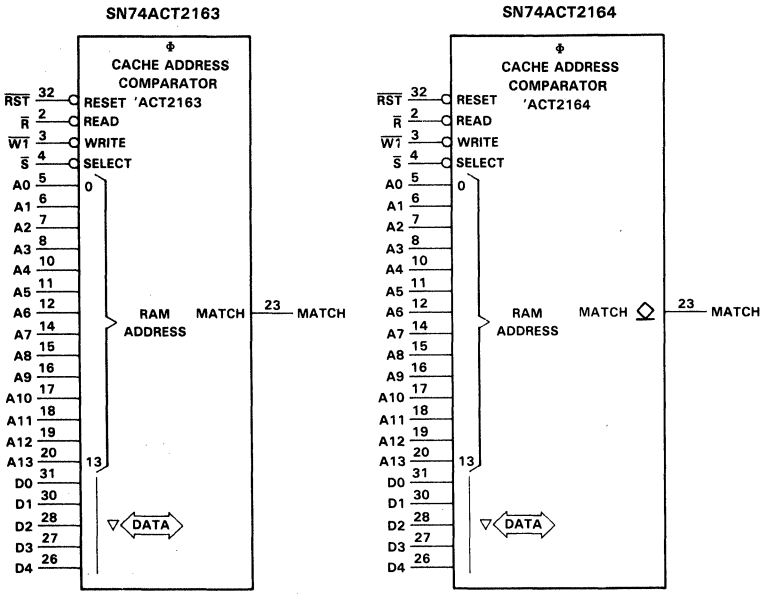
The 'ACT2163 features a totem-pole MATCH output and the 'ACT2164 features an open-drain MATCH output. 'ACT2164 is designed to reduce the address-to-MATCH slow-down normally associated with a capacitively loaded open-drain output and is tested with a high capacitive load.

A read mode is provided with the 'ACT2163 and 'ACT2164, which allows the contents of RAM to be read at the D0-D4 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high.

A reset input is provided for initialization. When $\overline{RST}$ is taken low, all 16K × 5 RAM locations are cleared to zero and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only one bit needs to be tied high regardless of the address width. These cache address comparators operate from a single 5-V supply and are offered in a 32-pin PLCC package.

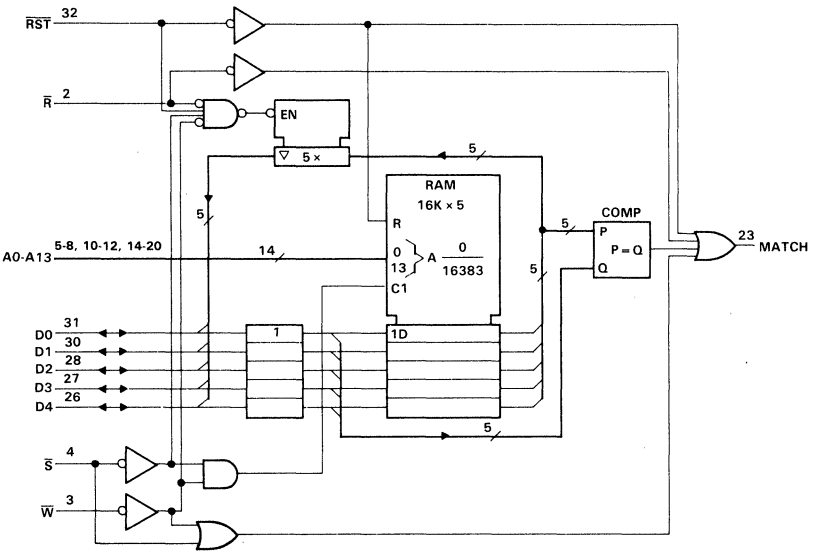
The SN74ACT2163 and SN74ACT2164 are characterized for operation from 0°C to 70°C.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUTS				I/O	OUTPUTS	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{RST}$	D0-D4	MATCH	
L	X	L	H	Input	H	Write
H	L	L	H	Output	H	Read
H	H	L	H	Input	L	Not equal
					H	Equal
H	X	X	L	Hi-Z	H	Memory reset
X	X	H	H	Hi-Z	H	Device disabled

TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	5	Address inputs. Addresses 1 of 16K by 5-bit RAM memory locations. Must be stable for the duration of the write cycle.
A1	6	
A2	7	
A3	8	
A4	10	
A5	11	
A6	12	
A7	14	
A8	15	
A9	16	
A10	17	
A11	18	
A12	19	
A13	20	
D0	31	Data (tag) inputs/outputs. D0-D4 are inputs during the compare and write modes. D0-D4 are outputs during the read mode.
D1	30	
D2	28	
D3	27	
D4	26	
GND	25	Ground
	24	
MATCH	23	When MATCH output is high during a compare cycle, D0-D4 equals the contents of the 5-bit memory location addressed by A0-A13. MATCH is also driven high during deselect, reset, read, and write.
$\overline{R}$	2	Read input. When $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high, addressed data is output to the D0-D4 pins and the MATCH output is forced high.
$\overline{RST}$	32	Reset input. Asynchronously clears entire RAM array to zero and forces MATCH high when $\overline{RST}$ is low.
$\overline{S}$	4	Chip select input. Enables device when $\overline{S}$ is low. Deselects device and forces MATCH high when $\overline{S}$ is high.
V_{CC}	9	Supply voltage
	22	
$\overline{W}$	3	Write control input. Writes D0-D4 into the RAM location addressed by A0-A13 and forces MATCH high when $\overline{W}$ is low. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are high and $\overline{S}$ is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage range, any input . . . . . −1.5 to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}): D0-D4 . . . . . ±25 mA
MATCH . . . . . ±50 mA
Continuous current through V_{CC} or GND pins . . . . . ±200 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (see Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage, MATCH ('ACT2164)				5.25	V
I_{OH}	High-level output current, MATCH ('ACT2163) and DO-D4 outputs				−8	mA
I_{OL}	Low-level output current	D0-D4, MATCH ('ACT2163)			8	mA
		MATCH ('ACT2164)			27	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.5 V). Rise and fall times at the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at the $\overline{\text{RESET}}$ pin is at its minimum high level (2.2 V). In systems with −1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at the $\overline{\text{RESET}}$ pin be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'ACT2163-20			'ACT2164-18			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{OH}	MATCH ('ACT2164)	V_{CC} = 5.25 V, V_{OH} = 5.25 V			10			10	μA
V_{OH}	MATCH ('ACT2164), D0-D4	V_{CC} = 4.75 V, I_{OH} = −8 mA	3.7			3.7			V
V_{OL}	D0-D4	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4			0.4	V
	MATCH (ACT2163)	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4			0.4	
	MATCH (ACT2164)	V_{CC} = 4.75 V, I_{OL} = 27 mA			0.4			0.4	
I_I		V_{CC} = 5.25 V, V_I = 0 to V_{CC}			±5			±5	μA
I_{OZ}		V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{S}$ is low			±10			±10	μA
I_{CC1}	Operating	V_{CC} = 5.25 V, $\overline{RST}$ at 3 V, $\overline{S}$ at 0 V		130	180		130	180	mA
I_{CC2}	Reset	V_{CC} = 5.25 V, $\overline{RST}$ at 0 V, $\overline{S}$ at 0 V		53	80		53	80	mA
I_{CC3}	Deselect	V_{CC} = 5.25 V, $\overline{RST}$ at 3 V, $\overline{S}$ at V_{CC}		100	150		100	150	mA
C_i		f = 1 MHz			5			5	pF
C_o		f = 1 MHz			6			6	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

compare cycle

PARAMETER		'ACT2163-20			'ACT2164-18			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address to MATCH		15	20		14	18	ns
$t_{a(S)}$	Access time from $\overline{S}$ to MATCH		10	15		10	15	ns
$t_{p(D-M)}$	Propagation time, data inputs to MATCH		12	16		12	16	ns
$t_{p(RST-MH)}$	Propagation time, $\overline{RST}$ low to MATCH high		15	20		15	20	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		8	12		8	12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		6	10		6	10	ns
$t_{p(WH-M)}$	Propagation delay, $\overline{W}$ high to MATCH‡		15	20		14	18	ns
$t_{v(A)}$	MATCH valid time after change of address	0			0			ns
$t_{v(D)}$	MATCH valid time after change of data	0			0			ns
$t_{v(S)}$	MATCH valid time (low) after $\overline{S}$ high	0			0			ns

read cycle

PARAMETER		'ACT2163-20			'ACT2164-18			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A-D)}$	Read access time from address to D0-D4		19	25		19	25	ns
$t_{en(S-D)}$	Enable time from $\overline{S}$ low to D0-D4		12	18		12	18	ns
$t_{en(R-D)}$	Enable time, $\overline{R}$ low to D0-D4		9	14		9	14	ns
t_{dis}	D0-D4 output disable time from $\overline{R}$, $\overline{S}$, or $\overline{W}$		8	12		8	12	ns
$t_{p(R-MH)}$	Propagation time, $\overline{R}$ low to MATCH high		8	12		8	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The MATCH output will glitch at the end of a write cycle after $\overline{W}$ returns high. This spec indicates when the MATCH output is stable after $\overline{W}$ returns high. This specification assumes that the address and/or data inputs are not changed immediately after $\overline{W}$ goes high.

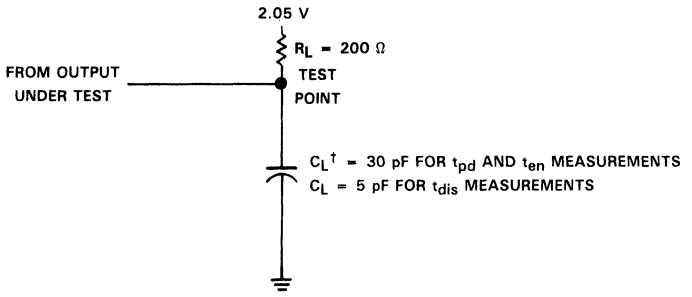
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		'ACT2163-20			'ACT2164-18			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{w(RSTL)}$	Pulse duration, $\overline{RST}$ low	80			80			ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	12			12			ns
$t_{su(A)}$	Setup time, address before $\overline{W}$ low	0			0			ns
$t_{su(D)}$	Setup time, data before $\overline{W}$ high	10			10			ns
$t_{su(S)}$	Setup time, $\overline{S}$ low before $\overline{W}$ high	10			10			ns
$t_{su(RST)}$	Setup time, $\overline{RST}$ inactive before $\overline{W}$ high	20			20			ns
$t_{h(A)}$	Hold time, address after $\overline{W}$ high	2			2			ns
$t_{h(WH-D)}$	Hold time, data after $\overline{W}$ high	0			0			ns
$t_{h(WL-D)}$	Hold time, data after $\overline{W}$ low with MATCH high (see Note 3)	10			10			ns
$t_{h(S)}$	Hold $\overline{S}$ low after $\overline{W}$ high	0			0			ns
t_{AVWH}	Address valid to write enable high	12			12			ns

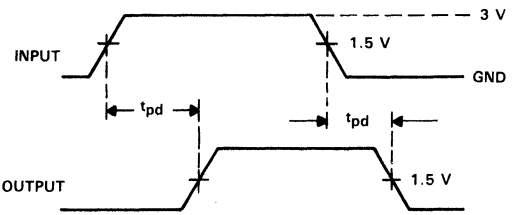
†All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: The purpose of $t_{h(WL-D)}$ is to ensure that when $\overline{W}$ is taken low during a compare cycle with MATCH high, MATCH will remain high without a glitch low. (As shown in the function table, $\overline{W}$ low forces MATCH high).

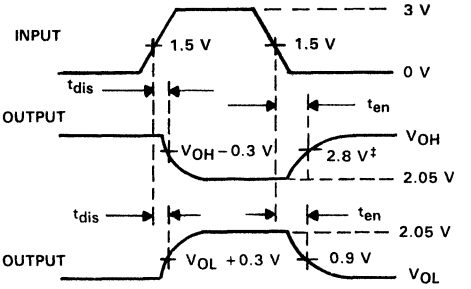
PARAMETER MEASUREMENT INFORMATION



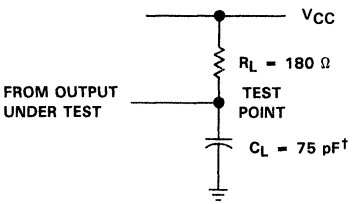
3-STATE AND TOTEM-POLE OUTPUTS LOAD CIRCUIT



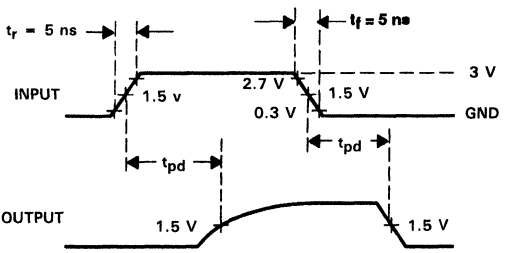
3-STATE AND TOTEM-POLE OUTPUTS PROPAGATION-TIME VOLTAGE WAVEFORMS



3-STATE OUTPUTS ENABLE/DISABLE VOLTAGE WAVEFORMS



OPEN-DRAIN OUTPUTS LOAD CIRCUITS



OPEN-DRAIN OUTPUTS VOLTAGE WAVEFORMS

†C_L includes probe and test fixture capacitance.
‡V_{OH} = 1.5 V for t_{en}(S – D)

FIGURE 2

PARAMETER MEASUREMENT INFORMATION

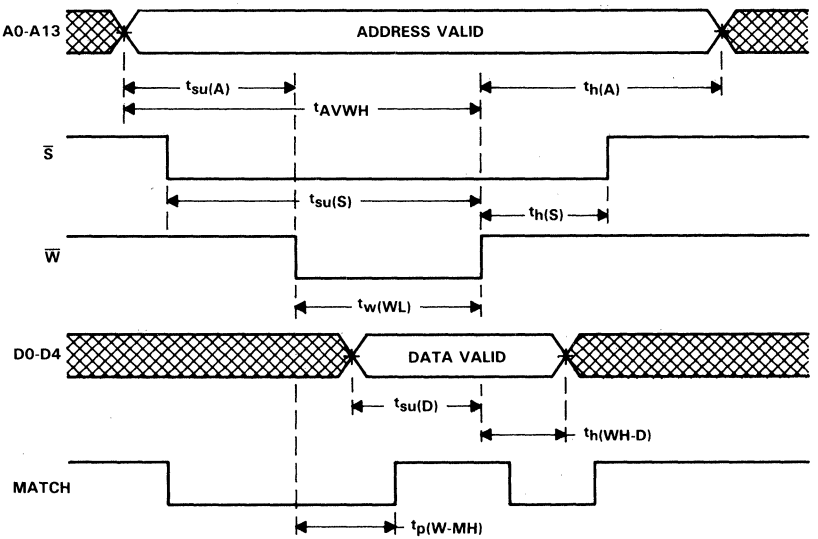


FIGURE 3. WRITE CYCLE TIMING

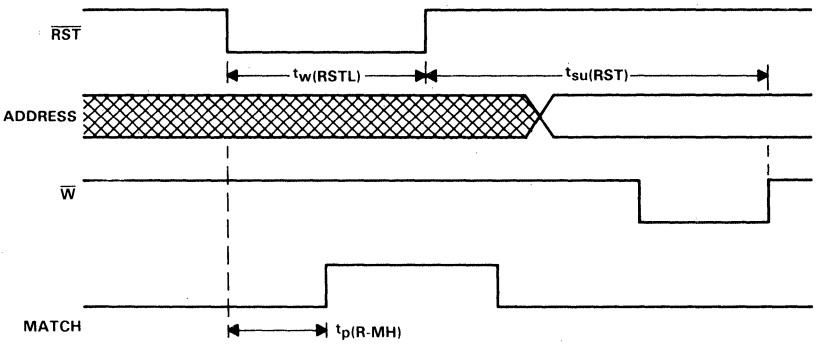


FIGURE 4. RESET CYCLE TIMING

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PARAMETER MEASUREMENT INFORMATION

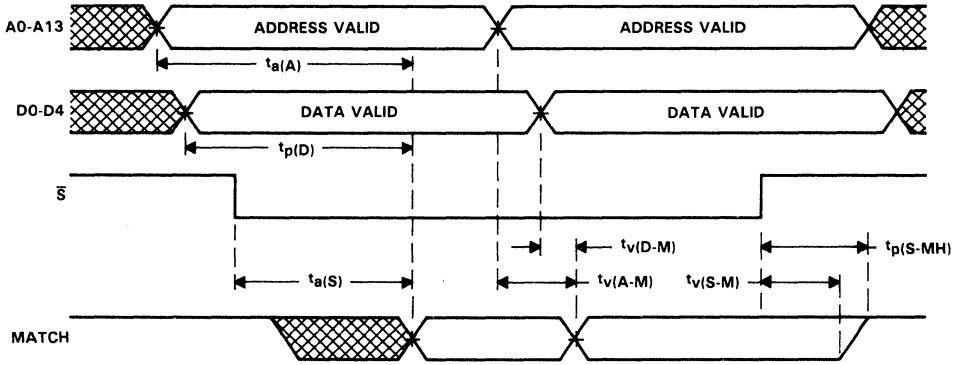


FIGURE 5. COMPARE CYCLE TIMING

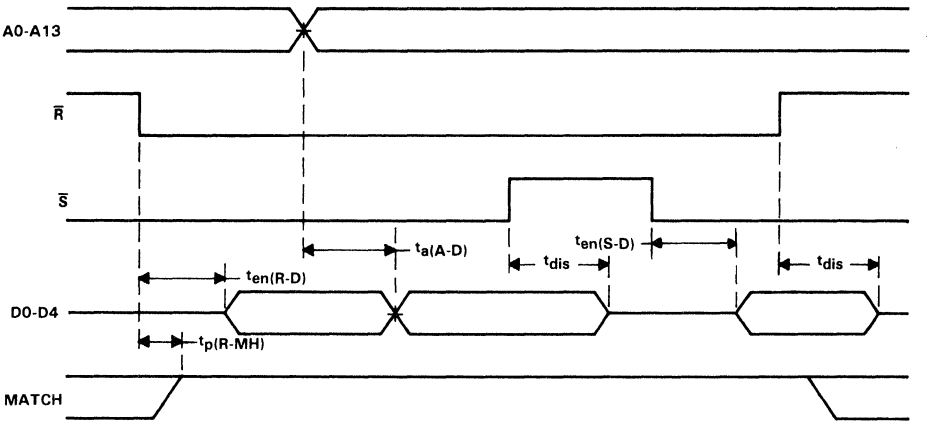
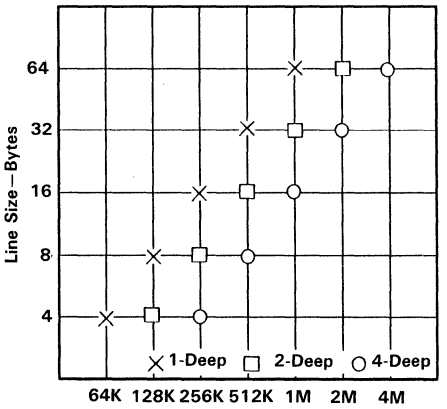


FIGURE 6. READ CYCLE TIMING

APPLICATION INFORMATION

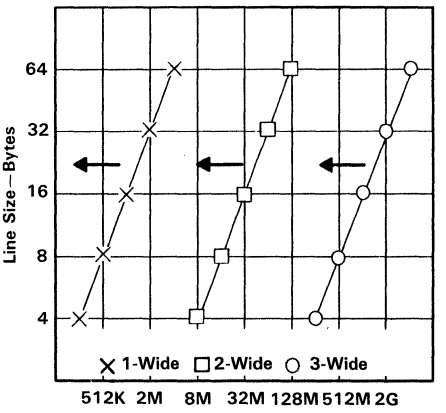
DEPTH CASCADING
NUMBER OF DEVICES
vs
LINE SIZE†



†Direct-Mapped Caches

FIGURE 7

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE†



†One Tag/line, Assumes a word length of 32 Bits

FIGURE 8

depth cascading

For two-way caches, each solution shown is moved to the right one increment doubling the cache size and the number of devices used. Four-way cache designs using the 'ACT2163 or 'ACT2164 will quadruple each solution shown within Figure 7.

width cascading

Memory coverage assumes one bit used as a valid bit. Each solution for a given line size (See Figure 8) can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth, memory coverage increases; i.e., two deep—twice as much memory.

usage explanation and example

Figures 7 and 8 provide a quick means for determining if the 'ACT2163 or 'ACT2164 will provide a good solution and the number of devices needed for implementation. For example, a design requires 256K bytes of direct mapped cache, memory coverage of 256M, and a line size of 16 bytes, a 16-byte line size means each tag location maps four 32-bit words of cached data. From Figure 7, it is determined that one 'ACT2163 or 'ACT2164 will provide a 256K byte cache with a 16-byte line size. From Figure 8, it is determined that three 'ACT2163s or 'ACT2164s cascaded in width will map 256M of memory (or as much as 1G). Therefore, one deep by three wide or three 'ACT2163s or 'ACT2164s are needed to meet the design requirements.

APPLICATION INFORMATION

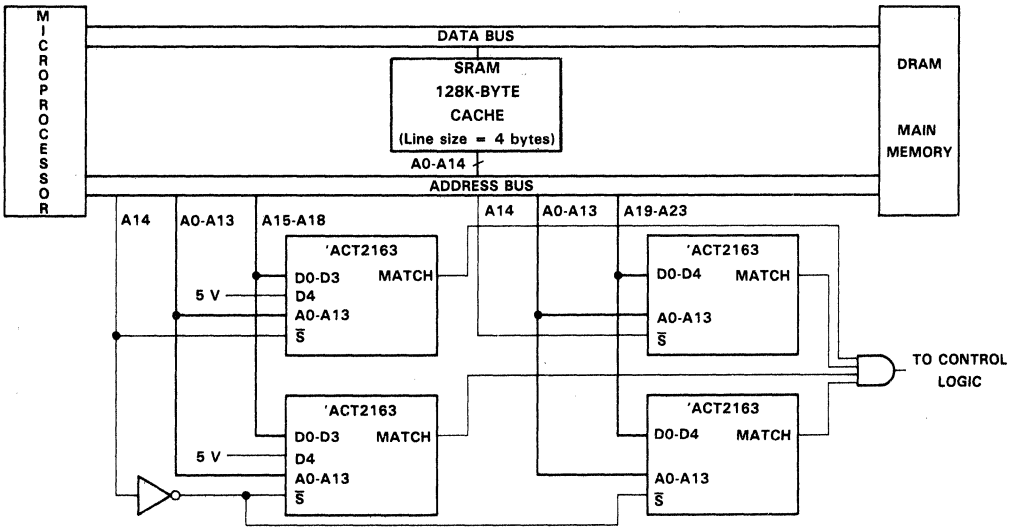
cascading the 'ACT2163 and 'ACT2164

The 'ACT2163 and 'ACT2164 are easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A13 inputs of each device with the same index and applying the additional address bits to the D0-D4 inputs. The select ($\overline{S}$) input allows these devices to be cascaded in depth. When a device is deselected, MATCH is driven high. It should be noted that a decoder can be used to drive the select input since the propagation delay from select to match is much faster than from address to match. Figure 9 shows the 'ACT2163 cascaded. The 'ACT2164 open-drain MATCH output is designed to reduce the typical RC slow down time normally associated with open-drain outputs. This feature reduces additional delay in the critical speed paths normally caused when cascading this type of device.

cache coherency through bus watching

When implementing cache designs, the problem of cache coherency is always a concern. One solution to this problem is to implement bus watching using the 'ACT2163 or 'ACT2164. By storing the same tags in the bus watcher RAM as is stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 10 shows a possible bus-watcher implementation.

APPLICATION INFORMATION



NOTE: In a similar manner, additional 'ACT2163s can be used for greater width and/or depth. When cascading the 'ACT2164, the AND gate in this figure is replaced by a pullup resistor and all MATCH outputs are wire-tied together.

FIGURE 9. CASCADING THE 'ACT2163

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APPLICATION INFORMATION

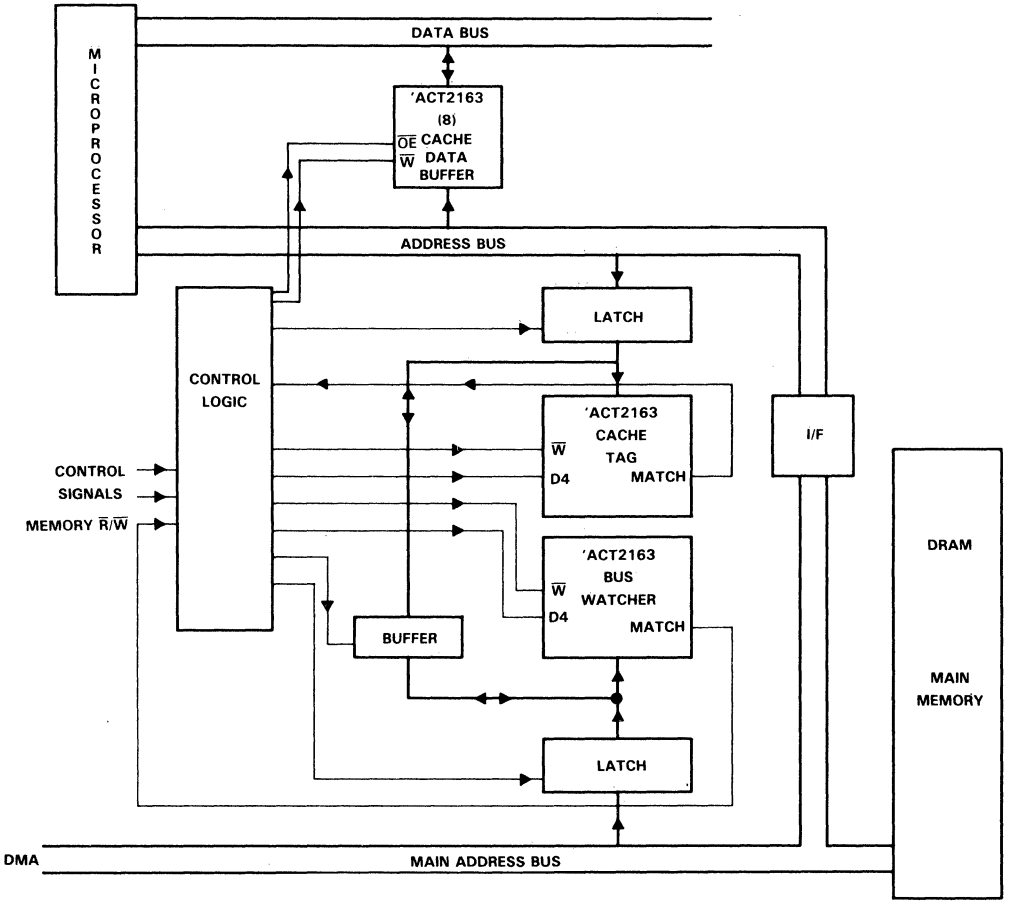
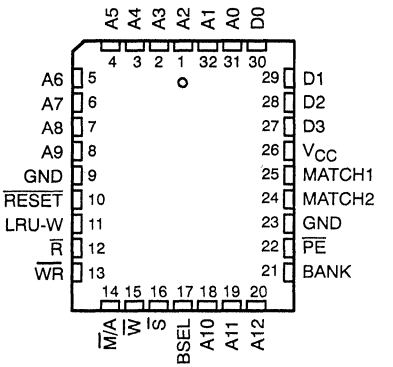


FIGURE 10. BUS WATCHING USING THE 'ACT2163

D3512, JUNE 1990

- **Fast Address to Match Time . . . 12 ns Max**
- **2-Way Architecture Significantly Improves Hit Rate**
- **Implements LRU Replacement Algorithm**
- **Useful for Bus Watching**
- **On-Chip Parity Generator and Checker**
- **Easily Expandable in Depth and Width**
- **Reliable Advanced BiCMOS Technology**
- **Fully TTL Compatible**

FM PACKAGE
(TOP VIEW)



description

The SN74BCT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8K x 5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74BCT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74BCT2160 is fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74BCT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'BCT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

PRODUCT PREVIEW

address comparison

The 'BCT2160 compares the contents of the memory location addressed by A0-A12 with the address bits (or tag) applied at D0-D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the 'BCT2160

The 'BCT2160 has been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transistion at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. The manual/auto ($\overline{M}$/A) input on the 'BCT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low. The BANK output is latched when $\overline{W}$ goes low. This latch will return transparent when $\overline{W}$ returns high. When $\overline{W}$ is low the D0-D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output will indicate which bank the data should be written to. If BANK is low, bank 1 should be written to. If BANK is high, bank 2 should be written to. When writing a tag with $\overline{M}$/A low, the BANK output will not indicate which bank is being selected by the BSEL input. BANK is the output of the internal 8K x 1 LRU RAM. When a write hit occurs, the match outputs will indicate which data bank to write to.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'BCT2160 contains an 8K x 1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0-D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0-D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

With a match output high indicating a match, the LRU RAM will also be updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address with $\overline{M}$/A high will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address with $\overline{M}$/A high will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur. When a word reset occurs, the addressed LRU bit is updated so that the next write to that address will be to the reset (invalidated) location.

parity generation and checking

The 'BCT2160 contains parity generation and checking circuitry. When the $\overline{PE}$ output goes low, a parity error exists in one of the two tag RAMs.

During a write cycle, address bits or data on D0-D3 plus generated odd parity are written into the 5-bit memory location in either bank 1 or bank 2 that is addressed by A0-A12. Also during write, a parity error may be forced for diagnostic purposes by holding the $\overline{R}$ input low. The addressed parity bits are included in the comparator circuitry of the 'BCT2160 so if a parity error occurs, the corresponding match output will be forced low. The bank written to is selected automatically or manually via the BSEL input depending on the state of the $\overline{M}$/A input. The LRU bit is not parity protected. The BANK outputs of the 'BCT2160s that are cascaded in width could be externally exclusive ORed to provide protection for the LRU bits.

operation as a data RAM

The 'BCT2160 can be used as a two-way 8K x 4 data RAM with parity generation and checking. By tying the manual/auto ($\overline{M}$/A) pin low, the BSEL input can be used to select which bank is being written to or read from. Through the use of the select pin, the 'BCT2160 can be cascaded for a deeper data RAM. Inputs $\overline{WR}$ and LRU-W should be tied high when using the 'BCT2160 as a data RAM.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all three 8K RAM locations are cleared to zero (with valid parity) and the MATCH1 and MATCH2 outputs are forced high. If a D0-D3 input of zero is compared to any memory location that has not been written into since reset, MATCH1 and/or MATCH2 will be high indicating that D0-D3 plus generated parity is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width. After reset, $\overline{PE}$ will be high for every addressed memory location indicating no parity error in the RAM data. After power-up, the 'BCT2160 must be initialized by resetting the device to ensure that all memory locations are at a known state. The 'BCT2160 could also be initialized by writing to every memory location (both banks).

single-entry invalidation

In cache tag systems, it is often necessary to invalidate a tag memory location when data in the cache becomes inconsistent with the data in main memory or in additional caches. The word-reset function on the 'BCT2160 allows any addressed memory location to be cleared to zero with valid parity by taking the word reset pin ($\overline{WR}$) low. By tying one of the D0-D3 input pins high, that particular bit can be used as a valid bit. Whenever D0-D3 is compared to a memory location cleared by $\overline{WR}$ (or by the master $\overline{RESET}$), a miss will occur. If a D0-D3 input pin is not tied high, a false match will occur whenever a D0-D3 of zero is compared to a reset location. Word reset is independent of the input at the D0-D3 pins. The $\overline{M}$/A input must be low for a word reset to occur when $\overline{WR}$ is taken low. Word reset can also be accomplished by holding $\overline{WR}$ low and taking $\overline{M}$/A low to reset the addressed location. At the same time that an addressed location is reset, the addressed LRU bit is updated so that the next write to the same address with $\overline{M}$/A high will be to the reset location. Input BSEL determines which bank $\overline{WR}$ affects. When cascading in width, all devices must receive the word-reset pulse for proper LRU RAM update.

PRODUCT PREVIEW

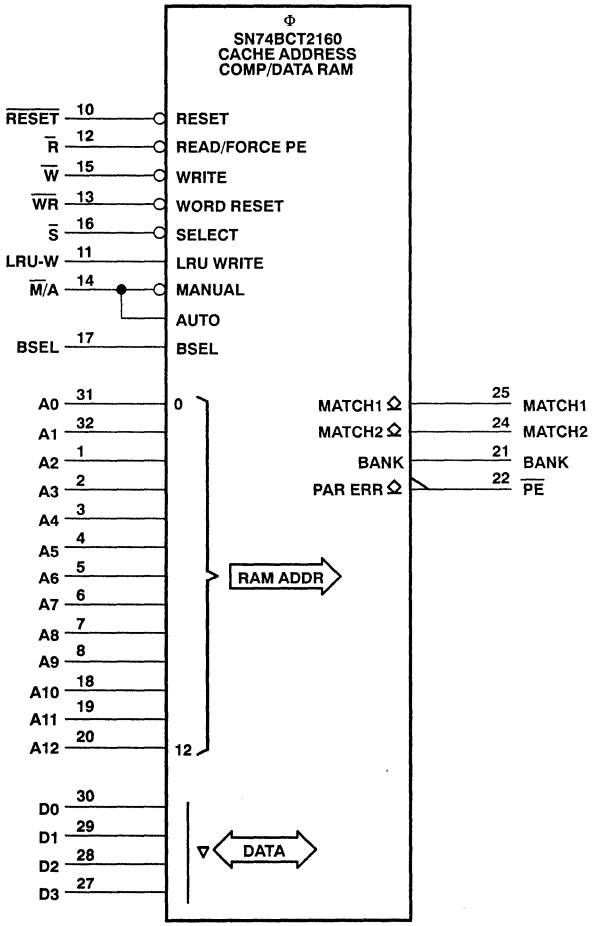
cascading the 'BCT2160

The 'BCT2160 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0-A12 inputs of each device with the same index and applying the additional address bits to the D0-D3 inputs. The select ($\overline{S}$) input allows this device to be easily cascaded in depth. When a device is deselected, the MATCH1 and MATCH2 outputs are driven high. This allows the match outputs to be wire tied or gated together when cascading in depth. A decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire-ANDing and must be wired-ANDed in the width direction to ensure proper LRU update.

cache coherency through bus watching

When implementing cache designs, cache coherency is usually a concern. A solution to this problem is to implement bus watching using the 'BCT2160. By storing the same tags in the bus watcher RAM as are stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation.

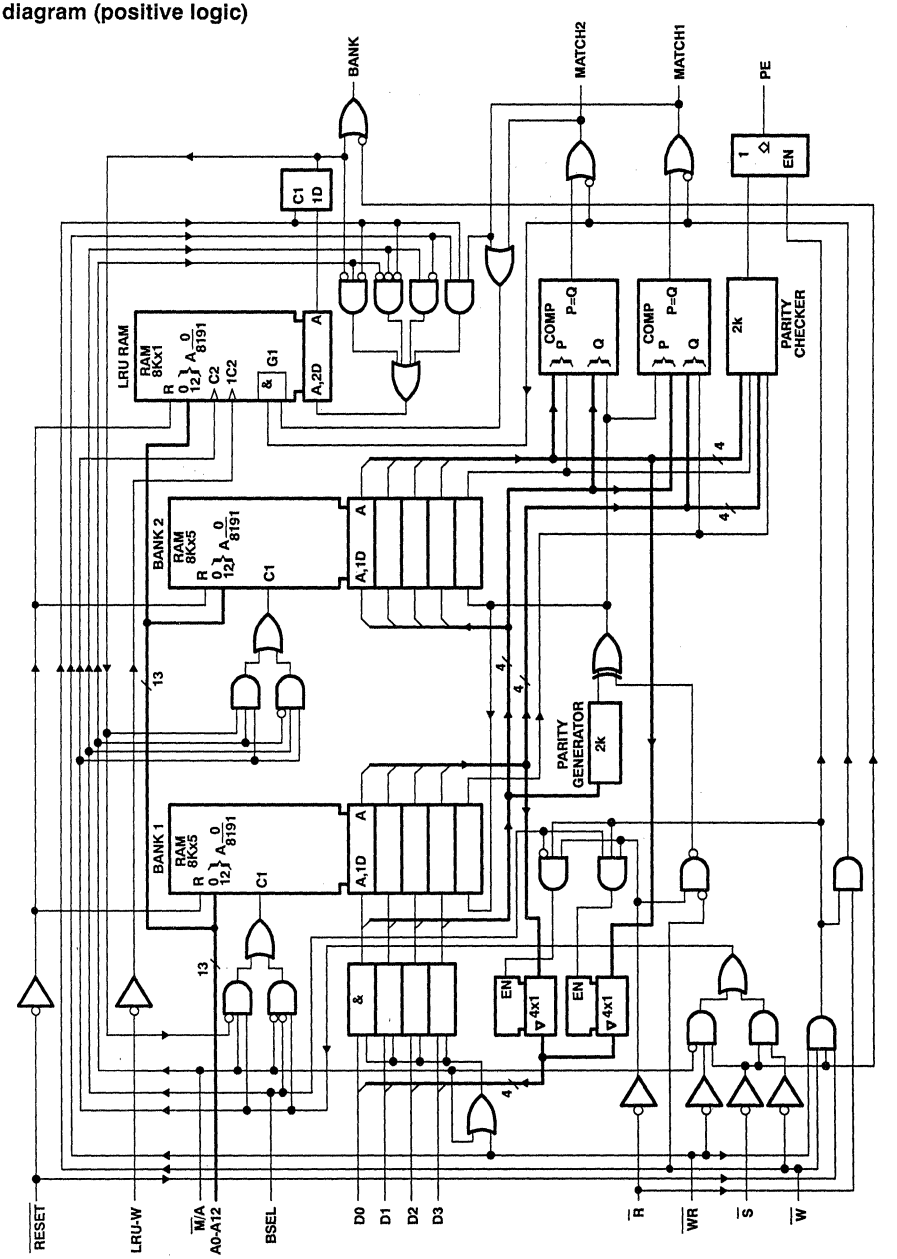
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

PRODUCT PREVIEW

logic diagram (positive logic)



Terminal Functions

PIN NAME	DESCRIPTION
A0-A12	Address inputs. Addresses a memory location in each of the three 8K RAM arrays. Address must be stable for the duration of the write cycle.
BSEL	Bank Select input. This input is used in conjunction with the manual/auto, read and word reset functions.When BSEL is low, bank 1 is selected. When BSEL is taken high, bank 2 is selected. When $\overline{M}$/A is high, the BSEL input does not affect writing.
BANK	Bank output. The BANK output is used during a write to indicate which bank D0-D3 is being written into when $\overline{M}$/A is high. BANK is low for bank 1 and high for bank 2. BANK is forced high during reset and deselect. BANK is used to indicate which cache SRAM bank the system data should be written into. When $\overline{W}$ is taken low, the output of the LRU RAM is latched causing BANK to remain stable. When $\overline{W}$ returns high, the latch returns transparent and the BANK output will switch if the LRU bit was changed. BANK is a totem-pole output.
D0-D3	Data (tag) inputs and outputs. Provides input to RAM bank 1 or bank 2 depending on the state of the $\overline{S}$, $\overline{W}$, BSEL, $\overline{M}$/A, and $\overline{WR}$ pins. When in the compare mode, D0-D3 plus generated parity are compared to the addressed 5-bit memory location in bank 1 and bank 2. D0-D3 also function as outputs (see the $\overline{R}$ pin description).
LRU-W	Least Recently Used Write timing signal. In the compare mode, a falling edge on LRU-W will initiate an LRU write pulse if MATCH1 and/or MATCH2 are high. If a falling edge at LRU-W occurs before MATCH1 or MATCH2 are valid based on t_{pd1} and t_{su1}, the LRU write may not occur or a false LRU write could occur. LRU-W will only initiate a LRU write pulse on a falling edge. LRU-W has no effect during any other mode of operation.
$\overline{M}$/A	Manual/Auto input. The $\overline{M}$/A input determines the bank select mode for writing data. When $\overline{M}$/A is low, the bank to be written into is selected manually via the BSEL input. When the $\overline{M}$/A input is high, the bank selection is done automatically. An internal 8K x 1 RAM is used to keep track of the bank to be written into using the least recently used (LRU) replacement algorithm. After the device is reset, the first write is into bank 1. The next time data is written to the same address, it will be stored in bank 2. Successive writes to the same address automatically alternate between bank 1 and bank 2. $\overline{M}$/A can also be used to perform the word reset function. With $\overline{WR}$ low, the addressed location in the selected bank will be reset when $\overline{M}$/A is taken low.
MATCH1 MATCH2	Match outputs. When MATCH1 or MATCH2 are high during a compare cycle, D0-D3 plus generated parity equal the contents of one of two memory locations addressed by A0-A12. MATCH1 is high when D0-D3 matches D0-D3 stored in bank 1. MATCH2 is high when D0-D3 matches D0-D3 stored in bank 2. The match outputs are high during deselect, write, read, word reset, and reset. The logic level at the match outputs is fed back to the internal LRU circuitry. If a match output is high indicating a match when LRU-W is taken low, the LRU bit is adjusted so that the next write into that address will be into the other bank (LRU concept). If a match occurs with both banks (MATCH1 and MATCH2 high) and LRU-W is taken low, bank 2 will be written into when $\overline{M}$/A is low and bank 1 will be written into when $\overline{M}$/A is high. Since this device features open-drain match outputs, an external pullup resistor of 180 Ω minimum is required. If a parity error is present in bank 1 or bank 2 during compare, the corresponding match output will be forced low.
$\overline{PE}$	Parity Error output. During compare cycles, a low level at $\overline{PE}$ indicates a parity error in one of the 8K X 5 RAMs. A parity error will force the corresponding match output low. $\overline{PE}$ is an open-drain output and an external pullup resistor is required. $\overline{PE}$ is disabled during write, reset, word reset, and deselect.
$\overline{R}$	Read input. When $\overline{R}$ is low and the device is selected, D0-D3 are enabled as outputs. The output data (tag) is determined by A0-A12 and the BSEL input. Outputs D0-D3 are disabled during write, word reset, reset, deselect, and when $\overline{R}$ is high. During write cycles, a parity error can be forced into the memory location addressed by A0-A12 of the selected bank when $\overline{R}$ is taken low.
$\overline{RESET}$	Reset input. Asynchronously clears all three RAM arrays to zero with valid parity independent of the select pin when $\overline{RESET}$ is low. By tying a single data input high, a false match will not occur when a tag of zero is applied after initialization.
$\overline{S}$	Chip select input. Enables device when $\overline{S}$ is low. When $\overline{S}$ is high, MATCH1 and MATCH2 are forced high. $\overline{PE}$ and D0-D3 are disabled when $\overline{S}$ is high and BANK is forced high.
$\overline{WR}$	Word Reset input. The $\overline{WR}$ input allows any addressed memory location to be cleared to zero with valid parity. This is achieved by taking $\overline{WR}$ low while in the manual mode ($\overline{M}$/A low). The desired bank is selected using the BSEL input. When $\overline{WR}$ is asserted, the addressed LRU bit is adjusted so that the next write to that address (with $\overline{M}$/A high) is into the reset memory location. By tying a single D0-D3 input high, this bit will act as a valid bit assuring that a false match will not occur with a reset memory location.
$\overline{W}$	Write control input. When the device is selected and $\overline{W}$ is low, D0-D3 and generated parity are written into the addressed memory location in either bank 1 or bank 2. The RAM bank to be written into can be selected automatically or manually depending on the $\overline{M}$/A input.

FUNCTION TABLES

write mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK†	D0-D3	
↓	H	L	L	L	H	H	H	H	H	L‡	Input	Write into bank 1
↓	H	L	L	H	H	H	H	H	H	L‡	Input	Write into bank 2
↓	H	L	H	X	H	X	H	H	H	H or L‡	Input	LRU write (bank 1 or 2)
↓	L	L	L	L	H	H	H	H	H	L‡	Input	Write parity error into bank 1
↓	L	L	L	H	H	H	H	H	H	L‡	Input	Write parity error into bank 2
↓	L	L	H	X	H	H	H	H	H	H or L‡	Input	Write parity error (LRU)
↓	H	L	L	X	H	L§	H	H	H	L§	Hi-Z	Write zero into selected bank

read mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
H	L	L	X	L	H	H	H	H	H	H or L	Output	Read bank 1
H	L	L	X	H	H	H	H	H	H	H or L	Output	Read bank 2
H	L	L	X	X	H	H	H	H	L	H or L	Output	Parity error in bank 1 or 2
H	H	L	X	X	H	H	H or L	H or L	EN	H or L	Hi-Z	Disable/compare

compare mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
							H	L	H	H or L		Match bank 1, miss bank 2
							L	H	H	H or L		Match bank 2, miss bank 1
H	H	L	X	X	H	H	H	H	H	H or L		Match bank 1 and 2
				or			L	L	H	H or L	Input	Miss bank 1 and 2
H	H	L	H	X	H	X	L	L	L	H or L		Parity error bank unknown
							L	H	L	H or L		Parity error bank 1, match bank 2
							H	L	L	H or L		Parity error bank 2, match bank 1

reset, word reset, and deselect mode

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0-D3	
H	X	L	X	X	L	X	H	H	H	L	Hi-Z	Memory reset-selected
H	X	H	X	X	L	X	H	H	H	H	Hi-Z	Memory reset-deselect
H	X	L	L	L	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 1
H	X	L	L	H	H	L	H	H	H	L¶	Hi-Z	Word reset in bank 2
H	X	L	H	X	H	L	H or L	H or L	EN	H or L	Hi-Z	Word reset disabled/compare mode
X	X	H	X	X	H	X	H	H	H	H	Hi-Z	Device disabled

EN denotes enabled, H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined output

† The BANK output is transparent when $\overline{W}$ is high and latched when $\overline{W}$ is low.

‡ When writing with $\overline{M}$/A high, the BANK output indicates which bank D0-D3 is being written into. When writing with $\overline{M}$/A low, the BANK output will be forced low and will not indicate which bank is being written into. After writing with $\overline{M}$/A low, the BANK output will indicate the correct LRU bit state.

§ The state of BANK after $\overline{W}$ and $\overline{M}$/A or $\overline{W}$ and $\overline{WR}$ return high is indeterminate. This operation is not recommended.

¶ The BANK output is forced low during word reset. After a word reset in bank 2, the BANK output will be high.

PRODUCT PREVIEW

FUNCTION TABLES (Continued)

LRU write

$\overline{S}$	$\overline{WR}$	$\overline{W}$	$\overline{M/A}$	BSEL	LRU-W†	MATCH1	MATCH2	QI‡	LRU WRITE	QN§	FUNCTION
L	H	L	H	X	X	H	H	L	YES	H	Write to bank 1, selected by LRU circuitry
L	H	L	H	X	X	H	H	H	YES	L	Write to bank 2, selected by LRU circuitry
L	H	L	L	L	X	H	H	X	YES	H	Write to bank 1, selected by BSEL input
L	H	L	L	H	X	H	H	X	YES	L	Write to bank 2, selected by BSEL input
L	H	H	X	X	↓	H	L	X	YES	H	Match bank 1
L	H	H	X	X	↓	L	H	X	YES	L	Match bank 2
L	X	H	H	X	↓	H	L	X	YES	H	Match bank 1
L	X	H	H	X	↓	L	H	X	YES	L	Match bank 2
L	H	H	L	X	↓	H	H	X	YES	H	Match bank 1 and 2
L	H	H	H	X	↓	H	H	X	YES	L	Match bank 1 and 2
L	L	H	L	L	X	H	H	X	YES	L	Word reset bank 1
L	L	H	L	H	X	H	H	X	YES	H	Word reset bank 2
L	L	H	H	X	X	H	H	X	NO	–	Word reset disabled
H	X	X	X	X	X	H	H	X	NO	–	Device disabled

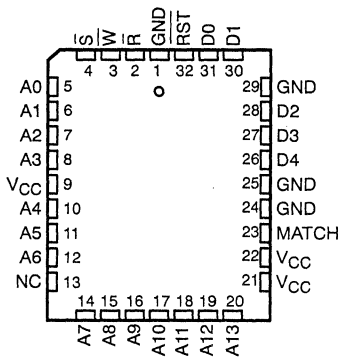
H denotes a high level, L denotes a low level, X denotes a don't care level, – denotes an undetermined level, ↓ denotes the falling edge of the signal.
† LRU-W is falling-edge-triggered and has effect only during the compare mode.
‡ QI is the state of the LRU RAM output before a LRU write occurs.
§ QN is the state of the LRU RAM output after a LRU write occurs.

PRODUCT PREVIEW

D3513, JUNE 1990

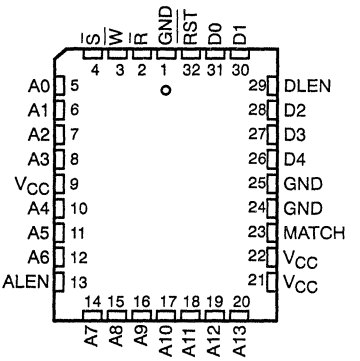
- **Fast Address to MATCH Delay 12-ns Max**
- **'BCT2163 has Totem-Pole Match Output**
- **'BCT2164 and 'BCT2166 have Open-Drain Match Outputs Tested with 75-pF Load**
- **'BCT2166 has Input Latches**
- **Self-Timed Write Circuitry**
- **Common I/O with Read Feature**
- **On-Chip Address/Data Comparator**
- **Easily Expanded in Depth and Width**
- **Reliable Advanced BiCMOS Technology**
- **Fully TTL Compatible**

SN74BCT2163, SN74BCT2164
FM PACKAGE
(TOP VIEW)



NC – No internal connection

SN74BCT2166 . . . FM PACKAGE
(TOP VIEW)



description

The 'BCT2163, 'BCT2164, and 'BCT2166 cache address comparators each consists of a high-speed 16K x 5 static RAM array and a 5-bit high-speed comparator. The 'BCT2166 has latches at the address, data, and select inputs. They are fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. The 'BCT2163, 'BCT2164, and 'BCT2166 address comparators are easily cascaded for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ and $\overline{R}$ are high, the cache address comparator compares the contents of the memory location addressed by A0-A13 with the applied D0-D4. An equality is indicated by a high level on the MATCH output.

The 'BCT2163, 'BCT2164, and 'BCT2166 have been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transition at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. When W is low the D0-D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse. During a write cycle the input levels on D0-D4 are written in the 5-bit memory addressed by A0-A13.

The 'BCT2163 features a totem-pole MATCH output and the 'BCT2164 and 'BCT2166 feature an open-drain MATCH output. The 'BCT2164 and 'BCT2166 are designed to reduce the address-to-MATCH slow-down normally associated with capacitively loaded open-drain outputs and are tested with a high capacitive load.

A read mode is provided with the 'BCT2163, 'BCT2164, and 'BCT2166 which allows the contents of RAM to be read at the D0-D4 pins. The read mode is selected when $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high.

These devices are covered by U.S. Patents for 4,831,625; 4,858,182; 4,884,270; and additional patents pending.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

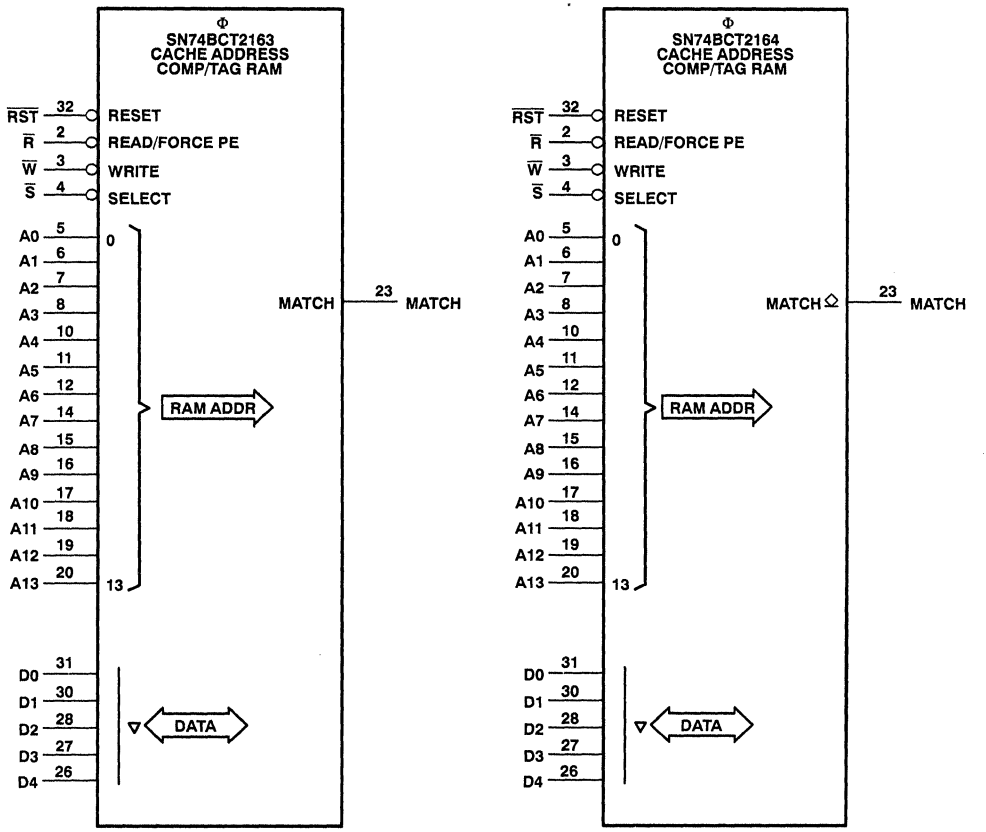
description (continued)

A reset input is provided for initialization. When $\overline{RST}$ is taken low, all 16K x 5 RAM locations are cleared to zero and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction only one bit needs to be tied high regardless of the address width. After power-up, these devices must be initialized by resetting the device to ensure that all memory locations are at a known state. These devices could also be initialized by writing to every memory location.

The 'BCT2166 is equipped with latches at the address, data, and select inputs. Input ALEN controls the latch at the A0-A13 and $\overline{S}$ inputs. DLEN controls the latch at the D0-D4 inputs. The latches are transparent when ALEN and DLEN are high and latched when ALEN and DLEN are low.

The SN74BCT2163, SN74BCT2164, and SN74BCT2166 are characterized for operation from 0°C to 70°C. These cache address comparators operate from a single 5-V supply and are offered in a 32-pin PLCC package.

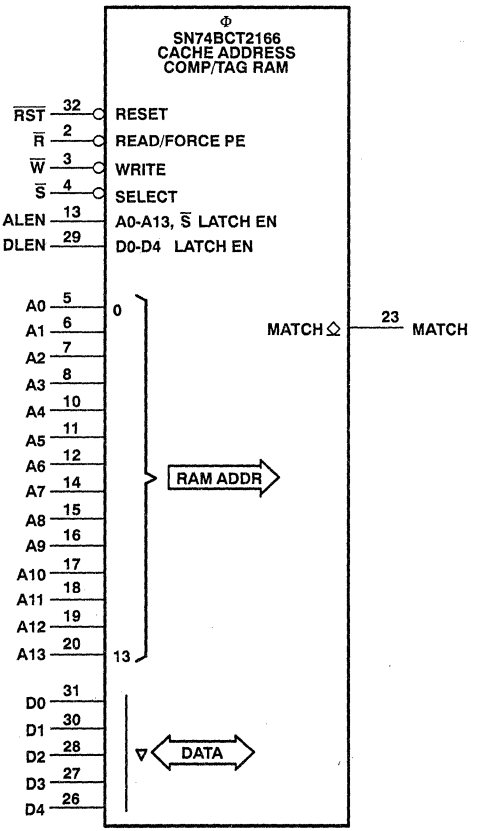
logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984.

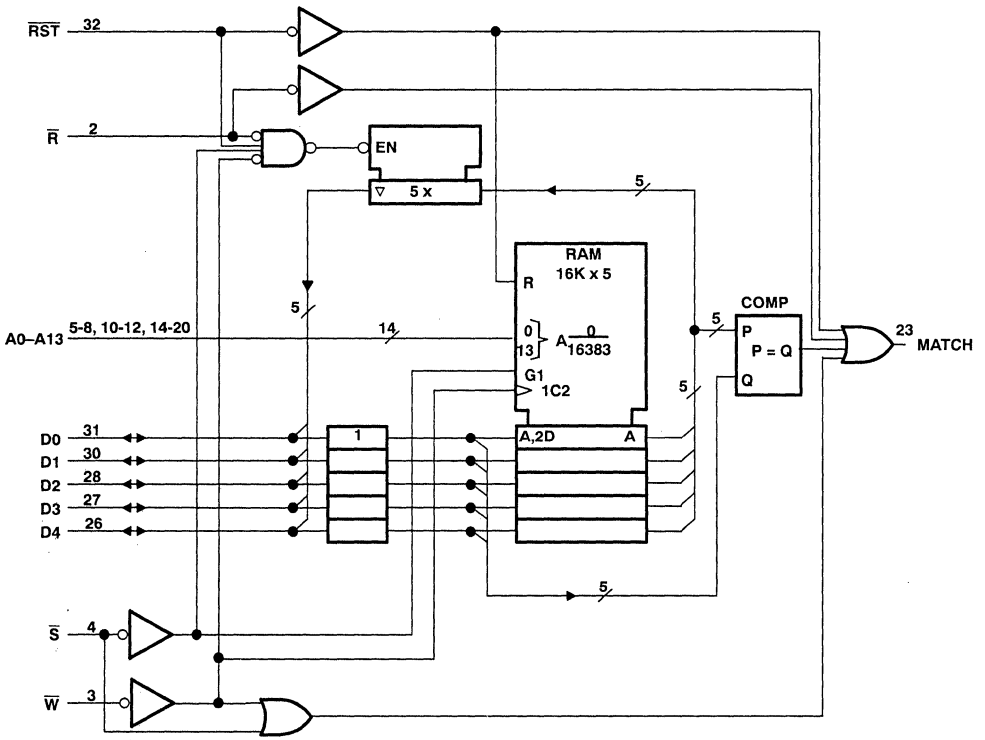
PRODUCT PREVIEW

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic) SN74BCT2163, SN74BCT2164



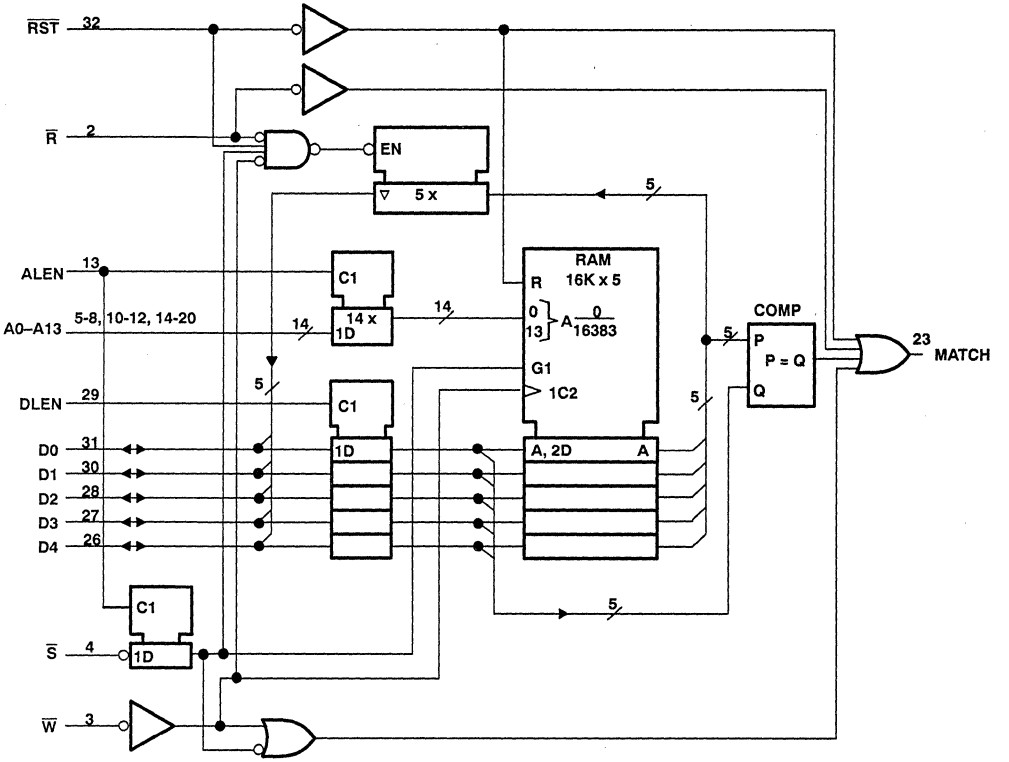
FUNCTION TABLE

INPUTS				I/O	OUTPUT	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$†	$\overline{RST}$	D0-D4	MATCH	
↓	X	L	H	Input	H	Write
↓	X	L	H	Latched	H	Write
L	X	L	H	Hi-Z	H	MATCH forced high
L	X	↓	H	Hi-Z	H	No write occurs
H	L	L	H	Output	H	Read
H	H	L	H	Input	L	Not equal
H	H	L	H	Latched	L	Not equal
H	H	L	H	Input	H	Equal
H	H	L	H	Latched	H	Equal
H	X	X	L	Hi-Z	H	Memory reset
X	X	H	H	Hi-Z	H	Device disabled

† ALEN going low latches the states of A0-A13 and $\overline{S}$. This column assumes the indicated levels at $\overline{S}$ exist within the latch.

PRODUCT PREVIEW

logic diagram (positive logic) SN74BCT2166



FUNCTION TABLE

INPUTS					I/O	OUTPUT	FUNCTION
$\overline{W}$	$\overline{R}$	DLEN	$\overline{S}$†	$\overline{RST}$	D0-D4	MATCH	
↓	X	H	L	H	Input	H	Write
↓	X	L	L	H	Latched	H	Write
L	X	X	L	H	Hi-Z	H	MATCH forced high
L	X	X	↓	H	Hi-Z	H	No write occurs
H	L	X	L	H	Output	H	Read
H	H	H	L	H	Input	L	Not equal
H	H	L	L	H	Latched	L	Not equal
H	H	H	L	H	Input	H	Equal
H	H	L	L	H	Latched	H	Equal
H	X	X	X	L	Hi-Z	H	Memory reset
X	X	X	H	H	Hi-Z	H	Device disabled

† ALEN going low latches the states of A0-A13 and $\overline{S}$. This column assumes the indicated levels at $\overline{S}$ exist within the latch.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13	5 6 7 8 10 11 12 14 15 16 17 18 19 20	Address inputs. Address 1 of 16K by 5-bit RAM memory locations. Must be stable for the duration of the write cycle.
ALEN ('BCT2166 Only)	13	Address and select latch enable input. When ALEN is high the latch is transparent. When ALEN is low A0-A13 and $\overline{S}$ are latched.
D0 D1 D2 D3 D4	31 30 28 27 26	Data (tag) inputs/outputs. D0-D4 are inputs during the compare and write modes. D0-D4 are outputs during the read mode.
DLEN ('BCT2166 Only)	29	Data latch enable input. When DLEN is high the latch is transparent. When DLEN is low D0-D4 are latched.
GND	1 24 25 29	Ground. (Pin 29 ground is for 'BCT2163 and 'BCT2164 only.)
MATCH	23	When MATCH output is high during a compare cycle, D0-D4 equals the contents of the 5-bit memory location addressed by A0-A13. MATCH is also driven high during deselect, reset, read, and write.
$\overline{R}$	2	Read input. When $\overline{R}$ and $\overline{S}$ are low and $\overline{W}$ is high, addressed data is output to the D0-D4 pins and the MATCH output is forced high.
$\overline{RST}$	32	Reset input. Aschronously clears entire RAM array to zero and forces MATCH high when $\overline{RST}$ is low.
$\overline{S}$	4	Chip select input. Enables device when $\overline{S}$ is low. Deselects device and forces MATCH high when $\overline{S}$ is high.
V_{CC}	9 21 22	Supply voltage.
$\overline{W}$	3	Write control input. Writes D0-D4 into the RAM location addressed by A0-A13 and forces MATCH high when $\overline{W}$ is low. Places selected device in compare mode when $\overline{W}$ and $\overline{R}$ are high and $\overline{S}$ is low.

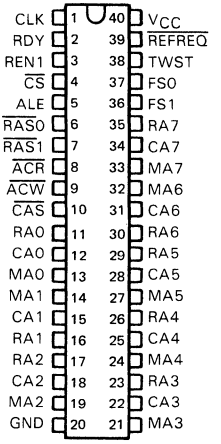
PRODUCT PREVIEW

Contents

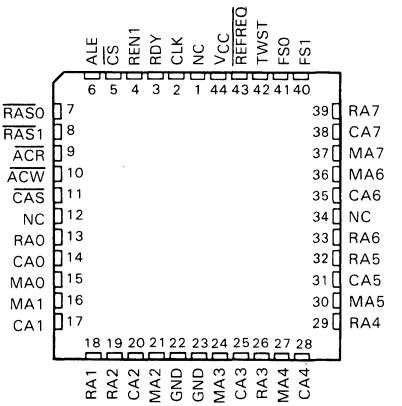
D2674, JANUARY 1982—REVISED AUGUST 1985

- Controls Operation of 8K, 16K, 32K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Devices
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait-State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns, 200 ns, or 250 ns

TMS4500A . . . N PACKAGE
(TOP VIEW)



TMS4500A . . . FN PACKAGE
(TOP VIEW)



description

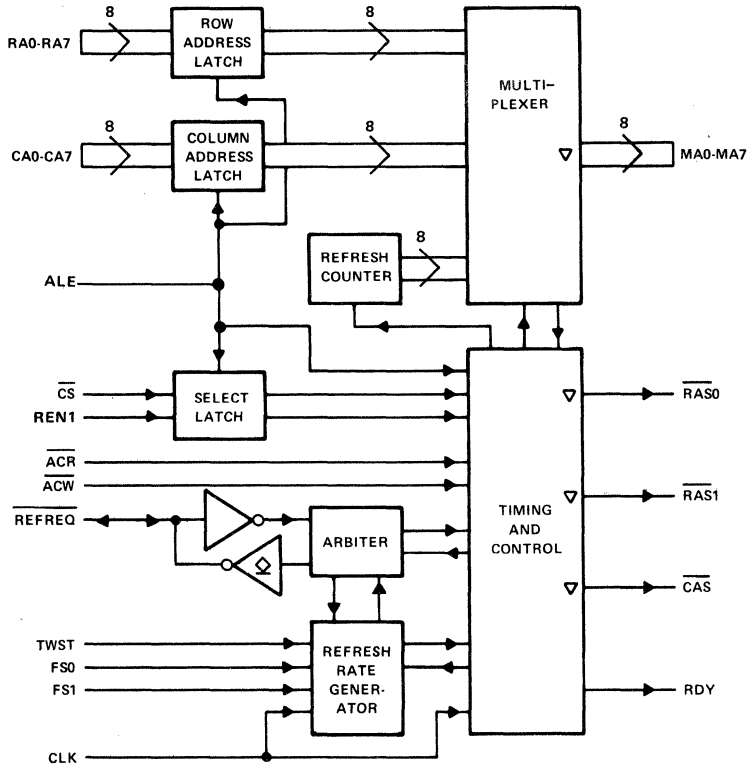
The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and 44-pin, 650-mil square plastic chip carrier package. It is characterized for operation from 0°C to 70°C.

functional block diagram



TERMINAL FUNCTIONS

PIN NAME	I/O/Z	DESCRIPTION
$\overline{ACR}$, ACW	I	Access Control, Read; Access Control, Write. A low on either of these inputs causes the column address to appear on MA0-MA7 and the column address strobe. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA7, $\overline{RAS0}$, $\overline{RAS1}$, and $\overline{CAS}$ go into a high-impedance (floating) state.
ALE	I	Address Latch Enable. This input is used to latch the 16 address inputs, $\overline{CS}$ and REN1. This also initiates an access cycle if chip select is valid. The rising edge (low level to high level) of ALE returns $\overline{RAS}$ to the high level.
$\overline{CAS}$	O	Column Address Strobe. This three-state output is used to latch the column address into the DRAM array.
CA0-CA7	I	Column Address. These address inputs are used to generate the column address for the multiplexer.
CLK	I	System Clock. This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.

TERMINAL FUNCTIONS (continued)

PIN NAME	I/O/Z	DESCRIPTION
$\overline{CS}$	I	Chip Select. A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
FS0, FS1	I	Frequency Select 0; Frequency Select 1. These are strap inputs to select Mode and Frequency of operation as shown in the Strap Configuration table.
MA0-MA7	O	Memory Address. These three-state outputs are designed to drive the addresses of the dynamic RAM array.
$\overline{RAS0}$, $\overline{RAS1}$	O	Row Address Strobe. These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
RA0-RA7	I	Row Address. These address inputs are used to generate the row address for the multiplexer.
RDY	O	Ready. This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
$\overline{REFREQ}$	I/O	Refresh Request. (This input should be driven by an open-collector output.) On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle in progress and the current refresh address is present on MA0-MA7. (Note: $\overline{REFREQ}$ contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
REN1	I	RAS Enable 1. This input is used to select one of two banks of RAM via the $\overline{RAS0}$ and $\overline{RAS1}$ outputs when chip select is present. When it is low, $\overline{RAS0}$ is selected; when it is high, $\overline{RAS1}$ is selected.
TWST	I	Timing/Wait Strap. A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.

STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLK FREQ. (MHz)	REFRESH FREQ. (kHz)	CLOCK FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	—	REFREQ	4
L	L	H	0	CLK + 31	1,984	64-95‡	3
L	H	L	0	CLK + 46	2,944	64-85‡	3
L	H	H	0	CLK + 61	3,904	64-82§	4
H	L	L	1	CLK + 46	2,944	64-85‡	3
H	L	H	1	CLK + 61	3,904	64-80‡	4
H	H	L	1	CLK + 76	4,864	64-77‡	4
H	H	H	1	CLK + 91	5,824	64-88¶	4

†The strap configuration resets the Refresh Timer circuitry.
‡The highest frequency in the refresh frequency column is the frequency that is produced if the minimum CLK frequency of the next selection state is used.
§The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 5 MHz.
¶The highest frequency in the refresh column is the refresh frequency if the CLK frequency is 8 MHz.

functional description

TMS4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0-MA7 follows the inputs RA0-RA7.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in the Strap Configuration table. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are low. The configuration straps allow the matching of memories to the system access time.

Upon Power-Up it is necessary to provide a reset signal by driving all three straps to the controller low to initialize internal counters. A system's low-active, power-on reset ($\overline{\text{RESET}}$) can be used to accomplish this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. [A low-to-high transition on TWST sets the refresh counter to FF_{16} (255_{10}).]

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

arbiter

the arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

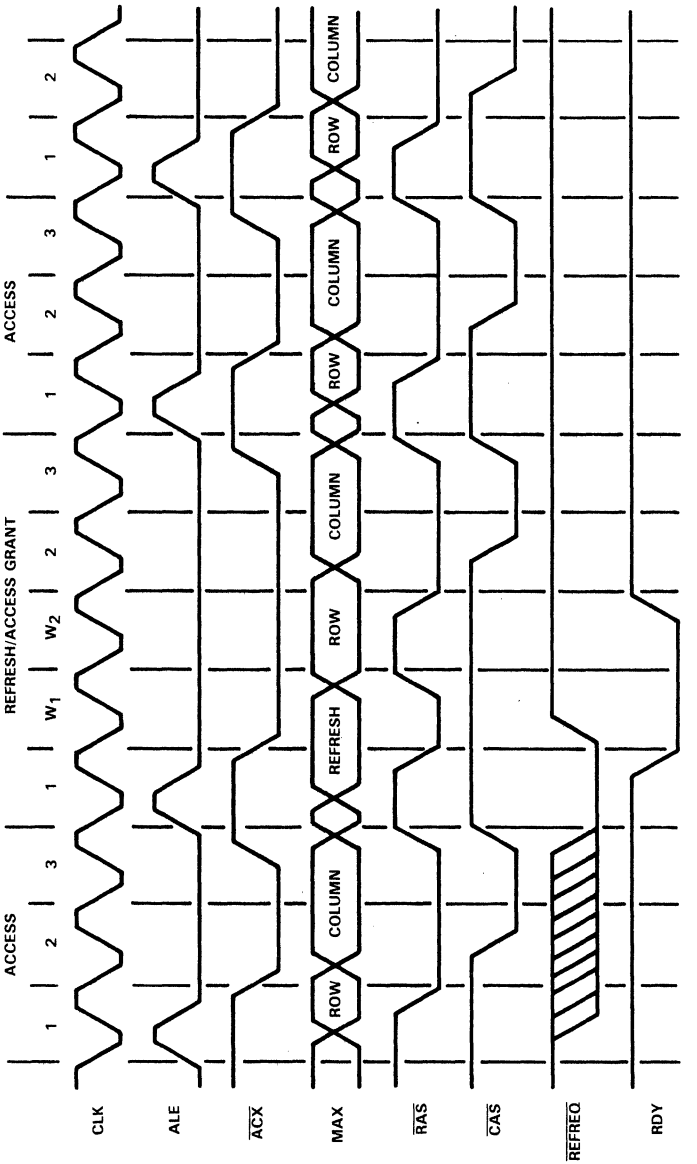


FIGURE 1. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS LOW)

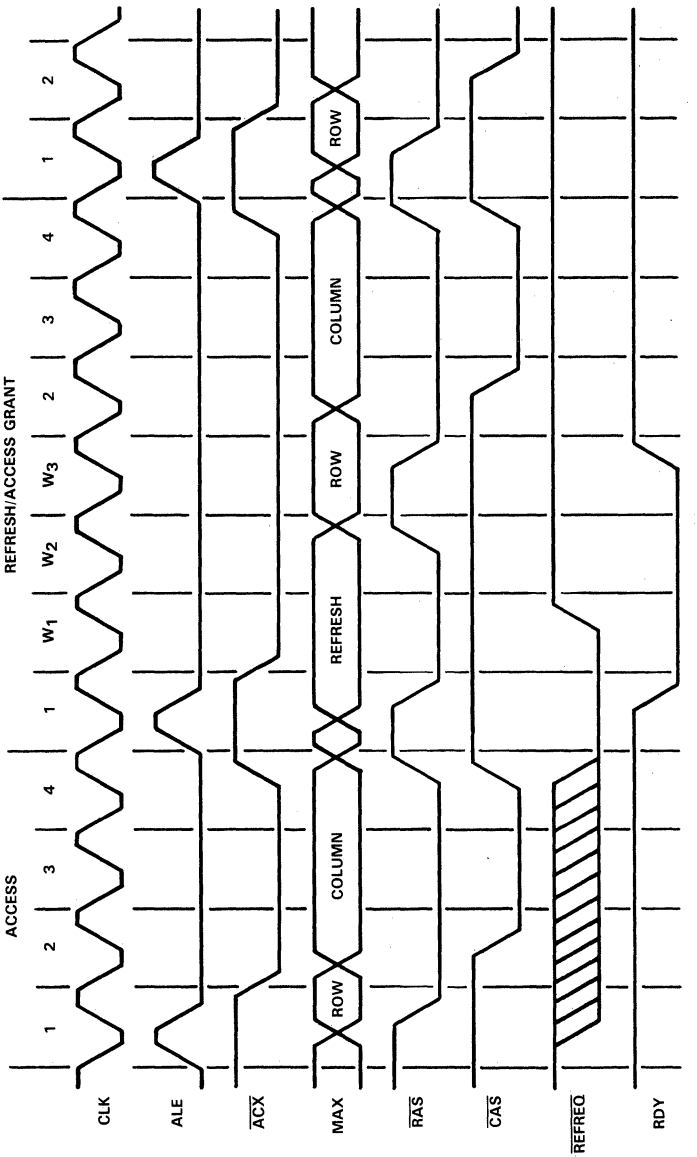


FIGURE 2. TYPICAL ACCESS/REFRESH/ACCESS CYCLE
(FOUR-CYCLE, TWST IS LOW)

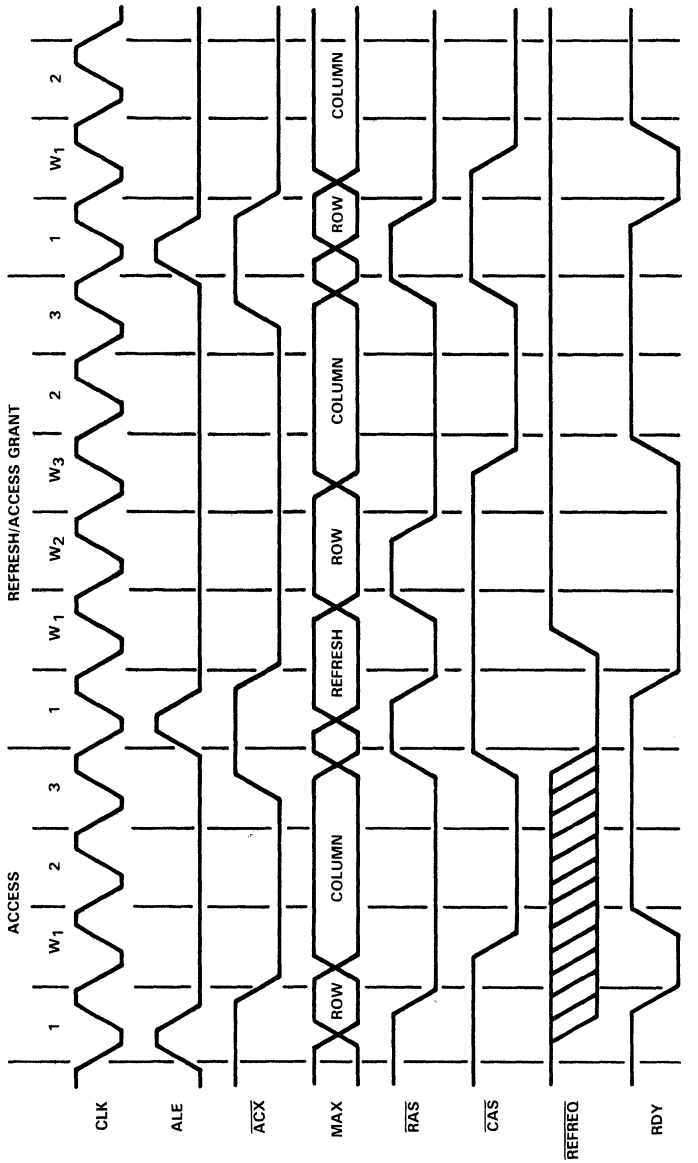


FIGURE 3. TYPICAL ACCESS/REFRESH/ACCESS CYCLE
(THREE-CYCLE, TWST IS HIGH)

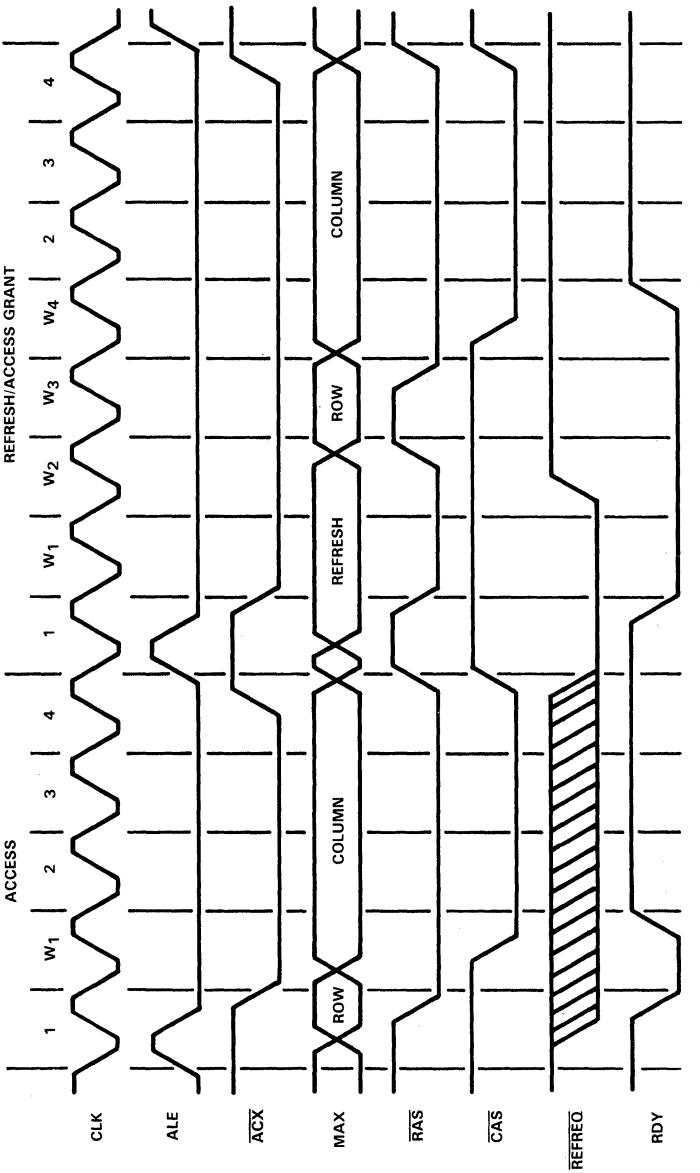


FIGURE 4. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS HIGH)

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range (any input) . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1.2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground terminal.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2.4		6	V
Low-level input voltage, V_{IL}	−1‡		0.8	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			4	mA
Short-circuit output current, I_{OS}§			−50	mA
Operating free-air temperature, T_A	0		70	°C

‡The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

§Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP¶	MAX	UNIT
V_{OH}	High-level output voltage	MA0-MA7, RDY	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4			V
		$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS}$			2.7			
		$\overline{REFREQ}$	V_{CC} = 4.5 V,	I_{OH} = −100 μA	2.4			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 4 mA			0.4	V
I_{IH}	High-level input current except $\overline{REFREQ}$		V_I = 5.5 V				10	μA
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0				−1.25	mA
		All others					−10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V,	V_O = 0 to 4.5 V			±50	μA
I_{CC}	Operating supply current		T_A = 0°C			100	140	mA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		5		pF
C_o	Output capacitance		V_O = 0,	f = 1 MHz		6		pF

¶All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended supply voltage range and operating free-air temperature range†

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	$C_L = 160$ pF		35		40		50	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	$C_L = 160$ pF		45		50		60	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	$C_L = 160$ pF		65		75		90	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	$C_L = 40$ pF		40		40		40	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Note 2)	$C_L = 160$ pF	60	150	70	200	80	250	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	$C_L = 160$ pF		30		30		40	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$ low	$C_L = 160$ pF	15		20		25		ns
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low	$C_L = 160$ pF		0		0		0	ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 2)	$C_L = 160$ pF	40	100	45	130	50	165	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	$C_L = 160$ pF		30		40		50	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	$C_L = 160$ pF	5	30	10	40	15	50	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	$C_L = 160$ pF	10		15		15		ns
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 3)	$C_L = 40$ pF		40		45		60	ns
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	$C_L = 40$ pF		30		35		35	ns
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low	$C_L = 40$ pF		30		35		45	ns
t_{CL-MAV}	Time delay, CLK low till refresh address valid	$C_L = 160$ pF		75		100		125	ns
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low	$C_L = 160$ pF	10	50	15	60	20	80	ns
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low	$C_L = 160$ pF	5		5		5		ns
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)	$C_L = 160$ pF		50		55		75	ns
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)	$C_L = 160$ pF		50		55		75	ns
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high	$C_L = 160$ pF	5	35	10	45	10	60	ns
t_{CH-MAX}	Refresh address valid after CLK high	$C_L = 160$ pF	15		20		25		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

NOTES: 2. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

3. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising after the edge that causes access RAS low on access grant cycles (assuming $\overline{ACX}$ low).

switching characteristics over recommended supply voltage range and operating free-air temperature range (continued)†

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CH-REL}	Time delay, CLK high till access $\overline{RAS}$ starting low	$C_L = 160$ pF		60		70		95	ns
t_{CL-CEL}	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 4)			125		140		185	
t_{CL-MAX}	Row address valid after CLK low		25		30		40		
$t_{REL-MAX}$	Row address valid after $\overline{RAS}$ low		25		30		35		
$t_{AEH-MAX}$	Column address valid after ALE high	$C_L = 160$ pF	10		15		20		
t_{dis}	Output disable time (3-state outputs)			100		125		165	
t_{en}	Output enable time (3-state outputs)			75		80		105	
$t_{CAV-CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low after refresh		0		0		0		
t_{CH-CEL}	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 4)			180		200		235	
t_{ACL-CL}	$\overline{ACX}$ low to CLK starting low	$C_L = 40$ pF	25		35		45		
$t_{ACL-RYH}$	$\overline{ACX}$ low to RDY starting high	$C_L = 40$ pF		40		50		60	
t_{CL-ACL}	CLK low to $\overline{ACX}$ starting low	$C_L = 40$ pF	0		0		0		
$t_{t(CEL)}$	$\overline{CAS}$ fall time	$C_L = 320$ pF		15		20		25	
$t_{t(CEH)}$	$\overline{CAS}$ rise time			30		35		45	
$t_{t(REL)}$	$\overline{RAS}$ fall time	$C_L = 160$ pF		15		20		25	
$t_{t(REH)}$	$\overline{RAS}$ rise time			15		20		25	
$t_{t(MAV)}$	Address transition time			20		20		25	
$t_{t(RYL)}$	RDY fall time	$C_L = 40$ pF		10		15		20	
$t_{t(RYH)}$	RDY rise time			20		25		35	

†See Parameter Measurement Information for test circuit and voltage waveforms.

NOTE 4: On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low. (See Refresh Cycle Timing Diagram.)

timing requirements over recommended supply voltage range and operating free-air temperature range (unless otherwise noted)†

PARAMETER		TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		120		140		ns
$t_{w(CH)}$	CLK high pulse duration	40		40		40		
$t_{w(CL)}$	CLK low pulse duration	40		45		45		
t_t	Transition time, all inputs		50		50		50	
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 5)	10		10		15		
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 5)	10		10		15		
t_{CL-AEH}	Time delay, CLK low to ALE starting high (see Note 6)	15		20		20		
$t_{w(AEH)}$	Pulse duration, ALE high	50		60		60		
t_{AV-AEL}	Time delay, address REN1 $\overline{CS}$ valid to ALE low	5		10		15		
t_{AEL-AX}	Time delay, ALE low to address not valid	10		10		10		
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 7, 8, 9, and 10)	$t_{h(RA)}+30$		$t_{h(RA)}+40$		$t_{h(RA)}+50$		
t_{ACH-CL}	Time delay, $\overline{ACX}$ high to CLK low (see Notes 7 and 11)	20		20		20		
t_{ACL-CH}	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		30		30		
t_{RQL-CL}	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 12)	20		20		20		
$t_{w(RQL)}$	Pulse duration, $\overline{REFREQ}$ low	20		20		20		
$t_{w(ACL)}$	$\overline{ACX}$ low duration (see Note 13)	110		140		175		

†See Parameter Measurement Information for test circuit and voltage waveforms.

NOTES:
5. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from $\overline{ACX}$ high to ALE low.
6. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
7. These specifications relate to system timing and do not directly reflect device performance.
8. On the access grant cycle following refresh, the occurrance of $\overline{CAS}$ low depends on the relative occurrance of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the high transition causing $\overline{RAS}$ low.
9. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to coincident with ALE.
10. $t_{h(RA)}$ is the dynamic memory row address hold time, $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems when the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
11. The minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
12. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
13. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

PARAMETER MEASUREMENT INFORMATION

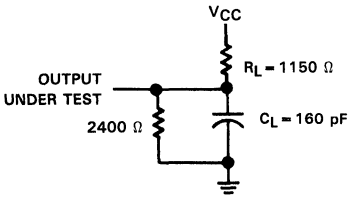


FIGURE 5. LOAD CIRCUIT

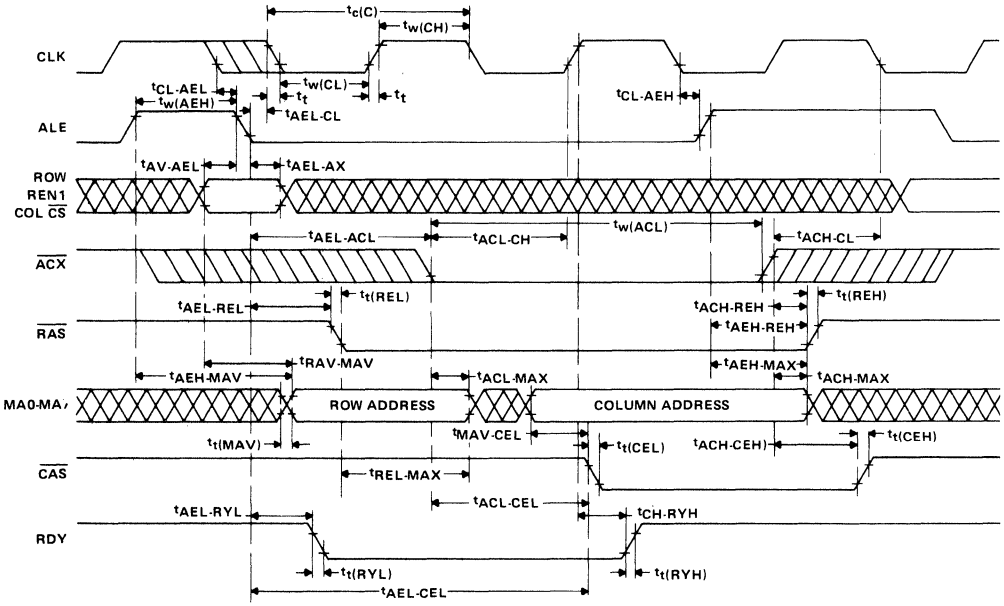


FIGURE 6. ACCESS CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION

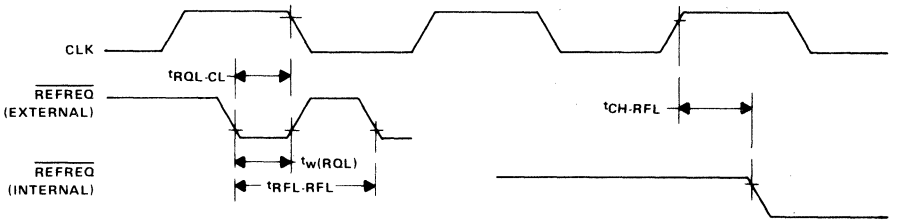
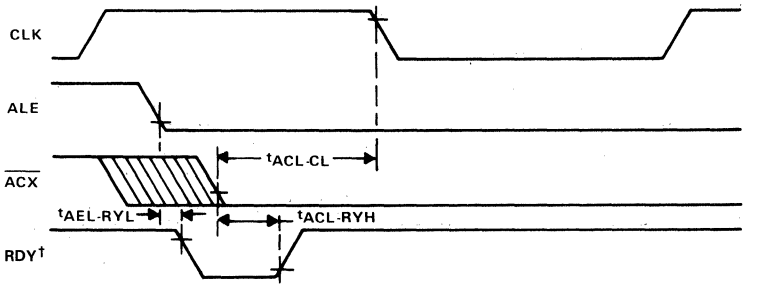


FIGURE 7. REFRESH REQUEST TIMING

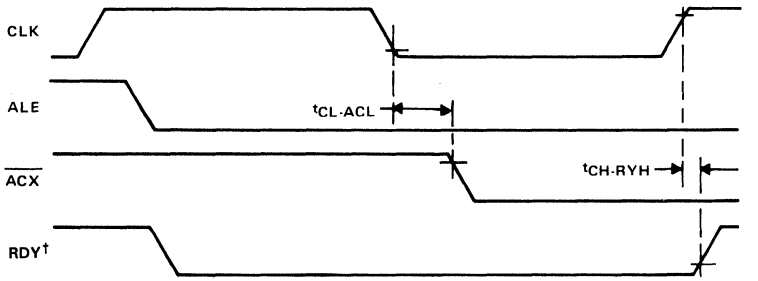


†RDY starting high is timed from $\overline{ACX}$ low ($t_{ACL-RYH}$) for the condition $\overline{ACX}$ low while CLK high.

FIGURE 8. READY TIMING (ACX DURING CLK HIGH)
(SEE NOTES 14 THRU 17)

NOTES: 14. For RDY high transiton (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK.
15. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY high transition will be $t_{ACL-RYH}$.
16. t_{ACL-CL} is a timing parameter for control of RDY to be dependent upon $\overline{ACX}$ low.
17. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

PARAMETER MEASUREMENT INFORMATION



†RDY starting high is timed from CLK high (t_{CH-RYH}) for the condition $\overline{ACX}$ going low while CLK low.

FIGURE 9. READY TIMING ($\overline{ACX}$ DURING CLK LOW) (SEE NOTES 14 THRU 17)

NOTES: 14. For RDY high transiton (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK.
15. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY high transition will be $t_{ACL-RYH}$.
16. t_{ACL-CL} is a timing parameter for control of RDY to be dependent upon $\overline{ACX}$ low.
17. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

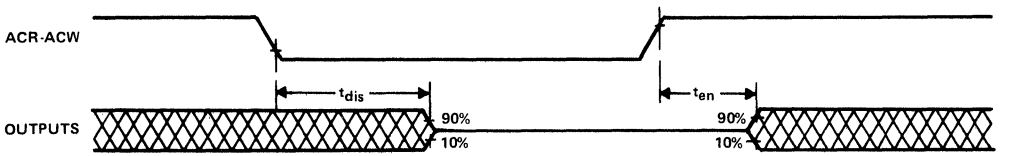


FIGURE 10. OUTPUT 3-STATE TIMING

PARAMETER MEASUREMENT INFORMATION

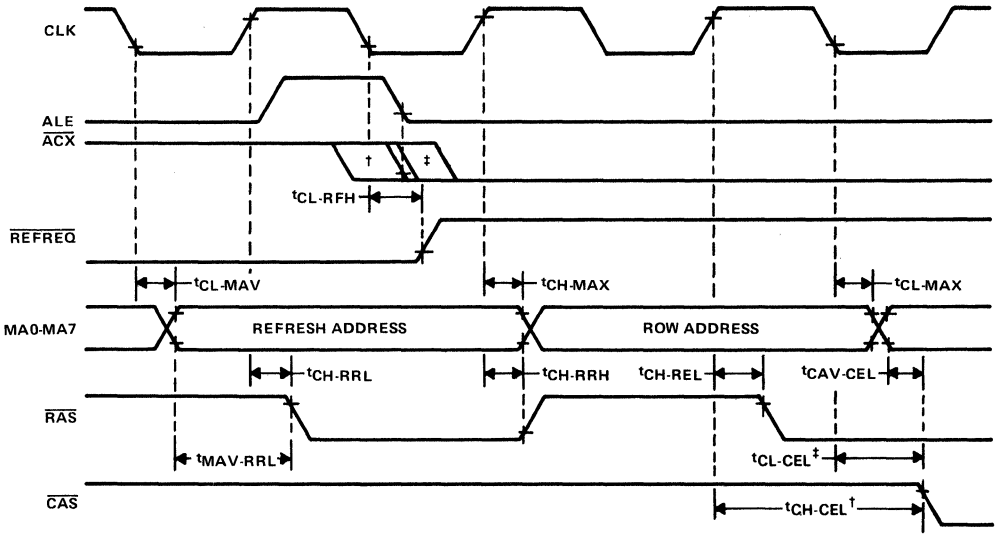
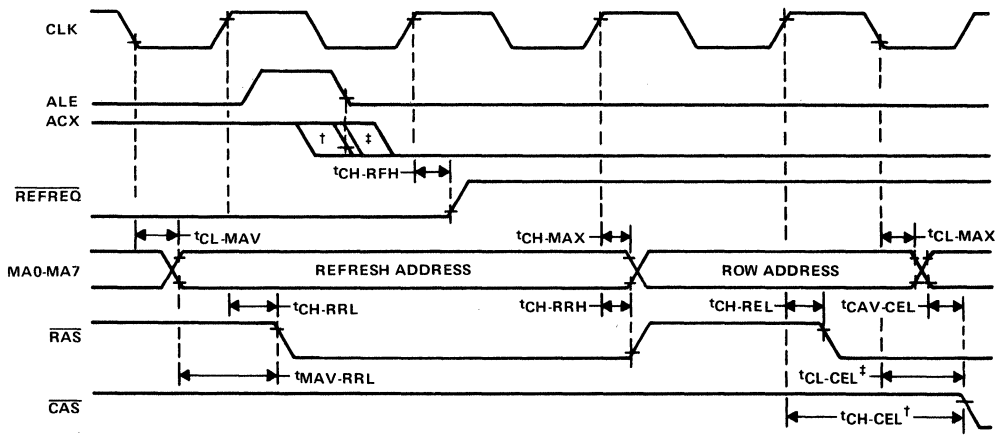


FIGURE 11. REFRESH CYCLE TIMING (THREE-CYCLE)



† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

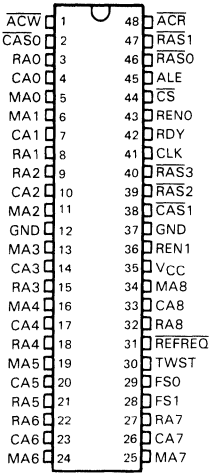
‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

FIGURE 12. REFRESH CYCLE TIMING (FOUR-CYCLE)

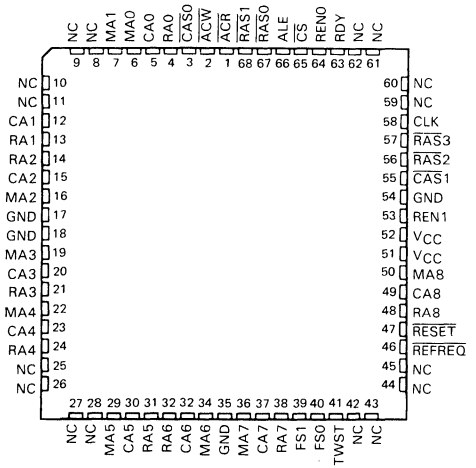
D2989, JUNE 1987—REVISED MARCH 1990

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2M Byte of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$ Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  115 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Equivalent to TMS4500A/B and to VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The THCT4502B is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

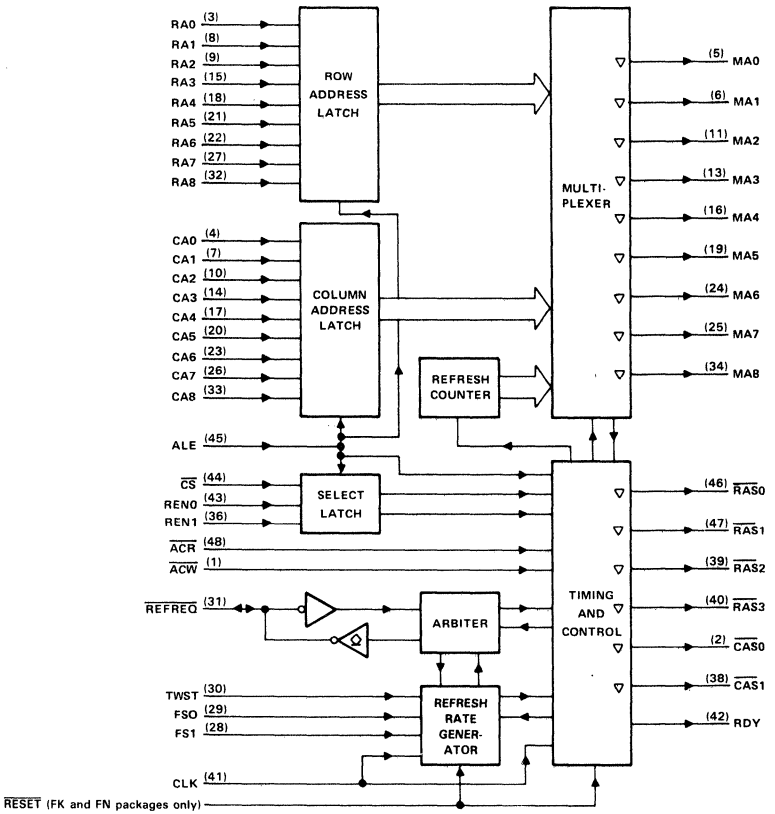
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The THCT4502B also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles.

The THCT4502B is characterized for operation from 0°C to 70°C.

functional block diagram†



†Pin numbers shown are for JD and N packages.

TERMINAL FUNCTIONS

PIN NAME	I/O	DESCRIPTION
$\overline{ACR}$ $\overline{ACW}$	I	Access Control, Read; Access Control, Write. A low on either of these inputs causes the column address to appear on MA0-MA8 and a low-going pulse from $\overline{CAS}$. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by forcing $\overline{RAS}$ and $\overline{CAS}$ high. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA8, $\overline{RAS}$0, $\overline{RAS}$1, $\overline{RAS}$2, $\overline{RAS}$3, $\overline{CAS}$0 and $\overline{CAS}$1 go into a high-impedance (floating) state.
ALE	I	Address Latch Enable. This input is used to latch the 18 address inputs, $\overline{CS}$, REN0, and REN1. This also initiates an access cycle if $\overline{CS}$ is low. The rising edge (low level to high level) of ALE returns all $\overline{RAS}$ outputs to the high level.
CA0-CA8	I	Column Address. These address inputs are used to generate the column address for the multiplexer.
$\overline{CAS}$0 $\overline{CAS}$1	O	Column Address Strobe. These three-state outputs are used to latch the column address into the DRAM array.
CLK	I	System Clock. This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, and FS0 inputs.
$\overline{CS}$	I	Chip Select. A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
FS0 FS1	I	Frequency Select 0; Frequency Select 1. These are strap inputs to select Mode and Frequency of operation as shown in the Strap Configuration Table.
MA0-MA6	O	Memory Address. These three-state outputs are designed to drive the addresses of the dynamic RAM array.
RA0-RA8	I	Row Address. These address inputs are used to generate the row address for the multiplexer.
$\overline{RAS}$0-$\overline{RAS}$3	O	Row Address Strobe. These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN0 and REN1. On refresh, all $\overline{RAS}$ signals are active.
RDY	O	Ready. This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
$\overline{REFREQ}$	I/O	Refresh Request. This input should be driven by an open-collector or open-drain output. On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA8. (Note: $\overline{REFREQ}$ contains an internal active pullup with a nominal resistance of 10 kΩ, which is disabled when $\overline{REFREQ}$ is low).
REN0 REN1	I	$\overline{RAS}$ Enable 0 and 1. These inputs are used to select one of four banks of RAM when $\overline{CS}$ is low. When REN1 is low, the lower banks are enabled via $\overline{CAS}$0, $\overline{RAS}$0, and $\overline{RAS}$1. When REN1 is high, the higher banks are enabled via $\overline{CAS}$1, $\overline{RAS}$2 and $\overline{RAS}$3. REN0 selects $\overline{RAS}$0 and $\overline{RAS}$2 when low, or $\overline{RAS}$1 and $\overline{RAS}$3 when high. (see Output Strobe Selection Table).
$\overline{RESET}$†	I	$\overline{RESET}$. Active-low input to initialize the pontroller asynchronously. Refresh Address is set to IFF_{16}, internal refresh requests, synchronizer, and frequency divider are cleared. (Note: $\overline{RESET}$ contains an internal pullup resistor with a nominal resistance of 100 kΩ, which allows this pin to be left open.)
TWST	I	Timing/Wait Strap. A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing or initialize the controller.

†This function is available only in the FK and FN packages.

FUNCTION TABLES

STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	EXTERNAL	–	REFREQ	3
L	H	L	0	CLK ÷ 61	3.904	64-95‡	3
L	H	H	0	CLK ÷ 91	5.824	64-88§	4
H	L	L	1	CLK ÷ 61	3.904	64-95‡	3
H	L	H	1	CLK ÷ 91	5.824	64-75‡	4
H	H	L	1	CLK ÷ 106	6.784	64-73‡	4
H	H	H	1	CLK ÷ 121	7.744	64-83¶	4

† This strap configuration resets the Refresh Timer Circuitry.
‡ Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.
§ Refresh frequency if clock frequency is 8 MHz.
¶ Refresh frequency if clock frequency is 10 MHz.

OUTPUT STROBE SELECTION

CONTROL INPUT		SELECTED OUTPUT					
REN1	REN0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$	$\overline{CAS1}$
L	L	X				X	
L	H		X			X	
H	L			X			X
H	H				X		X

NOTE: Changing the logic value of REN1 after a low-to-high transition of ALE and before $\overline{ACX}$ rises causes the other $\overline{CAS}$ to fall. Both $\overline{CAS}$ signals remain low until $\overline{ACX}$ rises.

functional description

The THCT4502B consists of six basic blocks: address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0-MA8 follows the inputs RA0-RA8.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in the Strap Configuration Table. The counter is reset when a refresh cycle is requested or when TWST, FS1, and FS0 are low. The configuration straps allow the matching of memories to the system access time. Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller (or $\overline{RESET}$ for devices in the FK and FN packages only) low. A systems power-on reset ($\overline{RESET}$) can be used to do this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. A low-to-high transition on TWST sets the refresh counter to $1FF_{16}$ (511_{10}).

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{RAS}$ and $\overline{CAS}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

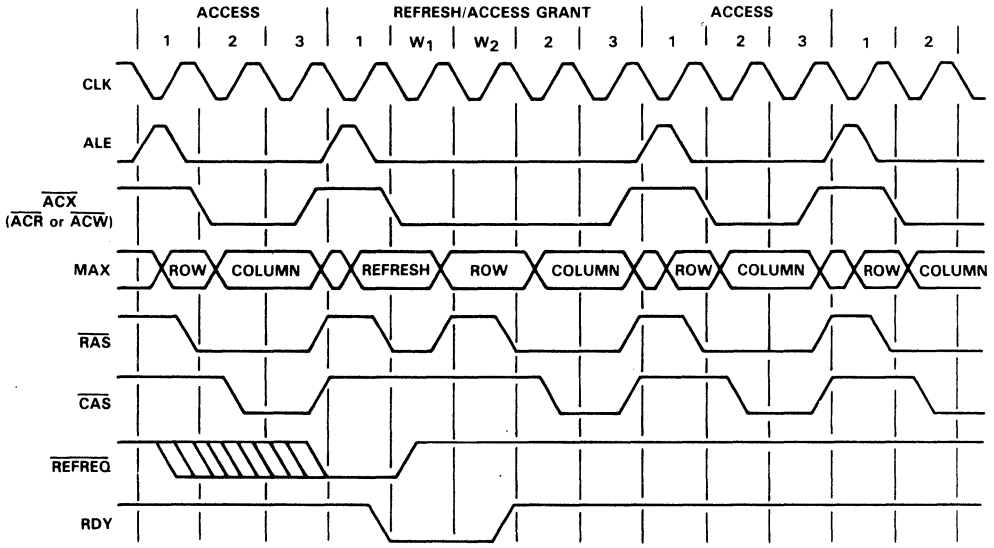


FIGURE 1. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS LOW)

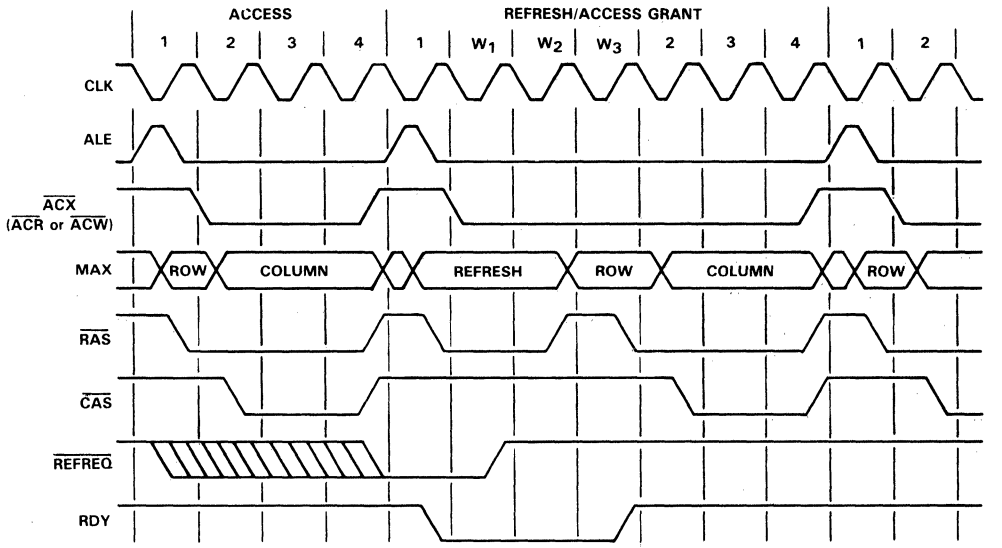


FIGURE 2. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS LOW)

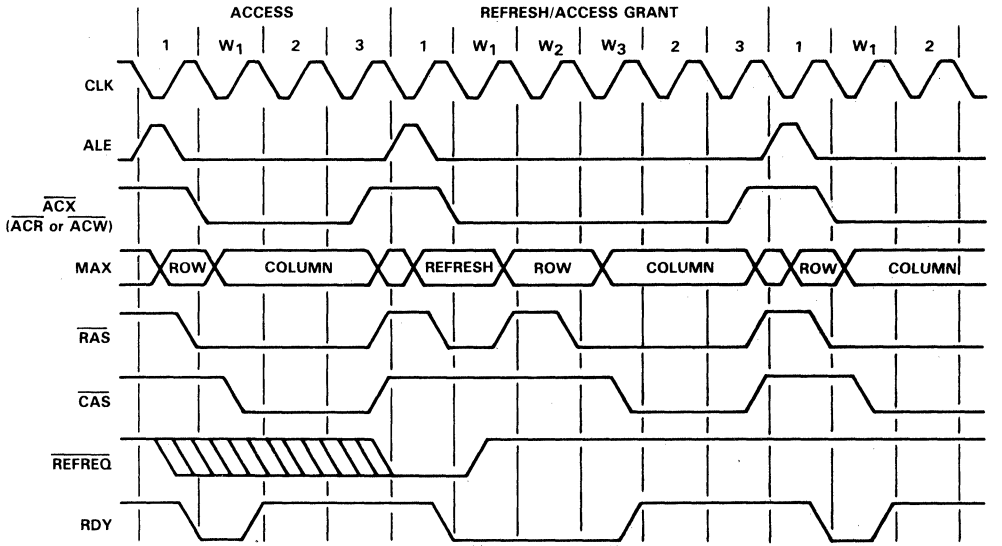


FIGURE 3. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS HIGH)

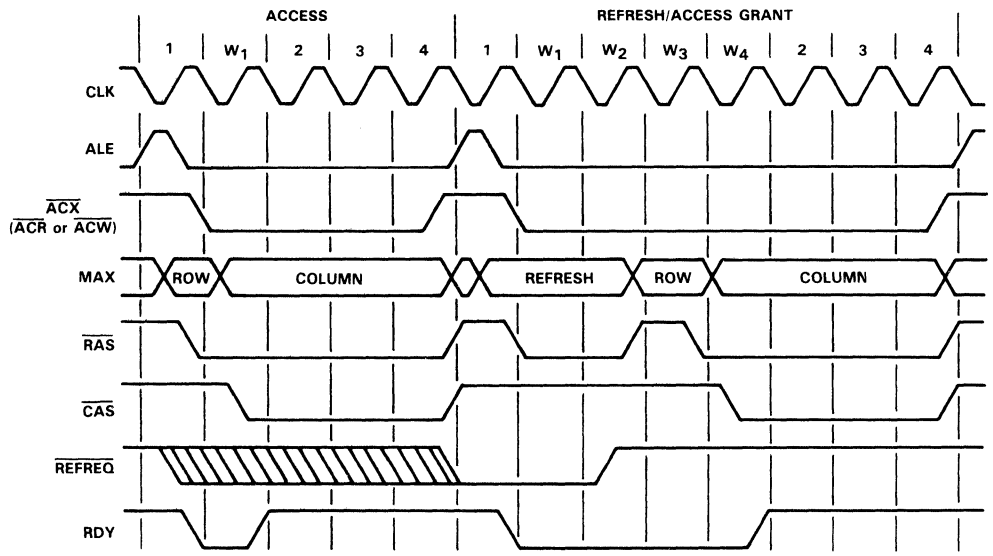


FIGURE 4. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS HIGH)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−1.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$, $V_I > V_{CC}$)	±20 mA
Output diode current, I_{OK} ($V_O < 0$, $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or JD package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage	-0.5†		0.8	V
V_O	Output voltage	-0.5		$V_{CC}+0.5$	V
t_t	Input transition (rise and fall) time	0		500	ns
T_A	Operating free-air temperature	0		70	°C

† The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}	High-level output voltage	MA0–MA8, $\overline{RAS0}$–$\overline{RAS3}$, $\overline{CAS0}$–$\overline{CAS1}$	I_{OH} = -20 μA	4.5 V	4.4			4.4		V
			I_{OH} = -6 mA	4.5 V	3.86			3.76		
		RDY	I_{OH} = -20 μA	4.5 V	4.4			4.4		
			I_{OH} = -4 mA	4.5 V	3.86			3.76		
		$\overline{REFREQ}$	I_{OH} = -20 μA	4.5 V	4			3.8		
V_{OL}	Low-level output voltage	RDY, $\overline{REFREQ}$	I_{OL} = 20 μA	4.5 V			0.1		0.1	V
			I_{OL} = 4 mA	4.5 V			0.32		0.37	
		MA0–MA8, $\overline{RAS0}$–$\overline{RAS3}$, $\overline{CAS0}$, $\overline{CAS1}$	I_{OL} = 20 μA	4.5 V			0.1		0.1	
			I_{OL} = 6 mA	4.5 V			0.32		0.37	
I_{IH}	High-level input current except $\overline{REFREQ}$		V_I = 5.5 V	5.5 V			0.1		1	μA
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0	5.5 V			-5		-50	μA
		$\overline{RESET}$					-100		-250	
		All others					-0.1		-1	
I_{OZ}‡	Off-state output current (3-state outputs only)		V_O = 0 to 5.5 V	5.5 V			±5		±50	μA
I_{CC}	Supply current		V_I = V_{CC} or 0, I_O = 0	5.5 V			5		15	mA
ΔI_{CC}§	Supply current change		One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3	mA
C_i	Input capacitance		V_I = 0, f = 1 MHz	5.5 V		5	10		10	pF

‡ This parameter, I_{OZ}, the high impedance-state output current, applies only for three-state outputs and transceiver I/O pins.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		THCT4502B-115		UNIT
		MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		ns
$t_{w(CH)}$	Pulse duration, CLK high	45		ns
$t_{w(CL)}$	Pulse duration, CLK low	45		ns
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 2)	15		ns
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 2)	15		ns
t_{CL-AEH}	Time delay, CLK low to ALE (see Note 3)	15		ns
$t_{w(AEH)}$	Pulse duration, ALE high	45		ns
t_{AV-AEL}	Time delay, address REN0, REN1, $\overline{CS}$ valid to ALE low	10		ns
t_{AEL-AX}	Time delay, ALE low to address not valid	15		ns
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 4, 5, 6, and 7)	$t_{h(RA)}+30$		ns
t_{ACH-CL}	Time delay, $\overline{ACX}$ high to CLK low (see Notes 4 and 8)	30		ns
t_{ACL-CH}	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		ns
t_{RQL-CL}	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 9)	35		ns
$t_{w(RQL)}$	Pulse duration, $\overline{REFREQ}$ low	30		ns
$t_{w(ACL)}$	Pulse duration, $\overline{ACX}$ low (see Note 10)	120		ns
t_{reset}	Power-up reset	$4t_{cCLK}$		ns

NOTES:
2. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge.
3. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
4. These specifications relate to system timing and do not directly reflect device performance.
5. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE, then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE, then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.
6. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
7. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
8. The minimum of 30 ns is specified to ensure arbitration will occur on falling CLK edge, t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
9. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
10. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS†	THCT4502B-115		UNIT
			MIN	MAX	
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 180 pF		35	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	C_L = 360 pF		42	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	C_L = 360 pF		60	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	C_L = 40 pF		33	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Note 11)	C_L = 360 pF	50	115	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	C_L = 180 pF		35	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$	C_L = 360 pF	10		ns
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low	C_L = 360 pF	0		ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 11)	C_L = 360 pF	25	80	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	C_L = 180 pF		40	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	C_L = 360 pF	5	30	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	C_L = 360 pF	5		ns
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 12)	C_L = 40 pF		42	ns
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	C_L = 40 pF		35	ns
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low	C_L = 40 pF		50	ns
t_{CL-MAV}	Time delay, CLK low till refresh address valid	C_L = 360 pF		70	ns
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low	C_L = 180 pF	5	50	ns
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low	C_L = 180 pF	5		ns
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)	C_L = 40 pF		50	ns
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)	C_L = 40 pF		50	ns
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high	C_L = 180 pF	5	30	ns
t_{CH-MAX}	Refresh address valid after CLK high	C_L = 360 pF	10		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

NOTES: 11. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

12. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ low on access grant cycles (assuming $\overline{ACX}$ low).

switching characteristics over recommended supply voltage range and operating free-air temperature range (continued)

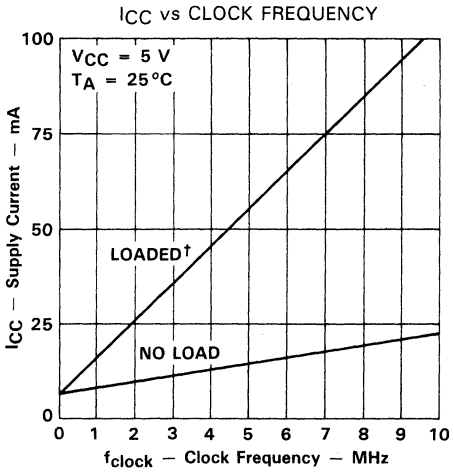
PARAMETER		TEST CONDITIONS†	THCT4502B-115		UNIT
			MIN	MAX	
t_{CH-REL}	Time delay, CLK high till access $\overline{RAS}$ starting low	C_L = 180 pF		45	ns
t_{CL-CEL}	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 13)	C_L = 360 pF		70	ns
t_{CL-MAX}	Row address valid after CLK low	C_L = 360 pF	15		ns
$t_{REL-MAX}$	Row address valid after $\overline{RAS}$ low	C_L = 360 pF	20		ns
$t_{AEH-MAX}$	Column address valid after ALE high	C_L = 360 pF	10		ns
t_{dis}	Output disable time (3-state outputs)	C_L = 360 pF		90	ns
t_{en}	Output enable time (3-state outputs)	C_L = 360 pF		55	ns
$t_{CAV-CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low after refresh (see Note 13)	C_L = 360 pF	0		ns
t_{CH-CEL}	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 14)	C_L = 360 pF		140	ns
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 360 pF		20	ns
$t_{t(CEH)}$	$\overline{CAS}$ rise time	C_L = 360 pF		30	ns
$t_{t(REL)}$	$\overline{RAS}$ fall time	C_L = 180 pF		20	ns
$t_{t(REH)}$	$\overline{RAS}$ rise time	C_L = 180 pF		30	ns
$t_{t(MAV)}$	Address transition time	C_L = 360 pF		30	ns
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		20	ns
$t_{t(RYH)}$	RDY rise time	C_L = 40 pF		27	ns

†See Parameter Measurement Information for load circuit and waveforms.

NOTES: 13. The occurrence of $\overline{CAS}$ low is guaranteed not to occur until the column address is valid on MAX.

14. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low. (See Refresh Cycle Timing Diagram)

TYPICAL CHARACTERISTICS



†Load is 360 pF for $\overline{CAS}$ and MA outputs, 180 pF, for all $\overline{RAS}$ outputs.

FIGURE 5

PARAMETER MEASUREMENT INFORMATION

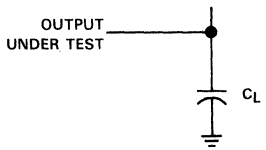
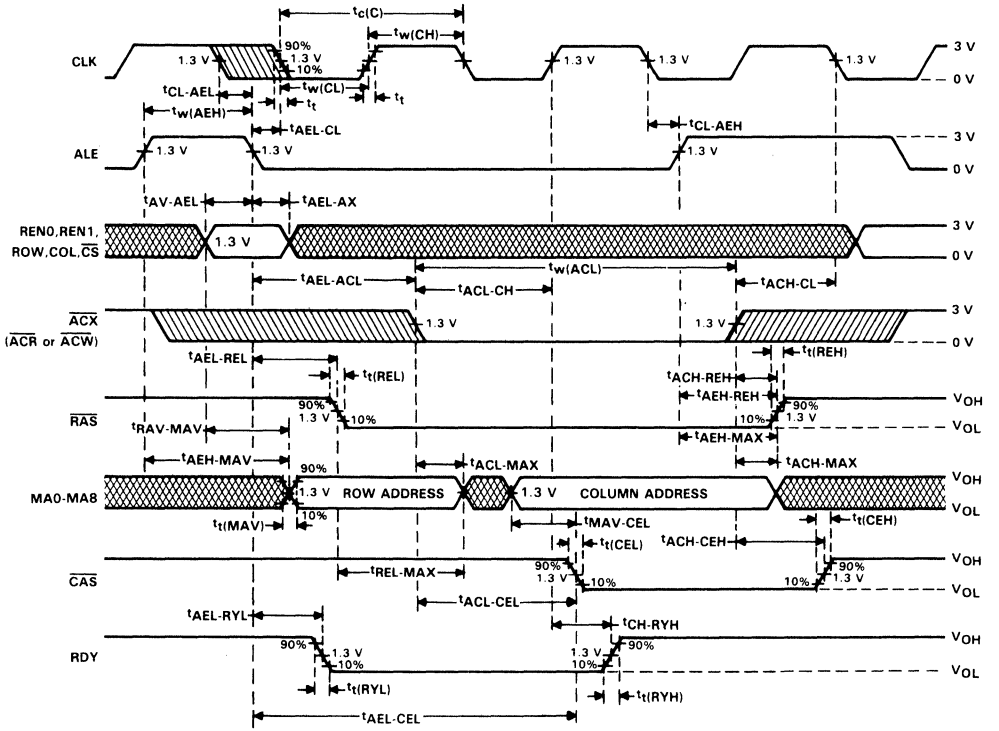


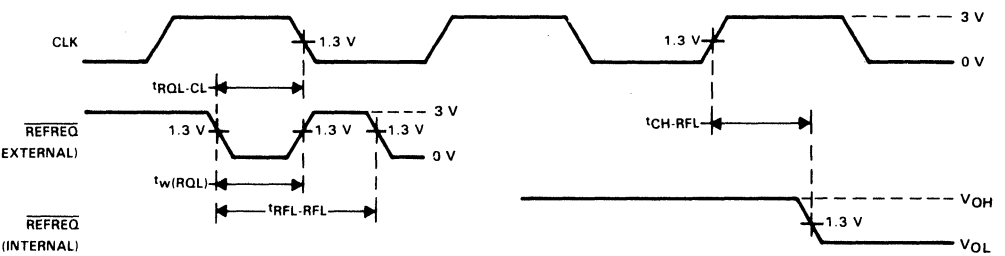
FIGURE 6. LOAD CIRCUIT

PARAMETER MEASUREMENT INFORMATION



NOTE 15: All transition times (t_r) are measured between 10% and 90% points.

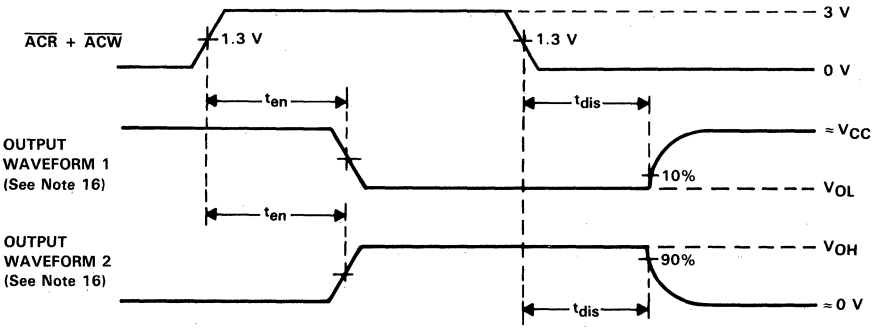
FIGURE 7: ACCESS CYCLE TIMING



NOTE 16: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 8. REFRESH REQUEST TIMING

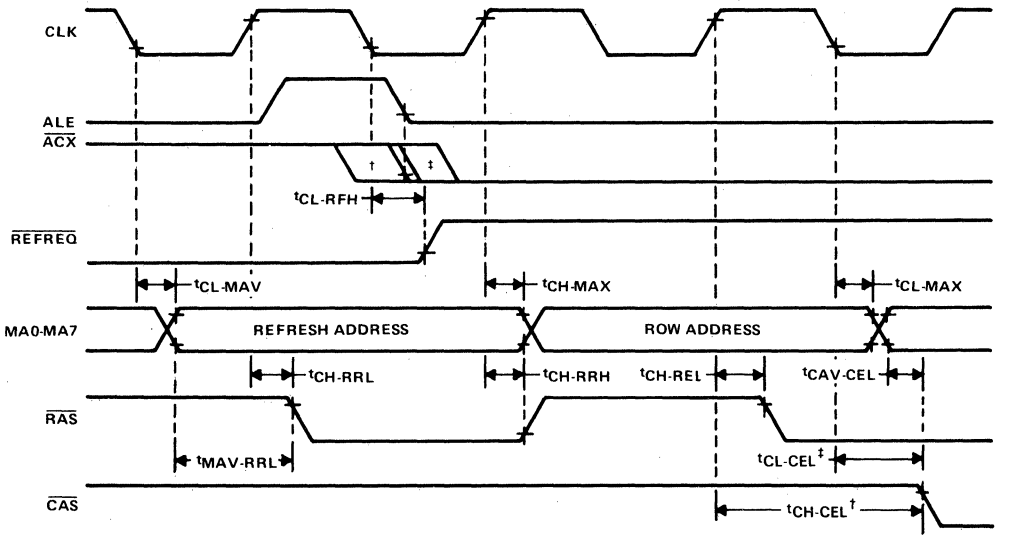
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE 16: Waveform 1 is an output with internal conditions such that the output is low except when disabled by the access controls. Waveform 2 is an output with internal conditions such that the output is high except when disabled by the access controls.

FIGURE 9. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

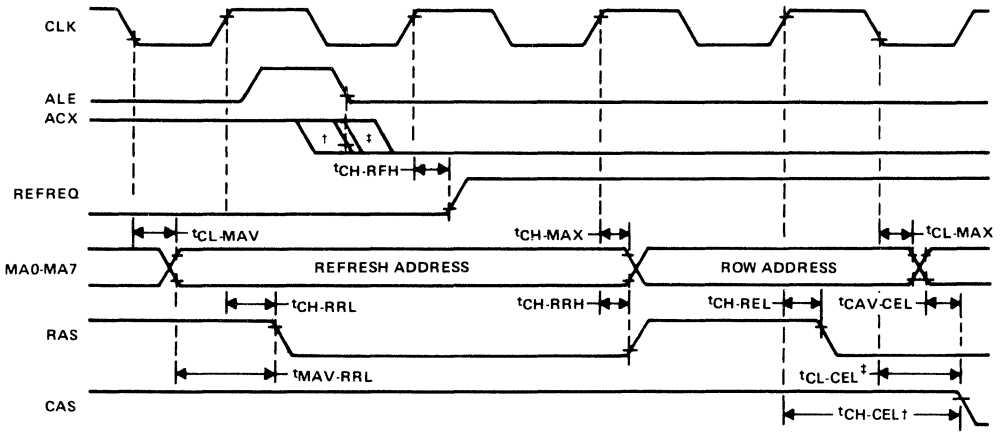


†On access grant cycle following refresh, CAS low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if ACX low occurs prior to or coincident with the falling edge of ALE.
‡On access grant cycle following refresh, CAS low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if ACX low occurs 20 ns or more after the falling edge of ALE.

FIGURE 10. REFRESH CYCLE TIMING (THREE-CYCLE)

NOTE 17: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

PARAMETER MEASUREMENT INFORMATION



†On access grant cycle following refresh, CAS low and address multiplexing are timed from CLK high transition (t_{CH-CEL}) if ACX low occurs prior to or coincident with the falling edge of ALE.

‡On access grant cycle following refresh, CAS low and address multiplexing are timed from CLK low transition (t_{CL-CEL}) if ACX low occurs 20 ns or more after the falling edge of ALE.

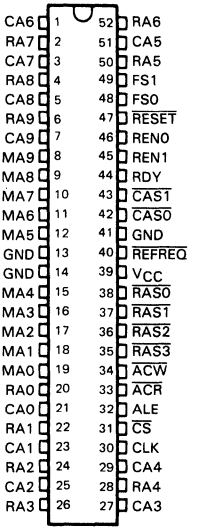
NOTE 16: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 11. REFRESH CYCLE TIMING (FOUR-CYCLE)

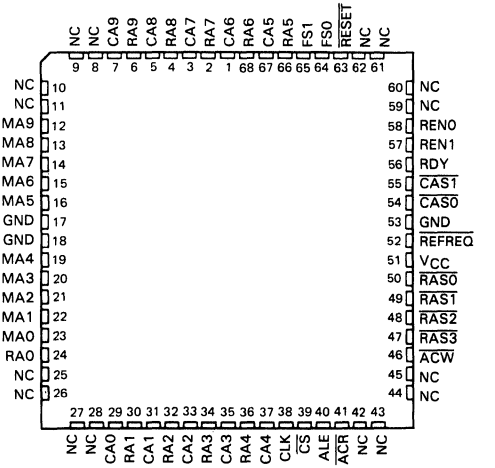
D3132, SEPTEMBER 1988—REVISED MAY 1989

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K, 256K, and 1M Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 4 Banks of Memory
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous $\overline{\text{RESET}}$
  - Choice of CLK Polarity on Refresh/Access Arbitration
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Refresh Frequencies for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range:
  100 ns ALE low to $\overline{\text{CAS}}$ low
- Functionally Compatible with TMS4500A/B and with THCT4502B
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

JD OR N PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

The 'ACT4503 is a monolithic DRAM system controller providing address multiplexing, timing, control, and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

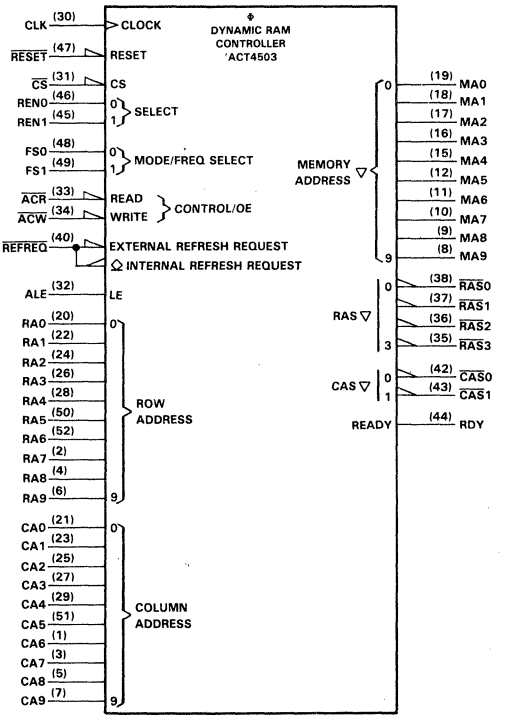
The controller contains an 20-bit multiplexer that generates the address lines for the memory device from the 20 system address bits and provides the strobe signals required by the memory to decode the address. A 10-bit refresh counter generates up to 1024 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The 'ACT4503 also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles. In order to guarantee correct refresh/access arbitration, the falling edge of ALE must not occur within a specified time period of either the rising or falling edge of CLK. The selection of the arbitration CLK edge is determined during reset (Figure 15). Knowing the processor's ALE to CLK timing relationship allows the designer to select the proper CLK edge to guarantee refresh/access arbitration on the 'ACT4503.

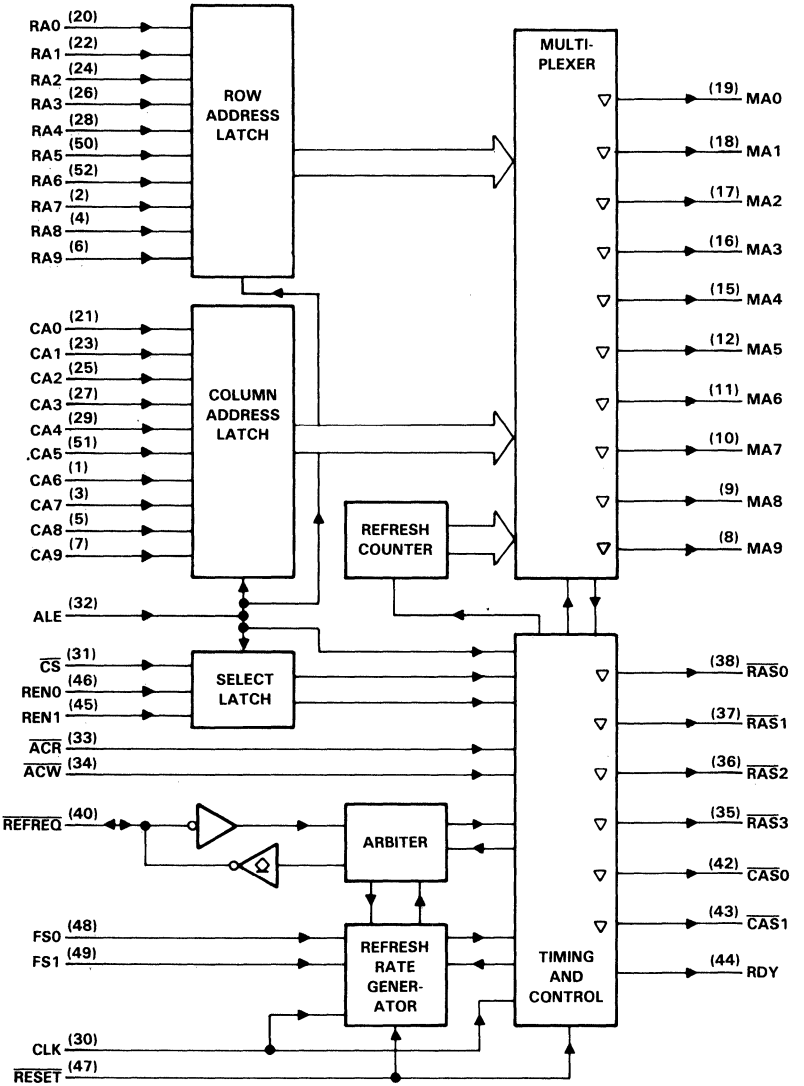
The SN74ACT4503 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984.
Pin numbers shown are for JD and N packages.

functional block diagram†



†Pin numbers shown are for JD and N packages.

TERMINAL FUNCTIONS

PIN NAME	PIN NO.†	I/O	DESCRIPTION
$\overline{ACR}$	33 [41]	I	Access Control, Read. A low on this input causes the column address to appear on MA0-MA9 and a low-going pulse from CAS.The rising edge of ACR or ACW terminates the cycle by forcing RAS and $\overline{CAS}$ high. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA9, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$, and $\overline{CAS1}$ go into a high-impedance state.
ACW	34 [46]	I	Access Control, Write. A low on this input causes the column address to appear on MA0-MA9 and a low-going pulse from $\overline{CAS}$. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by forcing $\overline{RAS}$ and $\overline{CAS}$ high. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA9, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$, and $\overline{CAS1}$ go into a high-impedance state.
ALE	32 [40]	I	Address Latch Enable. This input is used to latch the 20 address inputs, $\overline{CS}$, REN0, and REN1. This also initiates an access cycle if $\overline{CS}$ is low. The rising edge (low level to high level) of ALE returns all $\overline{RAS}$ outputs to the high level.
CA0	21 [29]	I	Column Address. These address inputs are used to generate the column address for the multiplexer.
CA1	23 [31]		
CA2	25 [33]		
CA3	27 [35]		
CA4	29 [37]		
CA5	51 [67]		
CA6	1 [1]		
CA7	3 [3]		
CA8	5 [5]		
CA9	7 [7]		
$\overline{CAS0}$	42 [54]	O	Column Address Strobe. These 3-state outputs are used to latch the column address into the DRAM array.
$\overline{CAS1}$	43 [55]		
CLK	30 [38]	I	System Clock. This input provides the master timing to generate refresh and access cycle timings and refresh rate. Refresh rate is determined by the FS1 and FS0 inputs.
$\overline{CS}$	31 [39]	I	Chip Select. A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
FS0	48 [64]	I	Frequency Select. These strap inputs are used to select Mode and Frequency of operation. The Strap Configuration table shows the input frequencies and internal refresh frequencies. Device operation mode can be chosen by controlling these Frequency Select pins during $\overline{RESET}$ low. The operating modes are shown in the Operation Mode Selection table. After $\overline{RESET}$ goes high, FS0 and FS1 must be set to the correct strap input levels to indicate the corresponding refresh rate for the input frequency.
FS1	49 [65]		
MA0	19 [23]	O	Memory Address. These 3-state outputs are designed to drive the addresses of the dynamic RAM array.
MA1	18 [22]		
MA2	17 [21]		
MA3	16 [20]		
MA4	15 [19]		
MA5	12 [16]		
MA6	11 [15]		
MA7	10 [14]		
MA8	9 [13]		
MA9	8 [12]		
RA0	20 [24]	I	Row Address. These address inputs are used to generate the row address for the multiplexer.
RA1	22 [30]		
RA2	24 [32]		
RA3	26 [34]		
RA4	28 [36]		

†Pin numbers shown are for the JD and N packages and parenthetically for the FK and FN packages.

TERMINAL FUNCTIONS (continued)

PIN NAME	PIN NO.†	I/O	DESCRIPTION
RA5 RA6 RA7 RA8 RA9	50 [66] 52 [68] 2 [2] 4 [4] 6 [6]	I	Row Address. These address inputs are used to generate the row address for the multiplexer.
$\overline{RAS}$0 $\overline{RAS}$1 $\overline{RAS}$2 $\overline{RAS}$3	38 [50] 37 [49] 36 [48] 35 [47]	O	Row Address Strobe. These 3-state outputs are used to latch the row address into the bank of DRAMs selected by REN0 and REN1. On refresh, all $\overline{RAS}$ signals are active.
$\overline{REFREQ}$	40 [52]	I/O	Refresh Request. This input should be driven by an open-collector or open-drain output. On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next arbitration edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next arbitration edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA9. (Note: $\overline{REFREQ}$ contains an internal active pullup with a nominal resistance of 5 kΩ, which is disabled when $\overline{REFREQ}$ is low).
REN0 REN1	46 [58] 45 [57]	I	RAS Enable. These inputs are used to select one of four banks of RAM when $\overline{CS}$ is low. When REN1 is low, the lower banks are enabled via $\overline{CAS}$0, $\overline{RAS}$0, and $\overline{RAS}$1. When REN1 is high, the higher banks are enabled via $\overline{CAS}$1, $\overline{RAS}$2, and $\overline{RAS}$3, REN0 selects $\overline{RAS}$0 and $\overline{RAS}$2 when low, or $\overline{RAS}$1 and $\overline{RAS}$3 when high (see Output Strobe Selection table).
$\overline{RESET}$	47 [63]	I	$\overline{RESET}$. Active-low input to initialize the controller asynchronously. Refresh address is set to 3FF. Internal refresh requests, synchronizer, and frequency divide are cleared. Row address hold time is calibrated to the input clock frequency after the $\overline{RESET}$ low-to-high transition. The calibration takes up to 15 clock cycles, during which an access request is treated as if it occurred during a refresh cycle. After the initial calibration, hold time is automatically calibrated once every refresh cycle and requires the same number of clock cycles as a refresh.
RDY	44 [56]	O	Ready. This totem-pole output signals the occurence of an access grant cycle, which occurs when an access request is generated during a refresh cycle. The RDY output signals the processor to wait when this type of cycle occurs.

†Pin numbers shown are for the JD and N packages and parenthetically for the FK and FN packages.

STRAP CONFIGURATION

STRAP INPUT LEVELS		REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	MAXIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
FS1	FS0					
L	L	CLK/61	3.904	5.824	64-95	3
H	H	CLK/91	5.824	7.744	64-85	4
H	L	CLK/121	7.744	8.704	64-72	4
L	H	CLK/136	8.704	10.50	64-77	4

OPERATION MODE SELECTION

SELECTION	OPERATION MODES
FS0-L	Access/refresh arbitration on high-to-low clock edge
FS0-H	Access/refresh arbitration on low-to-high clock edge
FS1-L	Refresh cycles initiated internally
FS1-H	Refresh cycles initiated externally. Internal refresh timer disabled.

OUTPUT STROBE SELECTION

CONTROL INPUT		SELECTED OUTPUT					
REN1	REN0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$	$\overline{CAS1}$
L	L	X				X	
L	H		X			X	
H	L			X			X
H	H				X		X

functional description

The 'ACT4503 consists of six basic blocks: address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the outputs MA0-MA9 follows the inputs RA0-RA9.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in the Strap Configuration table. The counter is reset when a refresh cycle is requested or when $\overline{RESET}$ is low. The configuration straps allow the matching of memories to the system access time. Upon power-up, it is necessary to provide a reset signal by driving $\overline{RESET}$ low. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. A low-to-high transition on $\overline{RESET}$ sets the refresh counter to $3FF_{16}$ (1023_{10}).

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 20 multiplexed addresses on 10 lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle (RDY = L) when an access request occurs during a refresh cycle. Arbitration can be configured, during the reset cycle, to operate on either clock edge.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{RAS}$ and $\overline{CAS}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

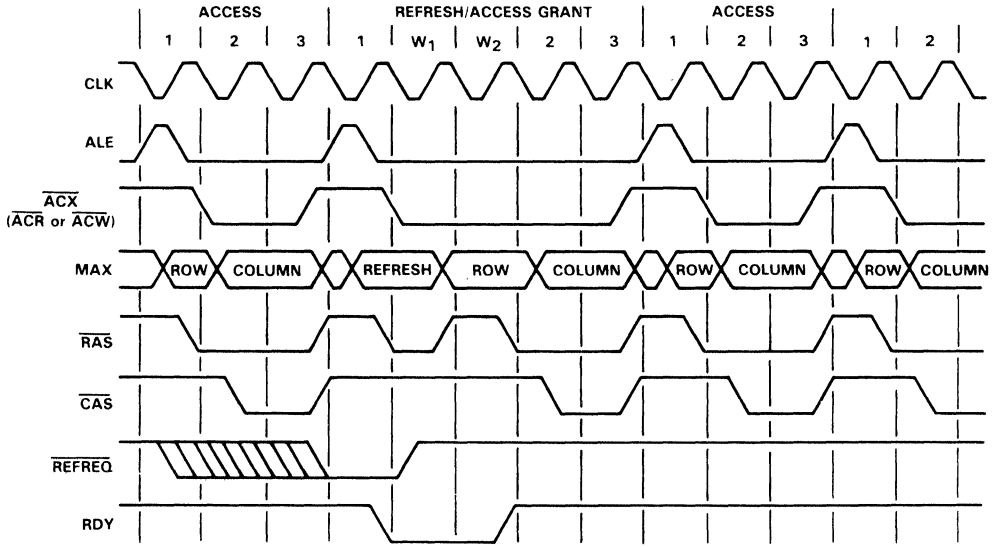


FIGURE 1. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)

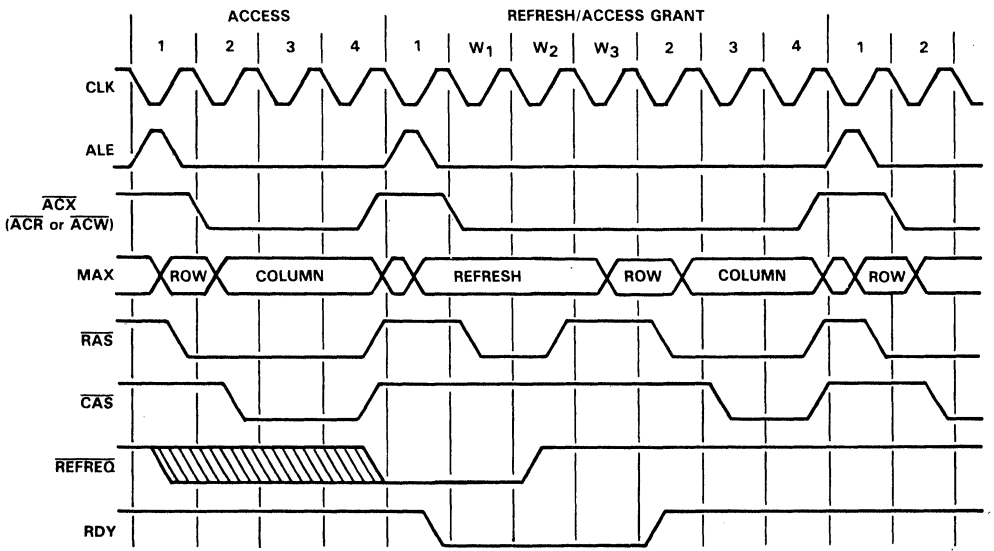


FIGURE 2. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)

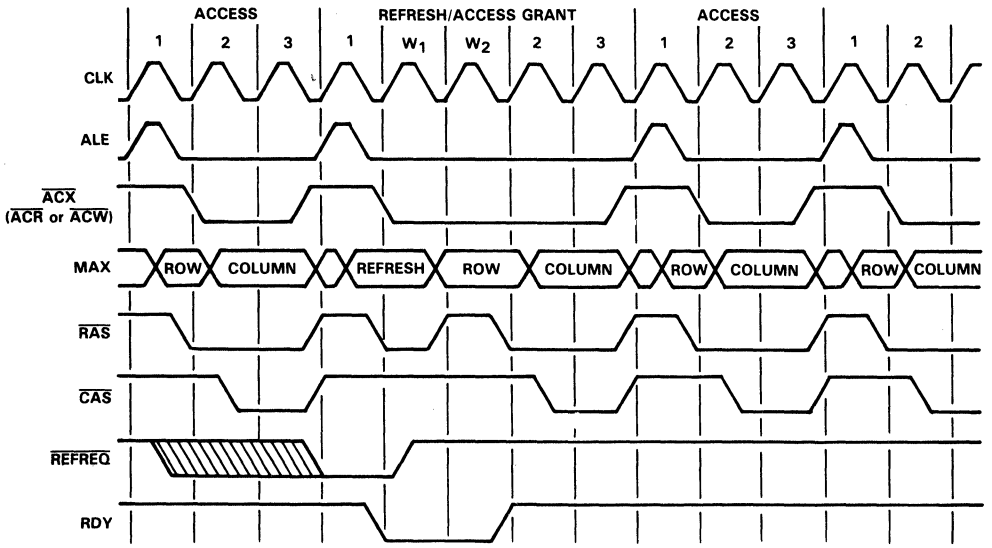


FIGURE 3. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)

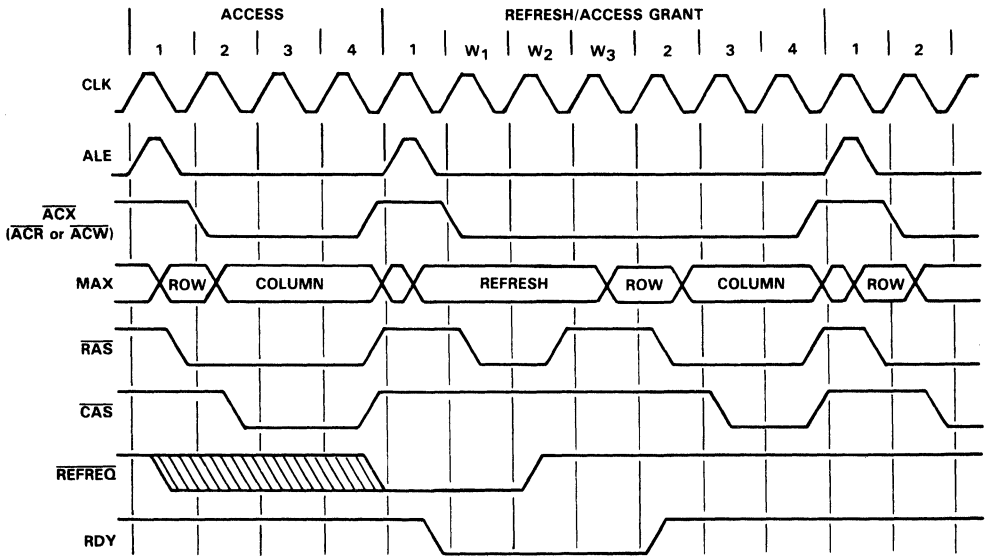


FIGURE 4. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (See Note 1) . . . . . −1.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$, $V_I > V_{CC}$) . . . . . ±20 mA
Output diode current, I_{OK} ($V_O < 0$, $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND pins . . . . . ±70 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or JD package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package . . . . . 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	−0.5†		0.8	V
V_O	Output voltage	−0.5‡		V_{CC}+0.5	V
t_t	Input transition (rise and fall) time	0		100	ns
T_A	Operating free-air temperature	0		70	°C

‡The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for input and output voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
V_{OH}	High-level output voltage	$\overline{REFREQ}$	I_{OH} = −20 μA	4.5 V	4			3.8		V
		All others	I_{OH} = −8 mA	4.5 V	3.8			3.7		
V_{OL}	Low-level output voltage		I_{OL} = 8 mA	4.5 V			0.4		0.4	V
I_{IH}	High-level input current	$\overline{REFREQ}$	V_I = 5.5 V	5.5 V			15		20	μA
		All others					0.1		1	
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0 V	5.5 V			−2		−2	mA
		All others					−0.5		−1	μA
I_{OZ}§	Off-state output current (3-state outputs only)		V_O = 0 to 5.5 V	5.5 V			20		20	μA
I_{CC}¶	Supply current (operative)		All inputs at V_{IL} or V_{IH}	5.5 V		30	40		50	mA
ΔI_{CC}#	Supply current change		One input at 0.5 or 2.4 V, All others at 0 V or V_{CC}	5.5 V		0.5	1		1	mA
C_i	Input capacitance		V_I = 0 V, f = 1 MHz	5.5 V		5	10		10	pF

§This parameter, I_{OZ}, the high-impedance-state output current, applies only for three-state outputs and transceiver I/O pins.
¶I_{CC} is measured with none of the memory address (MA0-MA9) outputs switching.
#This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 180 pF		14	20	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	C_L = 360 pF		20	30	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	C_L = 360 pF		21	30	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low	C_L = 40 pF		14	20	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Notes 2 and 5)	C_L = 360 pF	40	65	100	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	C_L = 180 pF		14	20	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$	C_L = 360 pF	12	25		ns
$t_{MAV-CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low	C_L = 360 pF	5	18		ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 2)	C_L = 360 pF	30	50	75	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	C_L = 180 pF		15	25	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	C_L = 360 pF	5	13	20	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	C_L = 360 pF	10	27		ns
t_{C-RYH}	Time delay, CLK high to RDY starting high (see Note 3)	C_L = 40 pF		12	20	ns
t_{C-RFL}	Time delay, CLK to $\overline{REFREQ}$ internal starting low	C_L = 40 pF		16	26	ns
t_{C-MAV}	Time delay, CLK to refresh address valid	C_L = 360 pF		32	50	ns
t_{C-RRL}	Time delay, CLK to refresh $\overline{RAS}$ starting low	C_L = 180 pF	10	20	40	ns
t_{C-RFH}	Time delay, CLK to REFREQ starting high	C_L = 40 pF R_L = 1 kΩ		35	50	ns
t_{C-RRH}	Time delay, CLK to refresh $\overline{RAS}$ starting high	C_L = 180 pF	10	17	25	ns
t_{C-MAX}	Refresh address valid after CLK	C_L = 360 pF	12	29		ns
t_{C-REL}	Time delay, CLK to access $\overline{RAS}$ starting low	C_L = 180 pF		19	30	ns
t_{C-CEL}	Time delay, CLK to access $\overline{CAS}$ starting low (see Notes 4 and 5)	C_L = 360 pF		65	105	ns
$t_{REL-MAX}$	Row address valid after $\overline{RAS}$ low (see Note 5)	C_L = 360 pF	20	22		ns
$t_{AEH-MAX}$	Column address valid after ALE high	C_L = 360 pF	15	29		ns
t_{dis}	Output disable time (3-state outputs)	C_L = 360 pF		48	60	ns
t_{en}	Output enable time (3-state outputs)	C_L = 360 pF		30	50	ns
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 360 pF		6	10	ns
$t_{(CEH)}$	$\overline{CAS}$ rise time	C_L = 360 pF		7.5	15	ns
$t_{t(REL)}$	$\overline{RAS}$ fall time	C_L = 180 pF		4.2	10	ns
$t_{t(REH)}$	$\overline{RAS}$ rise time	C_L = 180 pF		5	10	ns
$t_{t(MAV)}$	Address transition time	C_L = 360 pF		15	30	ns
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		2	6	ns
$t_{t(RYH)}$	RDY rise time	C_L = 40 pF		1.5	5	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

NOTES: 2. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

3. On an access grant cycle, RDY returns high on the edge of CLK that drives the access $\overline{RAS}$ low.
4. The occurrence of $\overline{CAS}$ low is guaranteed not to occur until the column address is valid on memory address (MAX).
5. Measurements are made at 10 MHz CLK frequency with FS0 and FS1 low. For each strap configuration, these parameters will be a minimum for the maximum allowed CLK frequency, and will increase with decreasing frequency.

timing requirements over recommended ranges of supply voltage and operating free-air temperature† (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
$t_{c(C)}$	CLK cycle time	90		ns
$t_{w(CH)}$	CLK high pulse duration	23		ns
$t_{w(CL)}$	CLK low pulse duration	23		ns
t_{AEL-C}	Time delay, ALE low to CLK (see Note 6)	20		ns
t_{C-AEL}	Time delay, CLK to ALE starting low (see Note 6)	0		ns
t_{C-AEH}	Time delay, CLK to ALE starting high (see Note 7)	0		ns
$t_{w(AEH)}$	Pulse duration ALE high	20		ns
t_{AV-AEL}	Time delay, address, REN0, REN1, $\overline{CS}$ valid to ALE low	5		ns
t_{AEL-AX}	Time delay, ALE low to address not valid	10		ns
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 8, 9, and 10)	$t_{h(RA)}+30$		ns
t_{ACH-C}	Time delay, $\overline{ACX}$ high to CLK (see Notes 8 and 11)	30		ns
t_{RQL-C}	Time delay, $\overline{REFREQ}$ low to CLK (see Note 12)	20		ns
$t_{w(RQL)}$	Pulse duration $\overline{REFREQ}$ low	10		ns
$t_{w(ACL)}$	Pulse duration $\overline{ACX}$ low (see Note 13)	20		ns
$t_{su(RST)}$	FS0 and FS1 before $\overline{RESET}$↑ (see Figure 15)	$3t_cCLK$		ns
$t_{h(RST)}$	FS0 and FS1 after $\overline{RESET}$↑ (see Figure 15)	0		ns
t_{reset}	Power-up reset	$4t_cCLK$		ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

NOTES:
6. In order to guarantee correct refresh/access arbitration, the falling edge of ALE must not occur within 20 ns before to 0 ns after the arbitration clock edge. The arbitration clock edge is selected during reset via FS0 and FS1. (See Figure 11).
7. If ALE rises before $\overline{ACX}$ and a refresh request is present, the next refresh/access edge of CLK after t_{C-AEH} will output the refresh address to MA0-MA9 and initiate a refresh cycle.
8. These specifications relate to system timing and do not directly reflect device performance.
9. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
10. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
11. The minimum of 30 ns is specified to ensure arbitration will occur on the next refresh/access CLK edge. t_{ACH-C} also affects precharge time such that the minimum t_{ACH-C} should be equal or greater than $t_{w(RH)} - t_{w(C)} + 30$ ns (for a cycle in which ACX high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM RAS precharge time. $t_{w(C)}$ represents CLK low pulse duration $t_{w(CL)}$ for three-cycle refresh with high-to-low CLK-edge arbitration, CLK high pulse duration $t_{w(CH)}$ for three-cycle refresh with low-to-high CLK edge arbitration, and CLK period $t_{c(C)}$ for four-cycle refresh.
12. This parameter is necessary only if refresh arbitration is to occur on this refresh/access arbitration CLK edge (in systems in which refresh is synchronized to external events).
13. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

PARAMETER MEASUREMENT INFORMATION

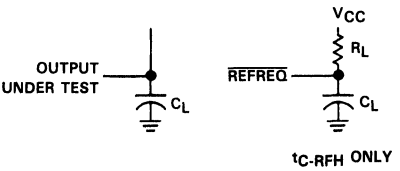
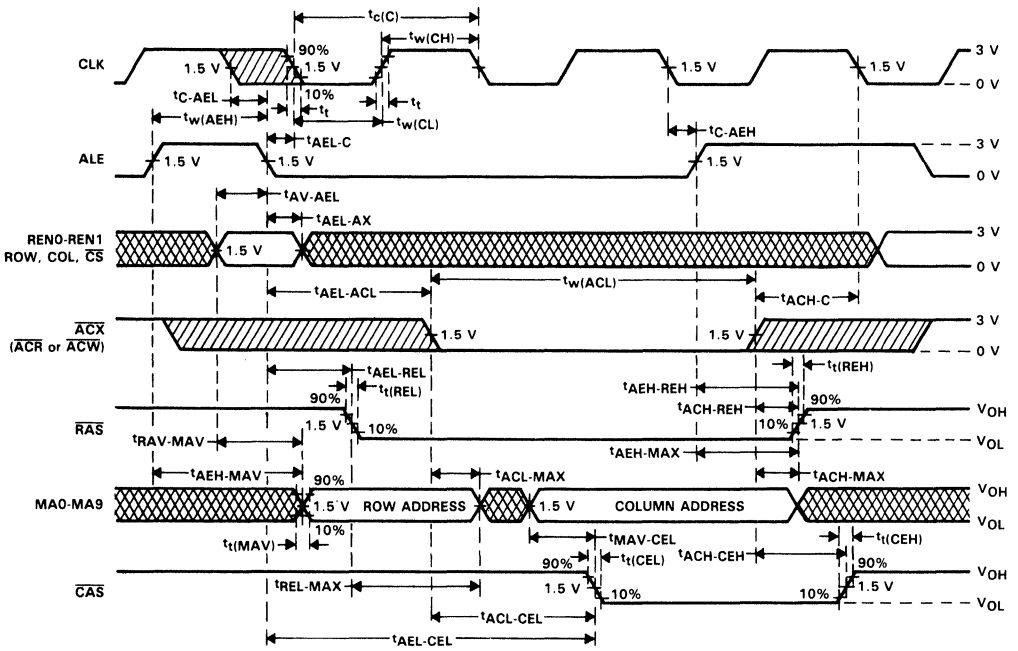


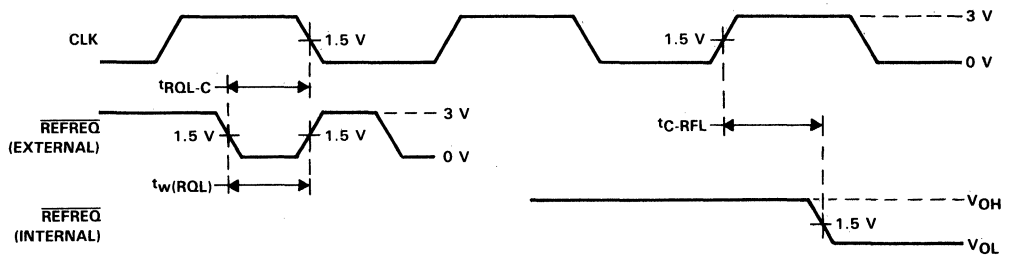
FIGURE 5. LOAD CIRCUITS



NOTE 14: All transition times (t_t) are measured between 10% and 90% points.

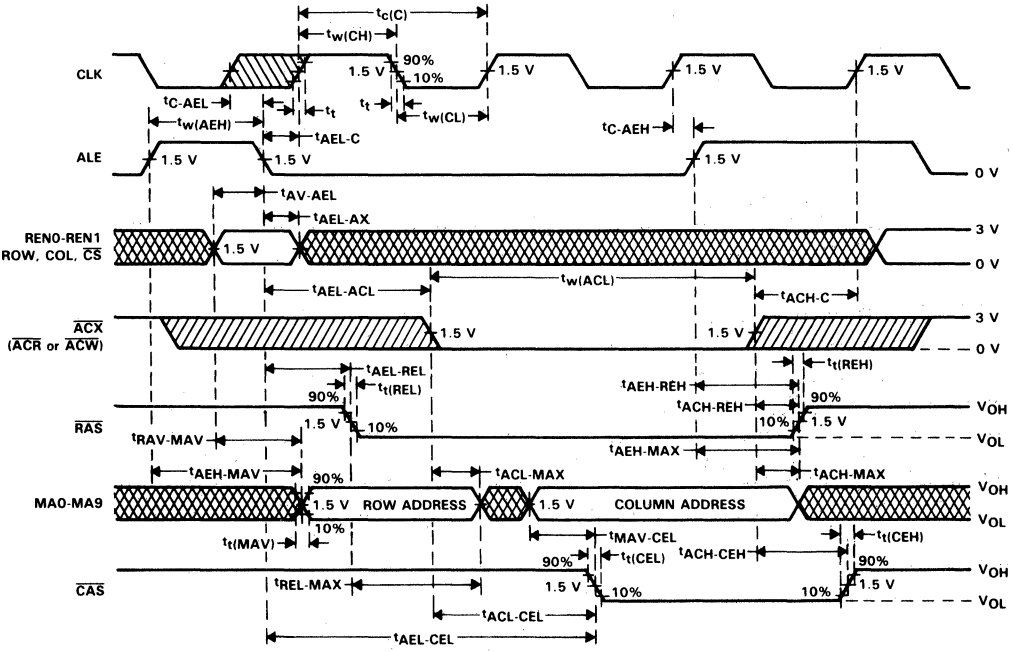
FIGURE 6. ACCESS CYCLE TIMING (HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)

PARAMETER MEASUREMENT INFORMATION



NOTE 15. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 7. REFRESH REQUEST TIMING (HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)



NOTE 14: All transition times (t_t) are measured between 10% and 90% points.

FIGURE 8. ACCESS CYCLE TIMING (LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)

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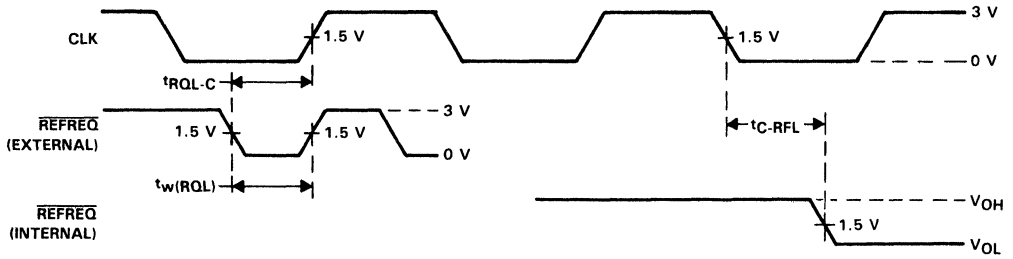
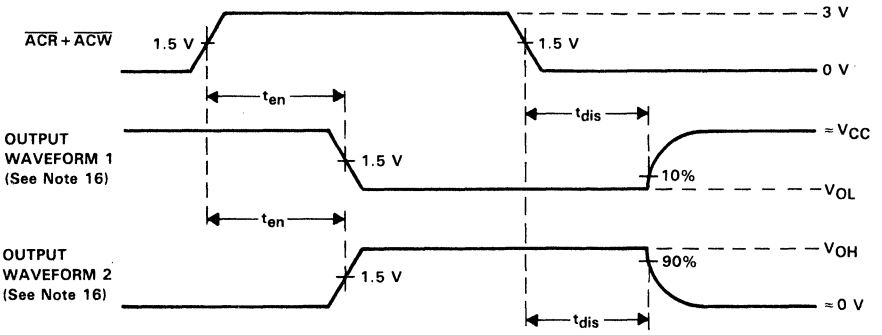
PARAMETER MEASUREMENT INFORMATION



NOTE 15. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 9. REFRESH REQUEST TIMING (LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)

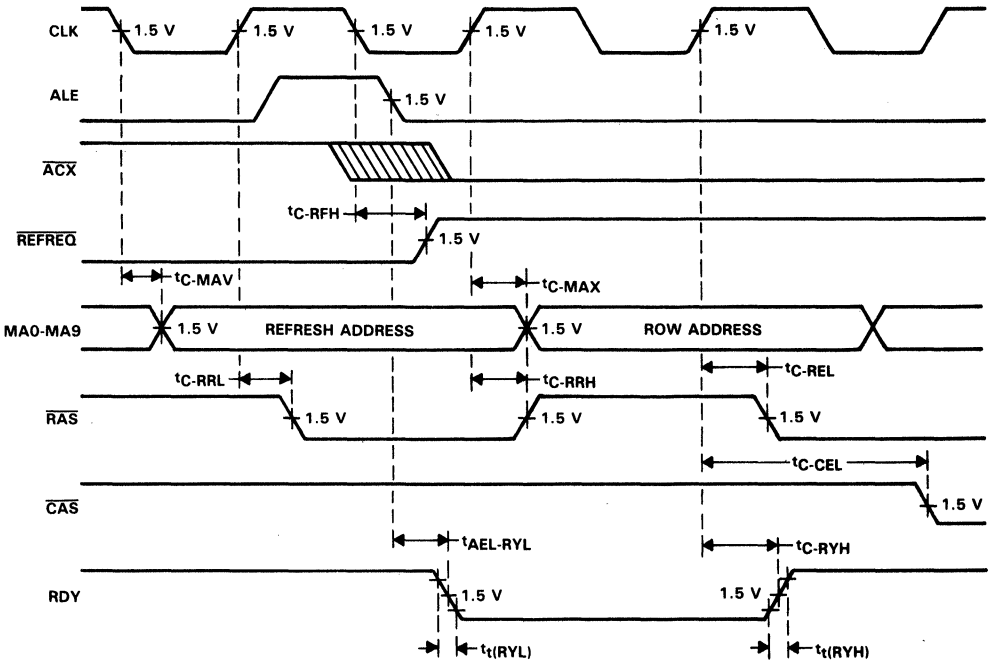


VOLTAGE WAVEFORMS

NOTE 16: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the access controls. Waveform 2 is an output with internal conditions such that the output is high except when disabled by the access controls.

FIGURE 10. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

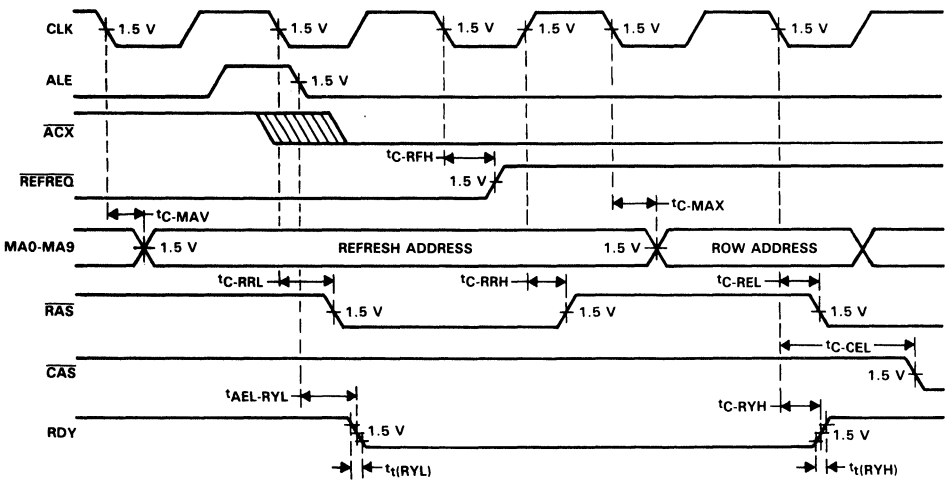
PARAMETER MEASUREMENT INFORMATION



NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 11. REFRESH CYCLE TIMING (THREE CYCLE, HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)

PARAMETER MEASUREMENT INFORMATION



NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 12. REFRESH CYCLE TIMING (FOUR CYCLE, HIGH-TO-LOW CLK REFRESH/ACCESS ARBITRATION)

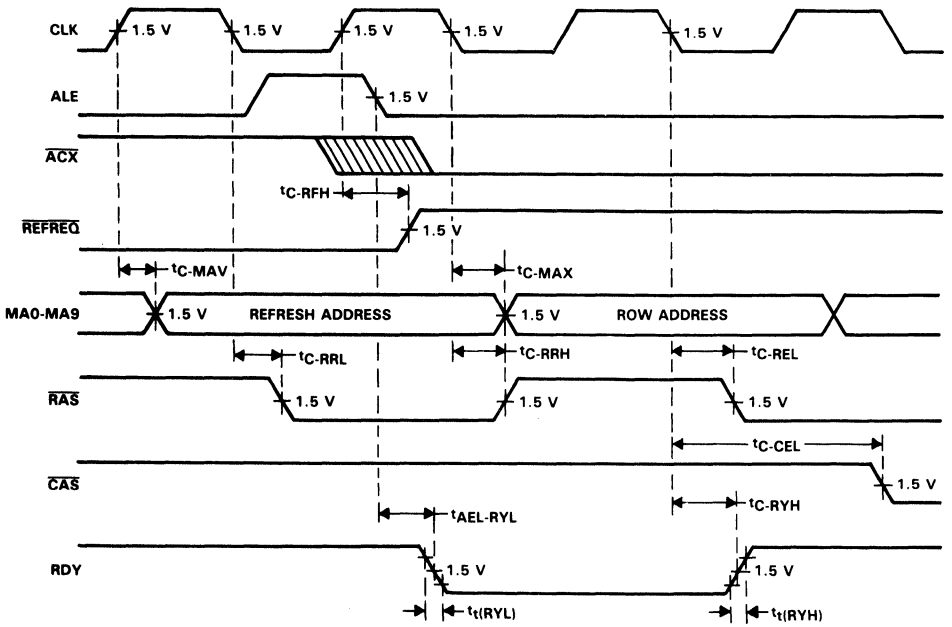
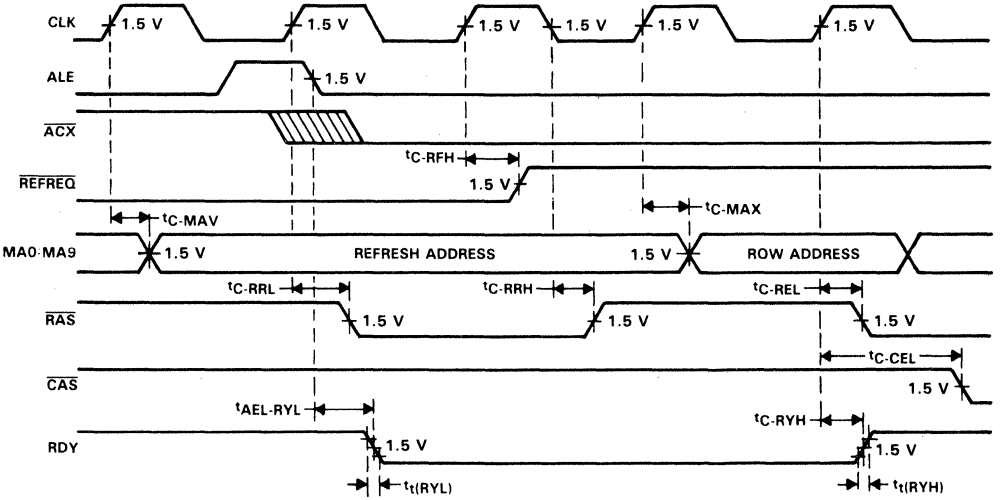


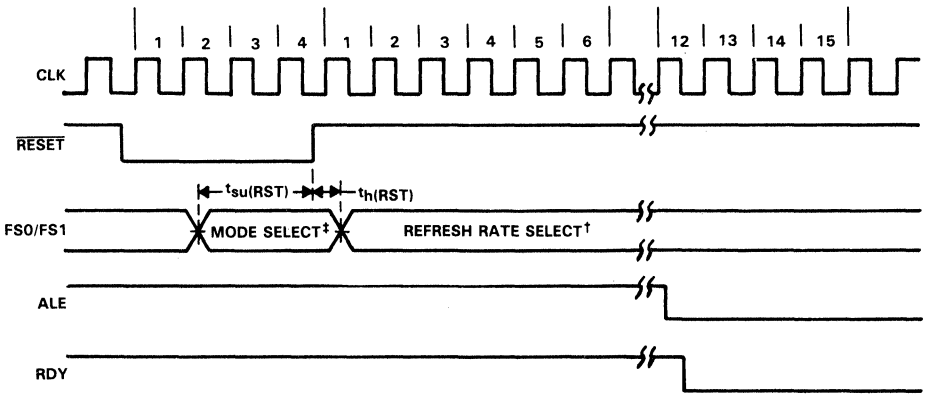
FIGURE 13. REFRESH CYCLE TIMING (THREE CYCLE, LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)

PARAMETER MEASUREMENT INFORMATION



NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 14. REFRESH CYCLE TIMING (FOUR CYCLE, LOW-TO-HIGH CLK REFRESH/ACCESS ARBITRATION)



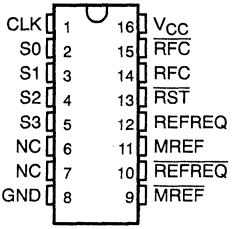
†See Strap Configuration table.
‡See Operation Mode Selection table.

FIGURE 15. RESET CYCLE TIMING

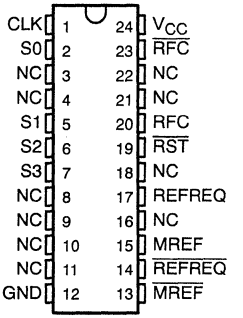
D3311, DECEMBER 1989–REVISED JULY 1990

- **Supports 16 Most Popular Microprocessor Speeds**
- **Supports Distributive- and Hidden-Refresh Operations**
- **Polarity Options Available for RFC, REFREQ, and MREF Signals**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

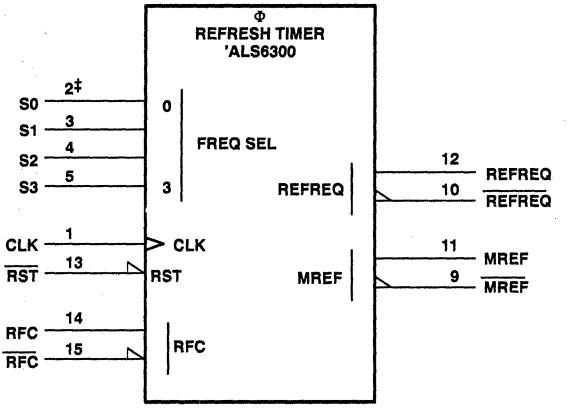
The 'ALS6300 input-selectable memory refresh timer allows the user to select one of sixteen popular divisor rates in order to generate appropriate refresh timing control signals to a memory timing control device. The flexible divide-by rates are based on the most widely used microprocessor clock frequencies and the most common dynamic RAM refresh timing requirements. In addition, this device supports both distributive- and hidden-refresh strategy by providing a refresh request signal (REFREQ) and a mandatory refresh signal (MREF). For design flexibility, the 'ALS6300 provides both active-high and active-low refresh request outputs (REFREQ and $\overline{\text{REFREQ}}$), mandatory refresh outputs (MREF and $\overline{\text{MREF}}$), and refresh-complete inputs (RFC and $\overline{\text{RFC}}$).

The DRAM memory refresh timer is basically a programmable frequency divider with special modifications to enhance its use as a refresh timer. The divisor rate is selected by applying the appropriate logic levels to the S0-S3 inputs shown in Table 1. When the internal counter reaches the selected divisor rate, REFREQ and $\overline{\text{REFREQ}}$ will go active (high and low, respectively) and stay active until an active level is seen on the RFC or $\overline{\text{RFC}}$ input. The 'ALS6300 will automatically generate a mandatory refresh signal, MREF and $\overline{\text{MREF}}$, if an active RFC or $\overline{\text{RFC}}$ is not received before 20 clock cycles before the next request. An active level on the RFC or $\overline{\text{RFC}}$ input will force REFREQ, $\overline{\text{REFREQ}}$, MREF, and $\overline{\text{MREF}}$ to their inactive states.

To achieve distributive refresh, either REFREQ, $\overline{\text{REFREQ}}$, MREF, or $\overline{\text{MREF}}$ can be used to activate the refresh cycle. When using hidden refresh, an active level on either REFREQ or $\overline{\text{REFREQ}}$ indicates that a refresh cycle should be performed immediately after the next memory access cycle. MREF or $\overline{\text{MREF}}$ is used to indicate that an access has not occurred during the given refresh period and to force the timing controller to initiate a refresh cycle within the next 20 clock periods.

A low level on the $\overline{\text{RST}}$ input clears the internal counter and sets the REFREQ, $\overline{\text{REFREQ}}$, MREF, and $\overline{\text{MREF}}$ outputs to their inactive state on the next active clock edge.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.
‡ Pin numbers are for N package.

logic diagram (positive logic)

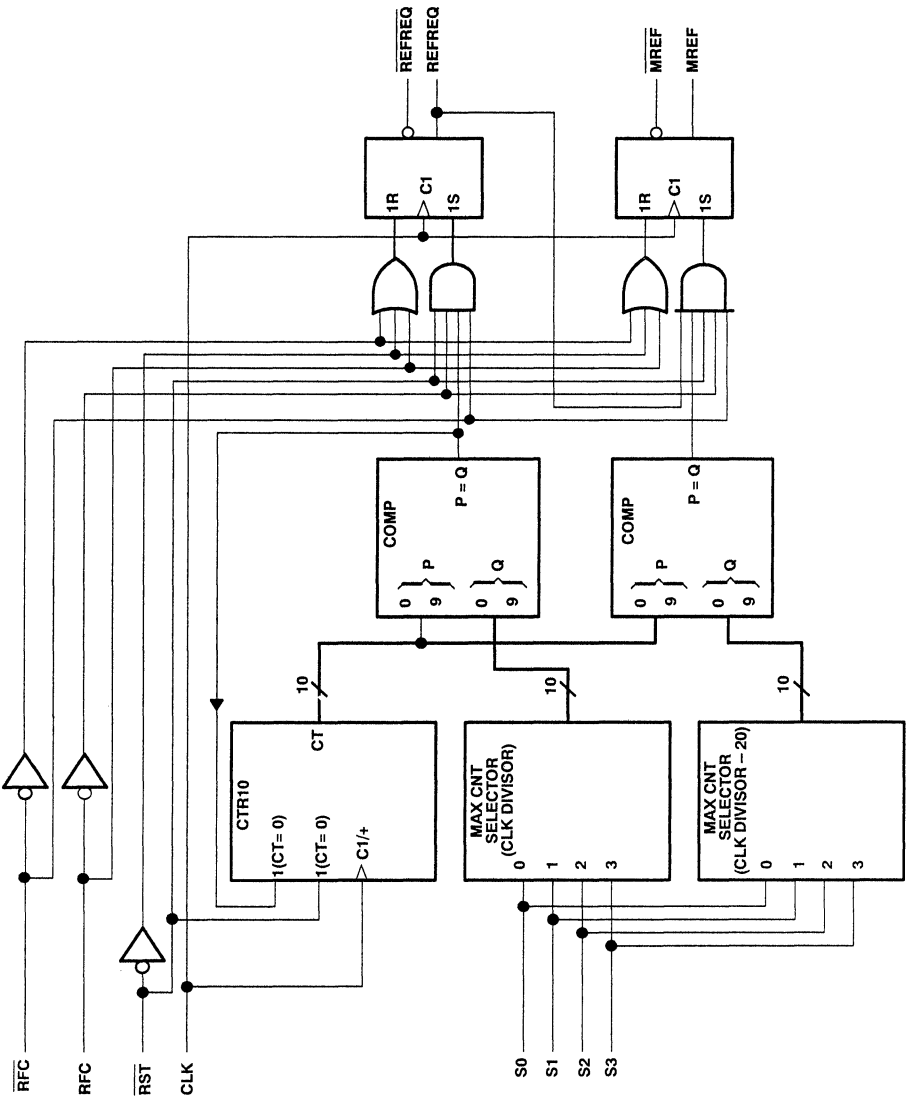


Table 1. System Clock Selection

SELECT INPUTS				CPU CLOCK FREQUENCY (MHz)	CLOCK DIVISOR	REFRESH PERIOD (μs)	% CHANCE OF HIDDEN REFRESH
S3	S2	S1	S0				
L	L	L	L	5	77	15.4	74.0
L	L	L	H	6	93	15.5	78.5
L	L	H	L	7.5	116	15.5	82.8
L	L	H	H	8	124	15.5	83.9
L	H	L	L	10	155	15.5	87.1
L	H	L	H	11	171	15.5	88.3
L	H	H	L	12	186	15.5	89.2
L	H	H	H	12.5	194	15.5	89.7
H	L	L	L	15	233	15.5	91.4
H	L	L	H	16	248	15.5	91.9
H	L	H	L	18	280	15.5	92.9
H	L	H	H	20	310	15.5	93.5
H	H	L	L	24	373	15.5	94.6
H	H	L	H	25	389	15.6	94.9
H	H	H	L	33	511	15.5	96.1
H	H	H	H	40	625	15.6	96.8

Terminal Functions

PIN NAME	PIN NO.†	DESCRIPTION
CLK	1	System clock input provides the base time period for the divider.
S0-S3	2-5	Frequency Select inputs select the desired clock divisor for the system clock according to Table 1.
$\overline{RST}$	13	Reset input, when low, synchronously clears the internal counter and sets $\overline{REFREQ}$ and $\overline{MREF}$ high and REFREQ and MREF low for one refresh period.
RFC	14	Refresh Complete input, when high, synchronously indicates to the timer the completion of the refresh cycle and sets $\overline{REFREQ}$ and $\overline{MREF}$ high and REFREQ and MREF low. When using RFC, $\overline{RFC}$ should be inactive (high).
$\overline{RFC}$	15	Refresh Complete input, when low, synchronously indicates to the timer the completion of the refresh cycle and sets $\overline{REFREQ}$ and $\overline{MREF}$ high and REFREQ and MREF low. When using $\overline{RFC}$, RFC should be inactive (low).
$\overline{MREF}$	9	Mandatory Refresh output goes low when $\overline{REFREQ}$ signal is still low and REFREQ is still high 20 clock cycles before the next request. $\overline{MREF}$ returns high on the next active CLK edge if RFC is high or $\overline{RFC}$ is low.
MREF	11	Mandatory Refresh output goes high when $\overline{REFREQ}$ signal is still low and REFREQ is still high 20 clock cycles before the next request. MREF returns low on the next active CLK edge if RFC is high or $\overline{RFC}$ is low.
$\overline{REFREQ}$	10	Refresh Request output goes low when the selected divisor is reached. $\overline{REFREQ}$ returns high on next active clock edge if RFC is high and $\overline{RFC}$ is low.
REFREQ	12	Refresh Request output goes high when the selected divisor is reached. REFREQ returns low on next active clock edge if RFC is high and $\overline{RFC}$ is low.

† Pin numbers are for N package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

NOTE 1: All voltage values are with respect to the GND terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				– 3.2	mA
I_{OL}	Low-level output current				16	mA
f_{clock}	Clock frequency		0		40	MHz
t_w	Pulse duration	Clock high	6			ns
		Clock low	6			
t_{su}	Input setup time before CLK		15			ns
t_h	Input hold time after clock		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = – 0.4 mA	V_{CC} – 2			V
	V_{CC} = 4.75 V,	I_{OH} = – 3.2 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA		0.35	0.5	V
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.25	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0.5 V	– 30		– 130	mA
I_{CC}	V_{CC} = 5.25 V			156	185	mA

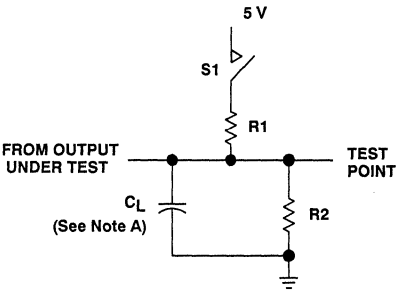
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 2)

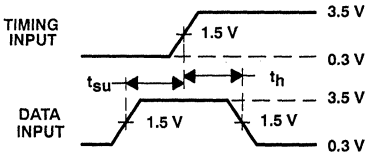
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 300 Ω, R2 = 390 Ω, T_A = 0°C to 70°C		UNIT
			MIN	MAX	
f_{max}			40		MHz
t_{pd}	CLK (RESET, RFC, $\overline{RFC}$)	REFREQ, $\overline{REFREQ}$, MREF, $\overline{MREF}$	3	10	ns
t_{pd}	CLK (CNT)	REFREQ, $\overline{REFREQ}$	3	10	ns
t_{pd}	CLK (CNT – 20)	MREF, $\overline{MREF}$	3	10	ns

NOTE 2: Load circuit and voltage waveforms are shown in Figure 3.

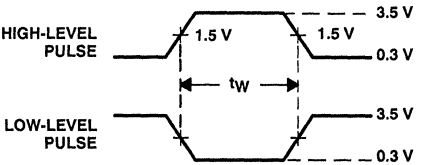
PARAMETER MEASUREMENT INFORMATION



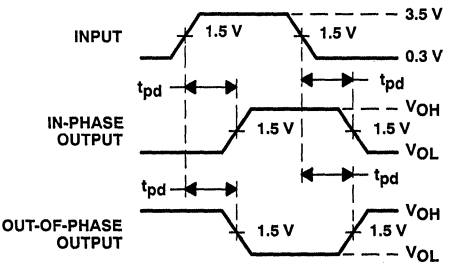
LOAD CIRCUIT FOR
3–STATE OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

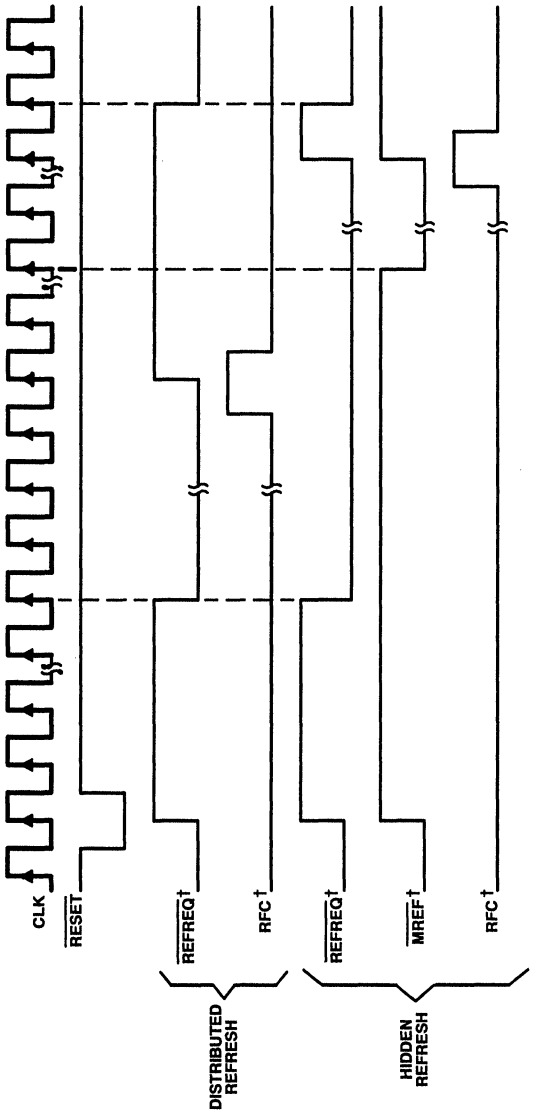


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

Figure 1

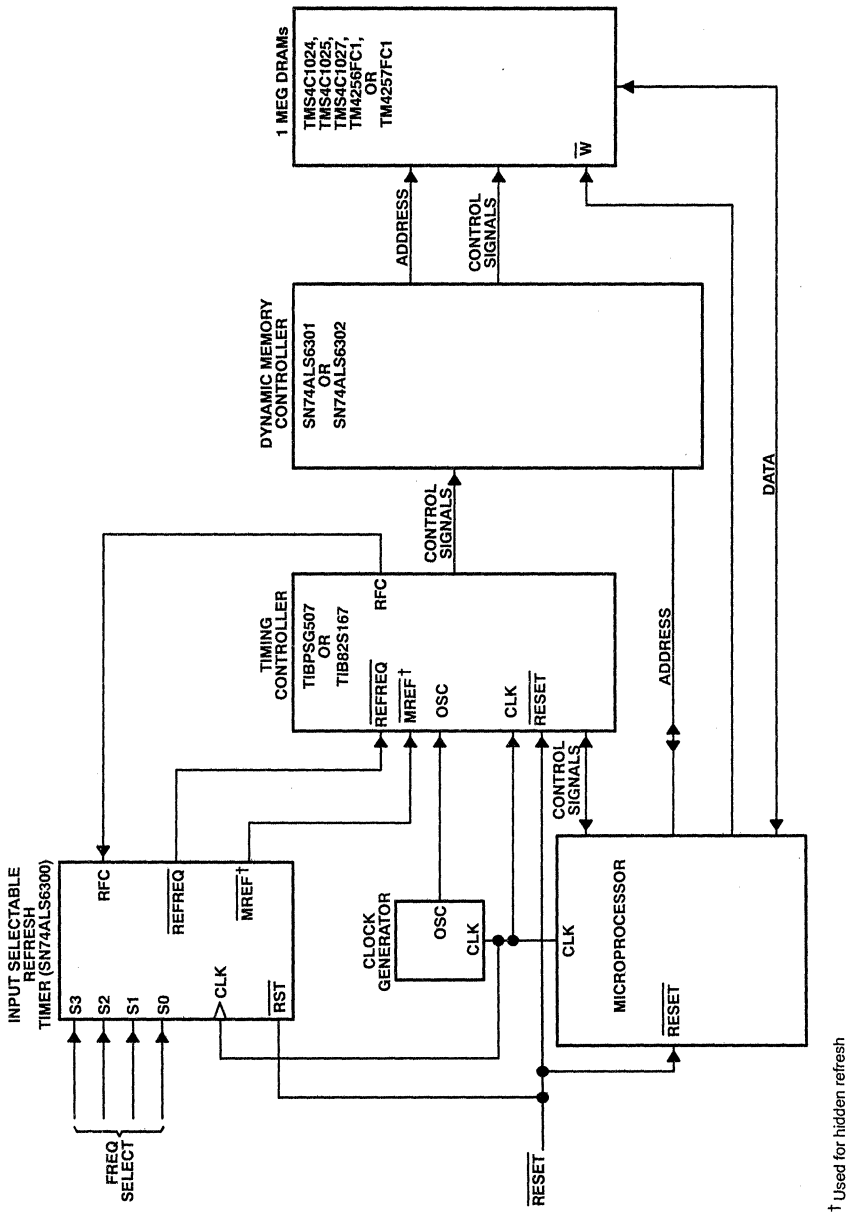
APPLICATION INFORMATION



†Polarity options (active-high or -low) available for these signals.

FIGURE 2. REFRESH CYCLE TIMING

APPLICATION INFORMATION



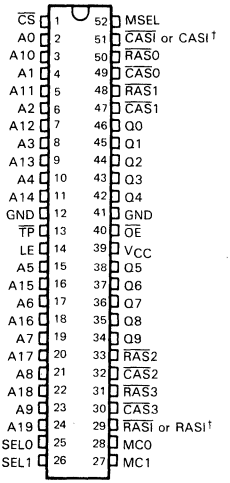
† Used for hidden refresh

FIGURE 3. TYPICAL SYSTEM INTERFACE FOR REFRESH TIMER

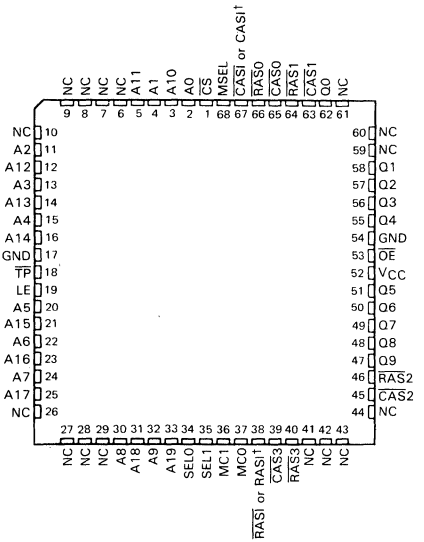
D2900, JANUARY 1986—REVISED MARCH 1988

- **Provides Control for 16K, 64K, 256K, and 1M Dynamic RAMs**
- **Highest-Order Two-Address Bits Select One of Four Banks of RAMs**
- **Supports Scrubbing Operations and Nibble-Mode Access**
- **Separate Output Enable for Multi-Channel Access to Memory**
- **52-Pin Dual-In-Line Package**

SN74ALS6301, SN74ALS6302 . . . JD OR N PACKAGE
(TOP VIEW)



SN74ALS6301, SN74ALS6302 . . . FN PACKAGE
(TOP VIEW)



† 'ALS6301 has active-low inputs $\overline{\text{CASI}}$ and $\overline{\text{RASI}}$; 'ALS6302 has active-high inputs CASI and RASI.

description

The 'ALS6301 and 'ALS6302 dynamic memory controllers (DMCs) are designed for use in today's high-performance memory systems. The DMC acts as the address controller between any processor and dynamic memory array.

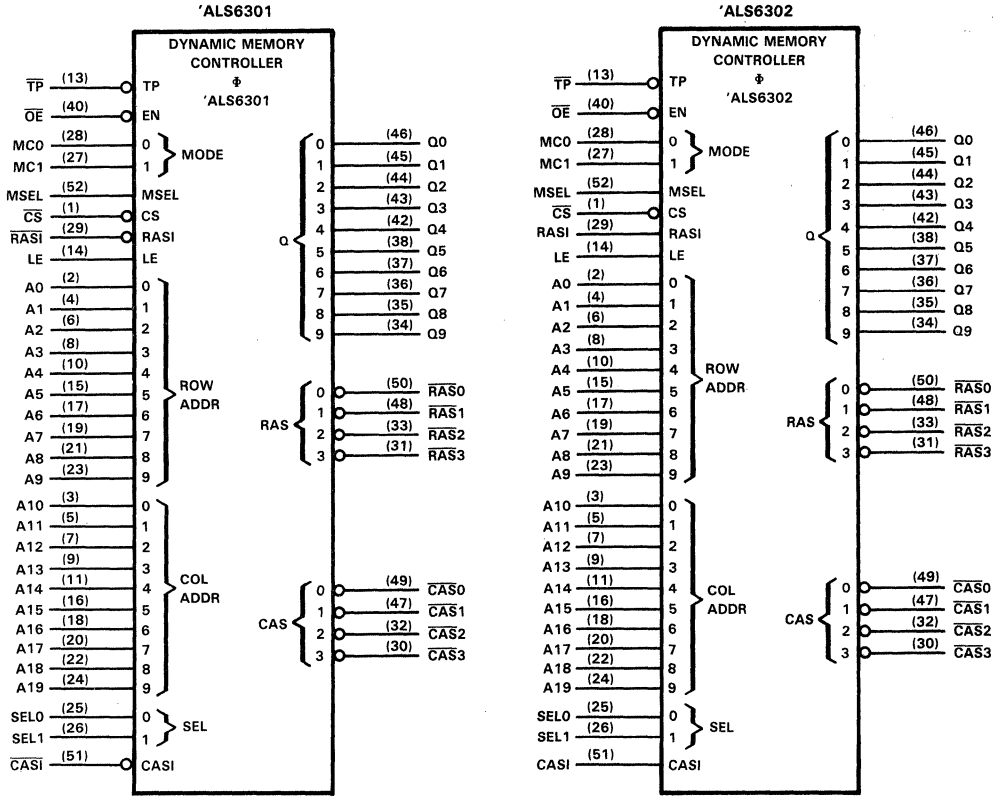
Two versions are provided that help simplify interfacing to the system dynamic timing controller. The 'ALS6301 offers active-low Row Address Strobe Input ($\overline{\text{RASI}}$) and Column Address Strobe Input ($\overline{\text{CASI}}$), while the 'ALS6302 offers active-high Row Address Strobe Input (RASI) and Column Address Strobe Input (CASI) inputs.

Using two 10-bit address latches, the DMC will hold the row and column addresses for any DRAM up to 1M. These latches and the two row/column refresh address counters feed into a 10-bit, 4-input MUX for output to the dynamic RAM address lines. A 2-bit bank select latch is provided to select one of the four $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ outputs. The two bits are normally obtained from the two highest-order address bits.

The 'ALS6301 and 'ALS6302 have two basic modes of operation, read/write and refresh. During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM, with the corresponding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals activated to strobe the addresses into the RAM. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles. In this mode all $\overline{\text{RAS}}$ outputs will be active (low) while only one $\overline{\text{CAS}}$ output is active at a time.

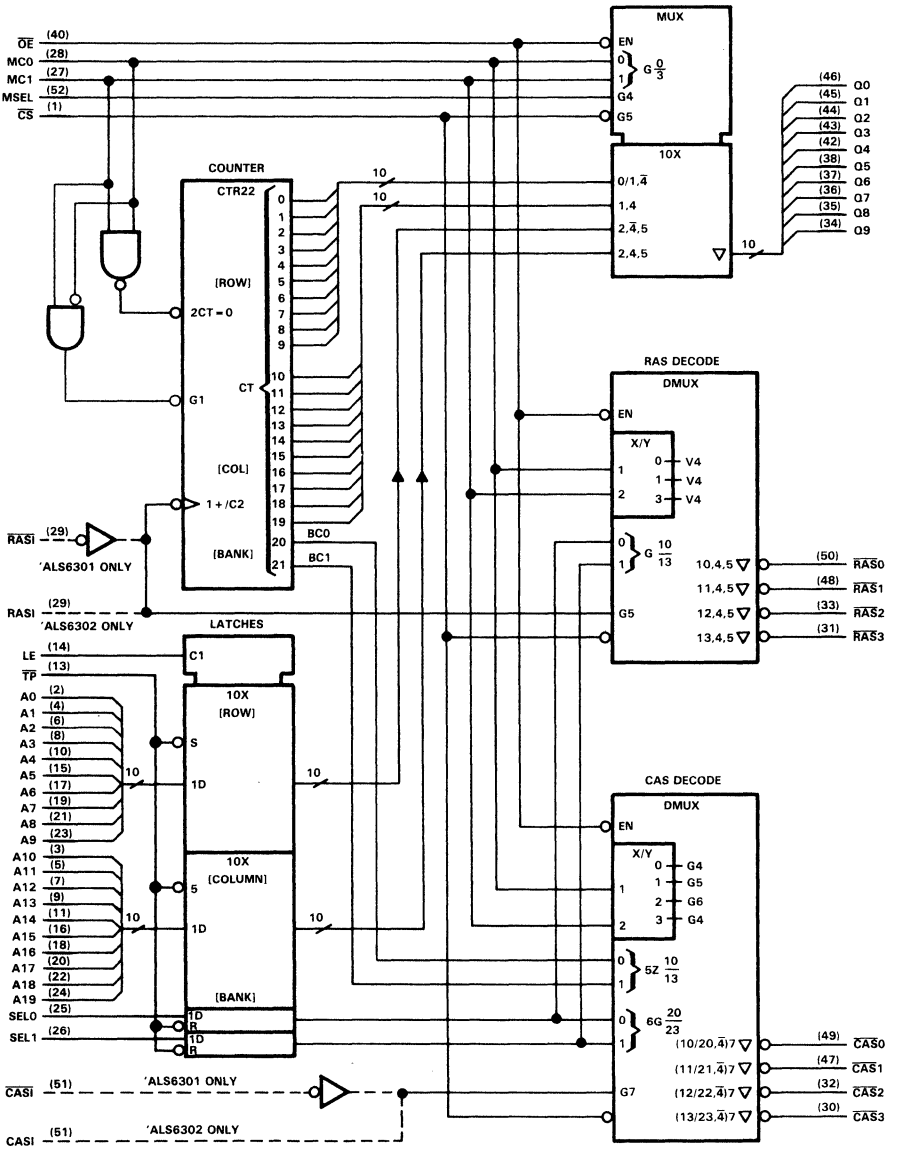
The SN74ALS6301 and SN74ALS6302 are characterized for operation from 0°C to 70°C.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std-91-1984 and IEC Publication 617-12.
Pin numbers shown are for JD and N packages.

logic diagram (positive logic)



Pin numbers shown are for JD and N packages.

TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A0-A19	Address Inputs. A0-A9 are latched in as the nine-bit row address for the DRAM. These inputs drive Q0-Q9 when the DMC is in the read/write mode and MSEL is low. A10-A19 are latched in as the column address, and will drive Q0-Q9 when MSEL is high and the DMC is in the read/write mode. The addresses are latched when the Latch Enable (LE) input signal is low.
$\overline{\text{CASI}}$ *or* CASI	Column Address Strobe Input. This input going active causes the selected $\overline{\text{CAS}}$ output to be forced low. The $\overline{\text{CASI}}$ input on the 'ALS6301 is active low input while on the 'ALS6302, CASI is active high input. (For more details see timing diagrams.)
$\overline{\text{CAS0}}$-$\overline{\text{CAS3}}$	Column Address Strobe. During normal Read/Write cycles the two selected bits (SEL0, SEL1) determine which $\overline{\text{CAS}}$ output will go active following $\overline{\text{CASI}}$ ('ALS6301) or CASI ('ALS6302) going active. When memory scrubbing is being performed, only the $\overline{\text{CAS}}$n signal selected will be active. For non-scrubbing cycles, all four $\overline{\text{CAS}}$ outputs will remain high.
$\overline{\text{CS}}$	Chip Select. This active-low input is used to enable the DMC. When $\overline{\text{CS}}$ is active, the DMC operates normally in all four modes. When $\overline{\text{CS}}$ goes high, the device will not enter the read/write mode. This allows other devices to access the same memory that the DMC is controlling.
LE	Latch Enable. This active-high input causes the row, column, and bank select latches to become transparent, allowing the latches to accept new input data. A low input on LE latches the input data.
MC0, MC1	Mode Controls. These inputs determine in which of the four modes the DMC operates. The description of each of the four operating modes is given in Table 2.
MSEL	Multiplexer Select. This input determines whether the row or column address will be sent to the memory address inputs. When MSEL is high, the column address is selected, while the row address is selected when MSEL is low. The address may come from either the address latch or refresh address counter depending on MC0 and MC1 (see Mode Control Function Table).
$\overline{\text{OE}}$	Output Enable. This active-low input enables/disables the output signals. When $\overline{\text{OE}}$ is high, the outputs of the DMC enter the high-impedance state.
Q0-Q9	Address Outputs. These address outputs feed the DRAM address inputs and provide drive for memory systems having capacitance of up to 500 picofarads.
$\overline{\text{RASI}}$ or RASI	Row Address Strobe Input. During the normal memory cycles, the decoded $\overline{\text{RAS}}$n output ($\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, *or* $\overline{\text{RAS3}}$) is forced low after receipt of an active Row Address Strobe Input signal. In either Refresh mode, all four $\overline{\text{RAS}}$ outputs will be low while the Row Address Strobe Input signal is active. The $\overline{\text{RASI}}$ on the 'ALS6301 is an active-low input while on the 'ALS6302, RASI is an active-high input. (For more details see timing diagrams).
$\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$	Row Address Strobe. Each of the Row Address Strobe outputs provides a $\overline{\text{RAS}}$ signal to one of the four banks of dynamic memory. Each $\overline{\text{RAS}}$n output will go low when selected by SEL0 and SEL1 after $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) goes active. All four go low in response to $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) while in the refresh mode.
SEL0, SEL1	Bank Select. These two inputs are normally the two highest-order address bits and are used in the read/write mode to select which bank of memory will be receiving the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals after $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) and $\overline{\text{CASI}}$ ('ALS6301) or CASI ('ALS6302) go active.
$\overline{\text{TP}}$	This active-low test input asynchronously sets the row and column input latches high, while forcing the two bank select latches low. In normal operation, $\overline{\text{TP}}$ is tied high.

FUNCTION TABLES

MODE-CONTROL

MC1	MC0	OPERATING MODE
L	L	Refresh Mode without Scrubbing. Refresh cycles are performed with only the row counter being used to generate the addresses. In this mode, all four $\overline{RAS}$ outputs are active while the four $\overline{CAS}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. During this mode, refresh cycles are done with both the row and column counters generating the addresses. MSEL is used to select either the row or the column counter. All four $\overline{RAS}$ outputs go low in response to $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), while only one $\overline{CAS}$n output goes low in response to $\overline{CASI}$ ('ALS6301) or CASI ('ALS6302). The bank counter keeps track of which $\overline{CAS}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the Row and Column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{RAS}$n and $\overline{CAS}$n outputs will be active. The refresh counter is disabled while in this mode.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302), putting them at start of the refresh sequence (see timing diagrams for more detail). In this mode, all four $\overline{RAS}$ outputs are driven low after the active edge of $\overline{RASI}$ ('ALS6301) or RASI ('ALS6302) so that DRAM wake-up cycles may also be performed.

FUNCTION TABLES (continued)

ADDRESS OUTPUT FUNCTIONS

MODE	INPUTS				OUTPUTS Q0-Q9
	MC1	MC0	MSEL	$\overline{CS}$	
Refresh without scrubbing	L	L	X	X	Row counter address
Refresh with scrubbing	L	H	L	X	Row counter address
			H	X	Column counter address
Read/write	H	L	L	L	Row address†
			H	L	Column address†
			X	H	All L
Clear refresh counter‡	H	H	X	X	All L

RAS OUTPUT FUNCTIONS

INPUTS							OUTPUTS			
'ALS6301 $\overline{RASI}$	'ALS6302 RASI	MC1	MC0	SEL1†	SEL0†	$\overline{CS}$	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$
L	H	L	L	X	X	X	L	L	L	L
L	H	L	H	X	X	X	L	L	L	L
L	H	H	L	L	L	L	L	H	H	H
				L	H	L	H	L	H	H
				H	L	L	H	H	L	H
				H	H	L	H	H	H	L
				X	X	H	H	H	H	H
L	H	H	H	X	X	X	L	L	L	L
H	L	X	X	X	X	X	H	H	H	H

CAS OUTPUT FUNCTIONS

INPUTS									OUTPUTS			
'ALS6301 $\overline{CASI}$	'ALS6302 CASI	MC1	MC0	SEL1†	SEL0†	INTERNAL BC1	INTERNAL BC0	$\overline{CS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$
L	H	L	L	X	X	X	X	X	H	H	H	H
L	H	L	H	X	X	L	L	X	L	H	H	H
						L	H	X	H	L	H	H
						H	L	X	H	H	L	H
						H	H	X	H	H	H	L
L	H	H	L	L	L	X	X	L	L	H	H	H
				L	H	X	X	L	H	L	H	H
				H	L	X	X	L	H	H	L	H
				H	H	X	X	L	H	H	H	L
				X	X	X	X	H	H	H	H	H
L	H	H	H	X	X	X	X	X	H	H	H	H
H	L	X	X	X	X	X	X	X	H	H	H	H

† If $\overline{TP}$ is low, the row and column address latch will be high. If $\overline{TP}$ is high, the row and column address latch will be at the levels entered when LE was last high.

‡ For 'ALS6301, clearing occurs on the low-to-high transition of $\overline{RASI}$; for 'ALS6302, clearing occurs on the high-to-low transition of RASI.

read/write operation details

During normal read/write operations, the row and column addresses are multiplexed to the dynamic RAM controlled by the MSEL input. The corresponding $\overline{RAS}$n and $\overline{CAS}$n output signals strobe the addresses into memory. The block diagram in Figure 1 shows a typical system interface for a four-megaword dynamic memory. The DMC is used to control the four banks of 1M memory.

For systems where addresses and data are multiplexed onto a single bus, the DMC uses latches, (row, column, and bank) to hold the address information. Figure 5 shows a typical timing diagram using the input latches. The twenty-two input latches are transparent when latch enable (LE) is high, and latch the input data whenever LE is taken low. For systems in which the processor has separate address and data buses, LE may be permanently high (see timing diagram in Figure 4).

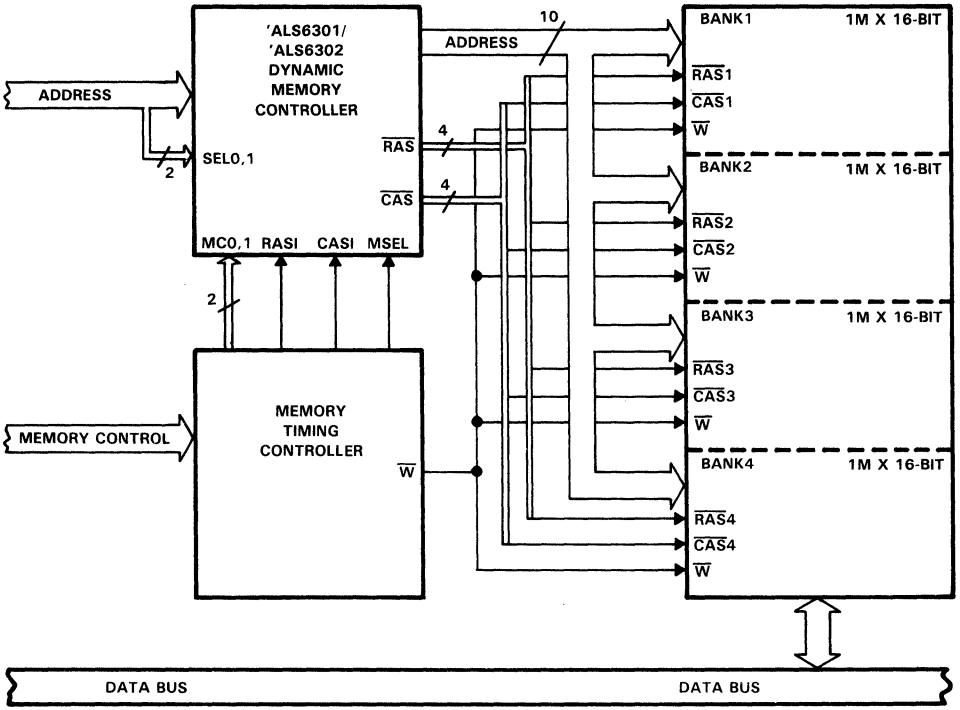


FIGURE 1. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY

read/write operations (continued)

The DMC is designed with heavy-duty outputs that are capable of driving four banks of 16-bit words, including six checkbits used for error detection and correction.

In addition to heavy-duty output drivers, the outputs are designed with balanced output impedances (25 Ω both high and low). This feature optimizes the drive low characteristics, based on safe undershoot, while providing symmetrical drive high characteristics. It also eliminates the external resistors required to pull the outputs up to the MOS V_{OH} level (V_{CC} – 1.5 V).

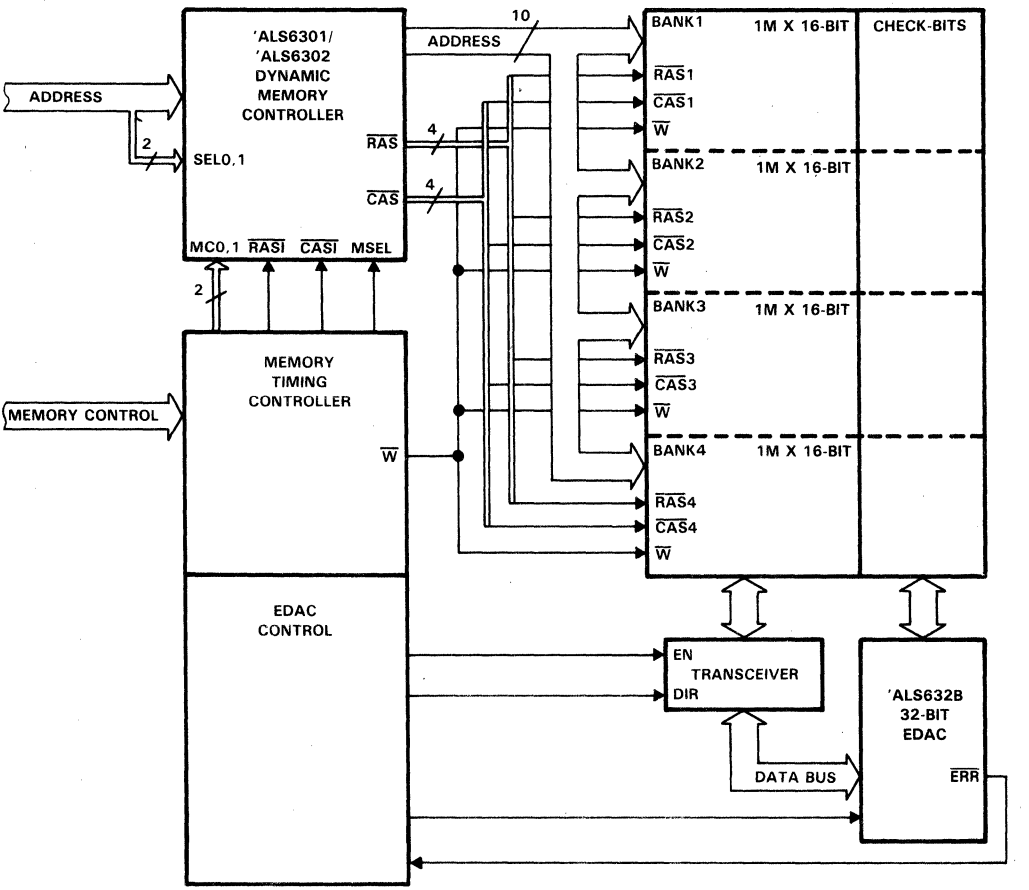


FIGURE 2. 4-MEGAWORD X 16-BIT DYNAMIC MEMORY WITH ERROR DETECTION AND CORRECTION

memory expansion

With a 10-bit address path, the DMC can control up to four megaword when using 1M dynamic RAMs. If a larger memory size is desired, the DMC's chip select ($\overline{CS}$) makes it easy to expand the memory size by using additional DMCs. A sixteen-megaword memory system is shown in Figure 3.

To maintain maximum performance in 32-bit applications, it is recommended that individual bus drivers be used for each bank.

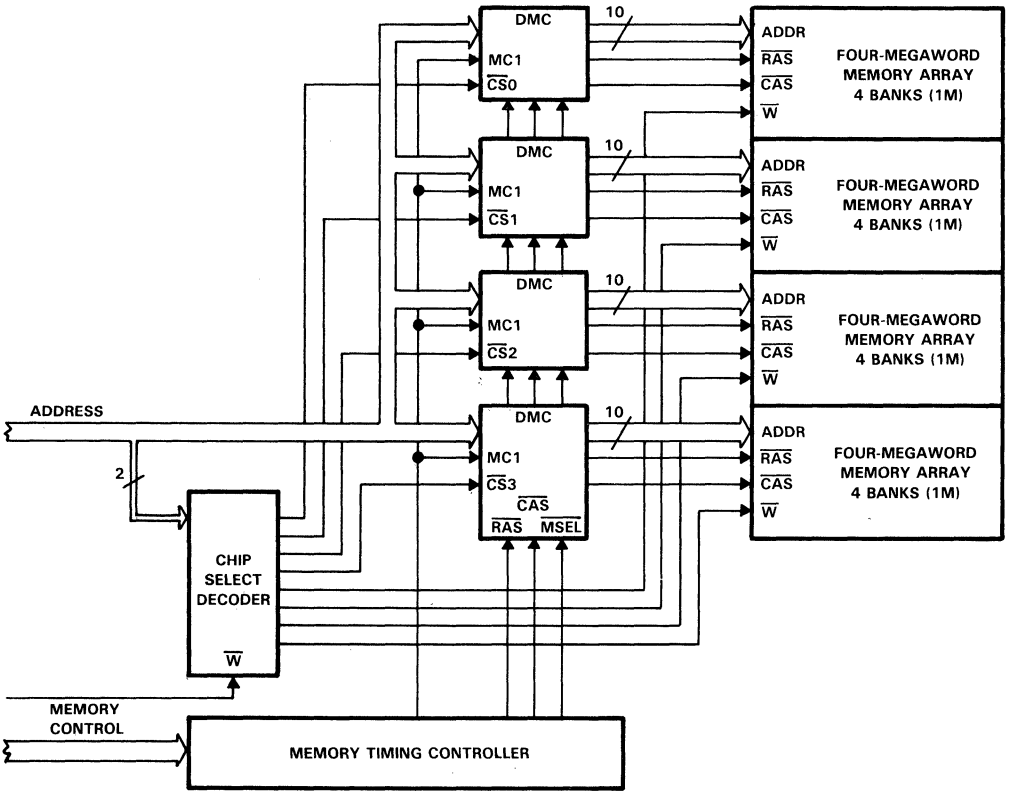


FIGURE 3. 16-MEGAWORD X 16-BIT DYNAMIC MEMORY

refresh operations

The two 10-bit counters in the 'ALS6301 and 'ALS6302 support 128-, 256-, 512-, and 1024-line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302. The refresh counters are reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302, if MC1 and MC0 are at a high logic level. See Figure 8 for additional timing details.

When performing refresh cycles without memory scrubbing (MC1 and MC0 both low), all four $\overline{\text{RAS}}$ outputs go low, while all $\overline{\text{CAS}}$ outputs are driven high. Typical timing for this mode of operation is shown in Figure 6.

decoupling

Due to the high switching speed and high drive capability of the 'ALS6301 and 'ALS6302, it is necessary to decouple the device for proper operation. Multilayer ceramic 0.1-μF to 1-μF capacitors are recommended for decoupling. It is important to mount the capacitors as close as possible to the power pins (V_{CC} and GND) to minimize lead inductance and noise. A ground plane is recommended.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND pins.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	(23) $\overline{RASI}$ low or RASI high	10			ns
		(24) $\overline{RASI}$ high or RASI low	10			
		(25) LE high	10			
t_{su}	Setup time	(26) An before LE↓	5			ns
		(27) SELn before LE↓	5			
		(28) MC0,1 high before $\overline{RASI}$↑ or RASI↓	10			
		(29) SELn before $\overline{RASI}$↓ or RASI↑	5			
t_h	Hold time	(30) An after LE↓	5			ns
		(31) SELn after LE↓	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	30			mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_O§	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			136	220	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit output current, I_{OS}.

'ALS6301 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RASn}$		2	10	14	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CASn}$		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6301 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	$\overline{RASI}$	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	$\overline{RASI}$	$\overline{RASn}$		3	9	18	ns
$t_{pd(3)}$	$\overline{CASI}$	$\overline{CASn}$		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

'ALS6302 switching characteristics, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	5	16	30	ns
$t_{pd(2)}$	RASI	$\overline{RAS}$n		2	10	14	ns
$t_{pd(3)}$	CASI	$\overline{CAS}$n		2	7	14	ns
$t_{pd(4)}$	Any A	Any Q		3	9	17	ns
$t_{pd(5)}$	MSEL	Any Q		5	13	22	ns
$t_{pd(6)}$	LE↑	Any Q			13	22	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	22	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	22	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		6	14	24	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		2	10	15	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		2	10	15	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			13	24	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			7	13	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	13	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			9	15	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			9	15	ns
$t_{en(17)}$	$\overline{OE}$↓	Any Q			10	18	ns
$t_{en(18)}$	$\overline{OE}$↓	Any $\overline{RAS}$			10	18	ns
$t_{en(19)}$	$\overline{OE}$↓	Any $\overline{CAS}$			10	18	ns
$t_{dis(20)}$	$\overline{OE}$↑	Any Q			12	20	ns
$t_{dis(21)}$	$\overline{OE}$↑	Any $\overline{RAS}$			12	20	ns
$t_{dis(22)}$	$\overline{OE}$↑	Any $\overline{CAS}$			12	20	ns

'ALS6302 switching characteristics, C_L = 150 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$t_{pd(1)}$	RASI	Any Q	V_{CC} = 4.5 V to 5.5 V, T_A = 0°C to 70°C	10	20	35	ns
$t_{pd(2)}$	RASI	$\overline{RAS}$n		3	9	18	ns
$t_{pd(3)}$	CASI	$\overline{CAS}$n		2	7	18	ns
$t_{pd(4)}$	Any A	Any Q		5	11	18	ns
$t_{pd(5)}$	MSEL	Any Q		5	15	24	ns
$t_{pd(6)}$	LE↑	Any Q			13	24	ns
$t_{pd(7)}$	LE↑	Any $\overline{RAS}$			13	24	ns
$t_{pd(8)}$	LE↑	Any $\overline{CAS}$			13	24	ns
$t_{pd(9)}$	MC0 or MC1	Any Q		8	15	25	ns
$t_{pd(10)}$	MC0 or MC1	Any $\overline{RAS}$		5	10	16	ns
$t_{pd(11)}$	MC0 or MC1	Any $\overline{CAS}$		5	10	16	ns
$t_{pd(12)}$	$\overline{CS}$	Any Q			16	25	ns
$t_{pd(13)}$	$\overline{CS}$	Any $\overline{RAS}$			9	15	ns
$t_{pd(14)}$	$\overline{CS}$	Any $\overline{CAS}$			9	15	ns
$t_{pd(15)}$	SEL0 or SEL1	Any $\overline{RAS}$			10	17	ns
$t_{pd(16)}$	SEL0 or SEL1	Any $\overline{CAS}$			10	17	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

* t_{pd} specified at C_L = 50, 150 pF

CAPACITIVE LOAD SWITCHING

THREE-STATE ENABLE/DISABLE

FIGURE 4. SWITCHING TEST CIRCUIT

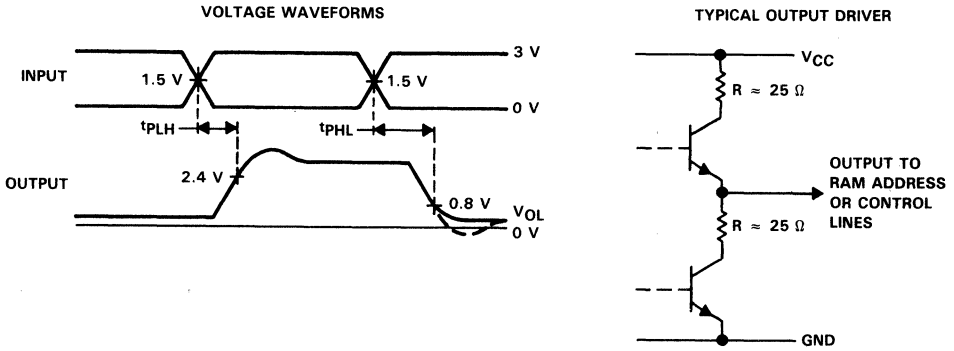
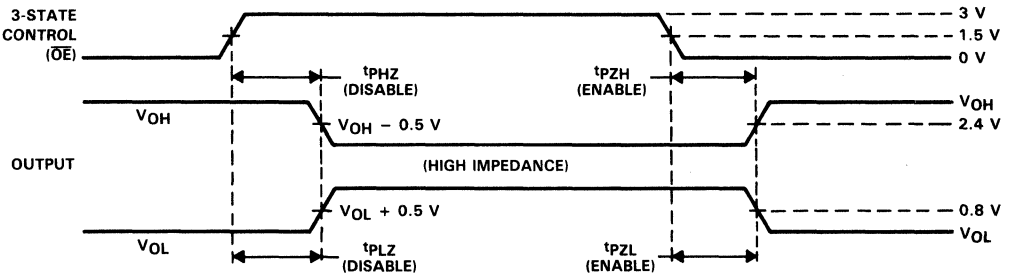


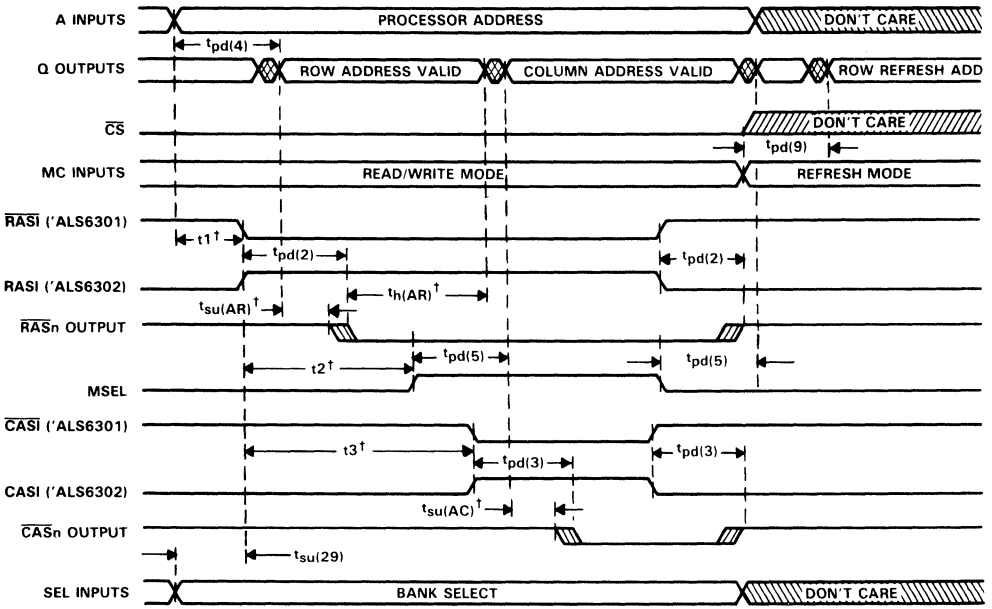
FIGURE 5. OUTPUT DRIVE LEVELS FOR TYPICAL SWITCHING CHARACTERISTICS



NOTE: Decoupling is needed for all AC tests

FIGURE 6. THREE-STATE CONTROL LEVELS

PARAMETER MEASUREMENT INFORMATION



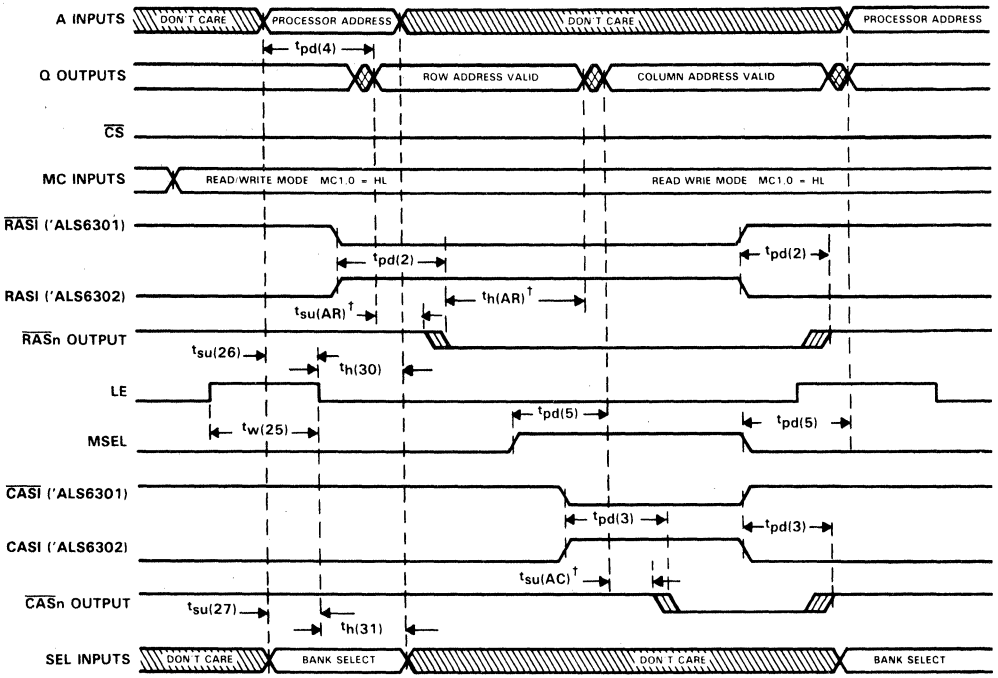
† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t1, t2, and t3 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirements for t1, t2, and t3 are as follows:

$t1(min) = t_{pd(4)}\ max + t_{su(AR)}\ min - t_{pd(2)}\ min$
$t2(min) = t_{pd(2)}\ max + t_{h(AR)}\ min - t_{pd(5)}\ min$
$t3(min) = t2\ min + t_{pd(5)}\ max + t_{su(AC)} - t_{pd(3)}\ min$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AR)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must relate to actual system capacitive loading.

FIGURE 7. READ/WRITE CYCLE TIMING (MC1, MC0 = 1, 0), (LE = H)

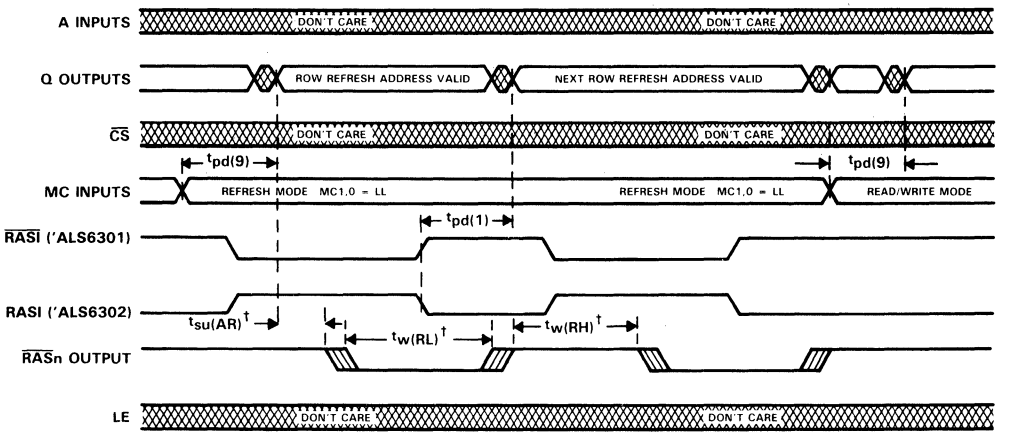
PARAMETER MEASUREMENT INFORMATION



†$t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. See the DRAM data sheet for applicable specifications.

FIGURE 8. READ/WRITE CYCLE TIMING USING INPUT LATCHES (MC1, MC0 = H, L)

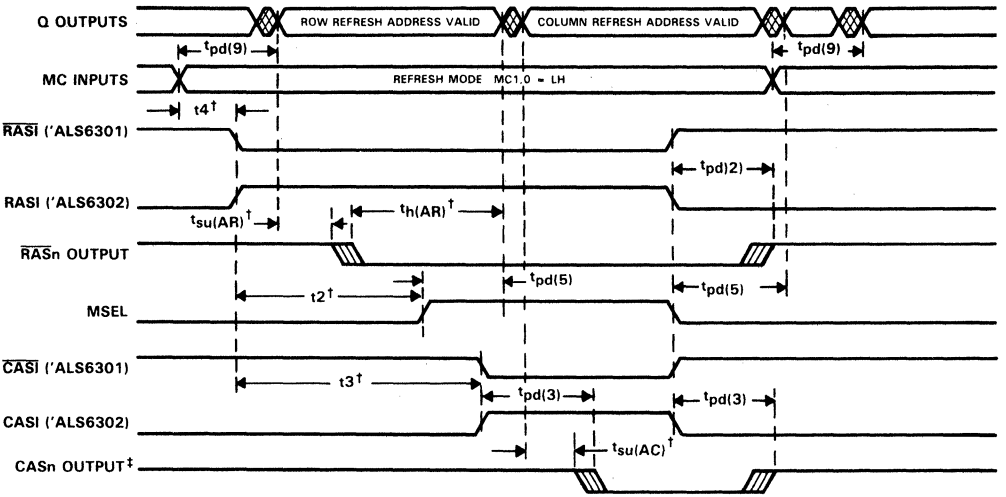
PARAMETER MEASUREMENT INFORMATION



†$t_{su(AR)}$, $t_{w(RL)}$, and $t_{w(RH)}$ are timing requirements of the dynamic RAM. See DRAM data sheet for applicable specifications.

FIGURE 9. REFRESH CYCLE TIMING (MC1, MC0 = L, L) WITHOUT SCRUBBING

PARAMETER MEASUREMENT INFORMATION



† Parameters $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$ are timing requirements of the dynamic RAM. Parameters t2, t3, and t4 represent the minimum timing requirements at the inputs to the DMC that guarantee DRAM timing specifications and maximum system performance. The minimum requirement for t2, t3, and t4 are as follows:

$$t2(\text{min}) = t_{pd(2)}\ \text{max} + t_{h(AR)}\ \text{min} - t_{pd(5)}\ \text{min}$$
$$t3(\text{min}) = t2\ \text{min} + t_{pd(5)}\ \text{max} + t_{su(AC)} - t_{pd(3)}\ \text{min}$$
$$t4(\text{min}) = t_{pd(9)}\ \text{max} + t_{su(AR)}\ \text{min} - t_{pd(2)}\ \text{min}$$

See the DRAM data sheet for applicable $t_{su(AR)}$, $t_{su(AC)}$, and $t_{h(AR)}$. In addition, note that propagation delay times given in the above equations are functions of capacitive loading. The values used in these equations must correspond to actual system capacitive loading.

‡ A $\overline{\text{CAS}}$n output is selected by the bank counter. All other $\overline{\text{CAS}}$n outputs will remain high.

FIGURE 10. REFRESH CYCLE TIMING (MC1, MC0 = L, H) WITH MEMORY SCRUBBING

PARAMETER MEASUREMENT INFORMATION

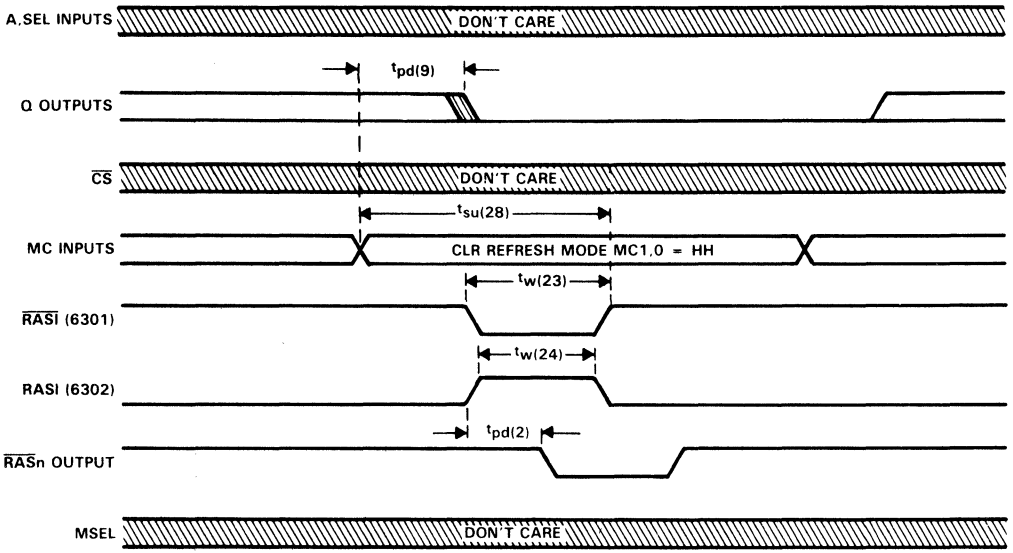


FIGURE 11. REFRESH COUNTER RESET (MC1, MC0 = H, H)

PARAMETER MEASUREMENT INFORMATION

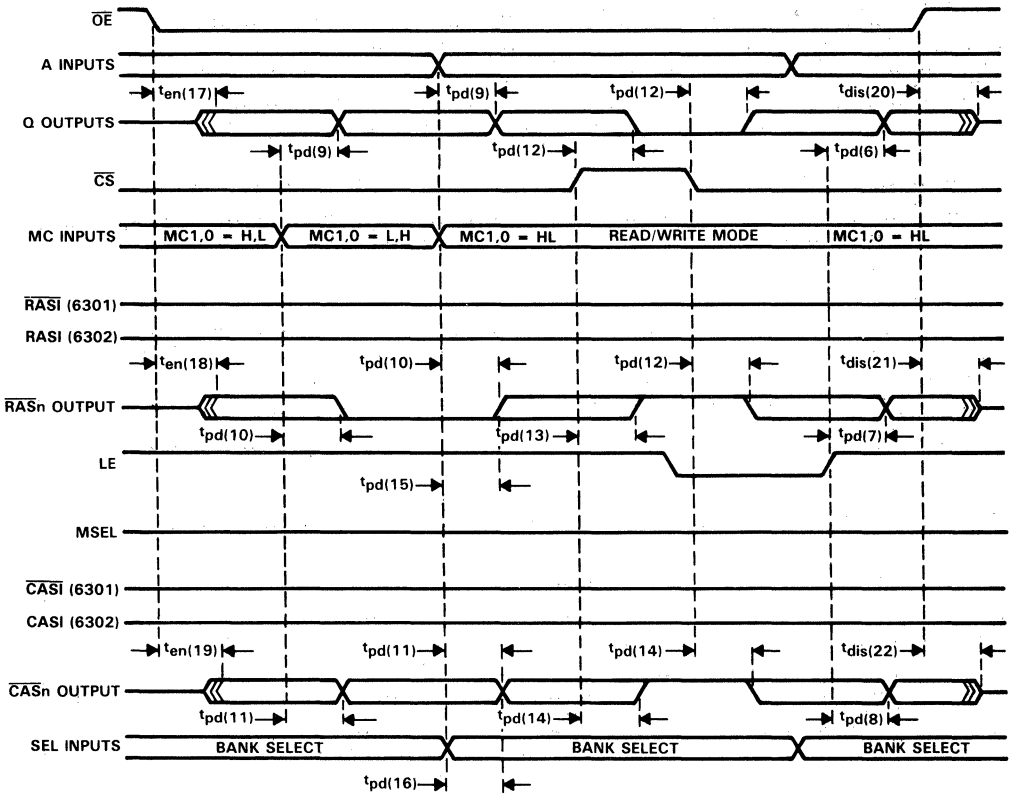


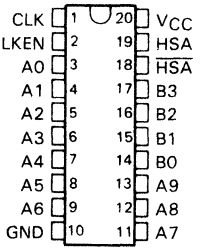
FIGURE 12. MISCELLANEOUS TIMING

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3020, JUNE 1987—REVISED DECEMBER 1989

- **Detects Present Row Equal to Last Row Address**
- **High-Performance Compare:**
  'ALS6310A CLK to HSA = 18 ns
  'ALS6311A Address to HSA = 14 ns
- **Compatible with 16K to 1M DRAMs**
- **Easily Interfaced with Microprocessor and Memory Timing Controller**
- **Dependable Texas Instruments Quality and Reliability**

DW OR N PACKAGE
(TOP VIEW)



description

The 'ALS6310A and 'ALS6311A are high-performance address comparators designed for implementing static column and page-mode access cycles.

When interfaced with the memory timing controller, these devices will detect if the present row being accessed is the same as the last row accessed. This is the fundamental requirement for implementing static column decode or page-mode access cycles.

The 'ALS6310A features two 14-bit registers and a high-speed address comparator. The first register is used to save the present row address while the second register is used to save the previous row address. On the high-to-low transition of CLK, the first register loads the new row address present on A0-A9. At the same time, the second register loads the address previously saved in the first register. The two row addresses are then compared. The High-Speed Access outputs (HSA and $\overline{\text{HSA}}$) will signal if the two addresses are equal.

The B0-B1 inputs are provided to monitor access cycles to different banks of memory. When used in conjunction with the 'ALS2968 and 'ALS6302 series DRAM controllers, the 'ALS6310A and 'ALS6311A can monitor up to 16 banks of memory. The CLK input on the 'ALS6310A can typically be interfaced with the microprocessor's Address Latch Enable (ALE) or Address Strobe (AS) outputs. This configuration simplifies the memory timing controller interface. Refer to the typical application diagram for further information.

The 'ALS6311A features one 14-bit register feeding a high-speed address comparator. This architecture offers a faster address match time, but does require the memory timing controller to generate the CLK input. Typically, the 14-bit register would only be updated if there was a change in row or bank address. Refer to the application diagram for further information.

More information on static column DRAM access can be found in the Texas Instruments application report *System Solutions for Static Column Decode*.

The SN74ALS6310A and SN74ALS6311A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE ('ALS6310A)

INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↓	P=Q	P=Q	H	L
H	↓	P=Q	P≠Q	L	H
H	↓	P≠Q	P=Q	L	H
H	↓	P≠Q	P≠Q	L	H
X	H	X	X	HSA_0	$\overline{HSA}0$
L	X	X	X	HSA_0	$\overline{HSA}_0$

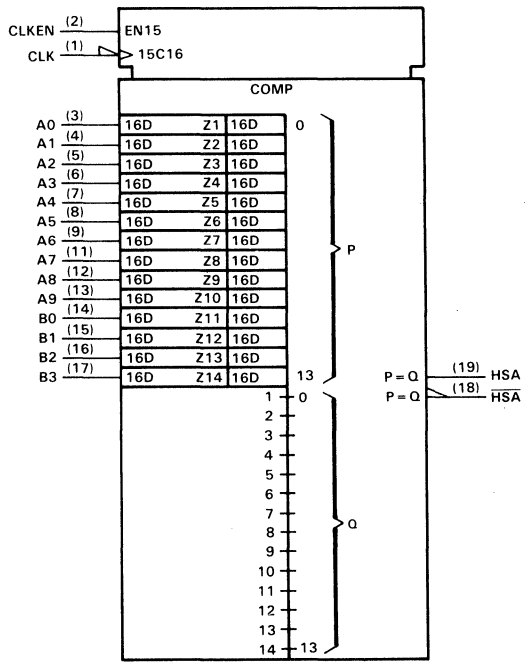
FUNCTION TABLE ('ALS6311A)

INPUTS				OUTPUTS	
CLKEN	CLK	A0-A9	B0-B3	HSA	$\overline{HSA}$
H	↑	X	X	H	L
X	X	P=Q	P=Q	H	L
X	No↑	X	P≠Q	L	H
X	No↑	P≠Q	X	L	H
L	X	X	P≠Q	L	H
L	X	P≠Q	X	L	H

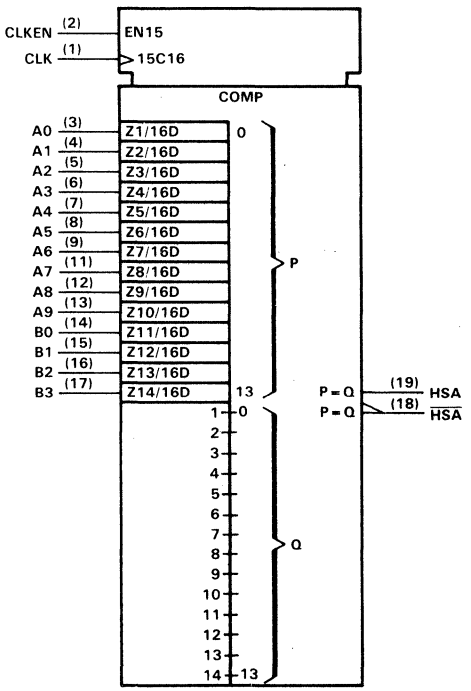
P = previous address
Q = present address

logic symbols†

ALS6310A



'ALS6311A



†These symbols are in accordance with ANSI/IEEE Std 91 1984 and IEC Publication 617-12.

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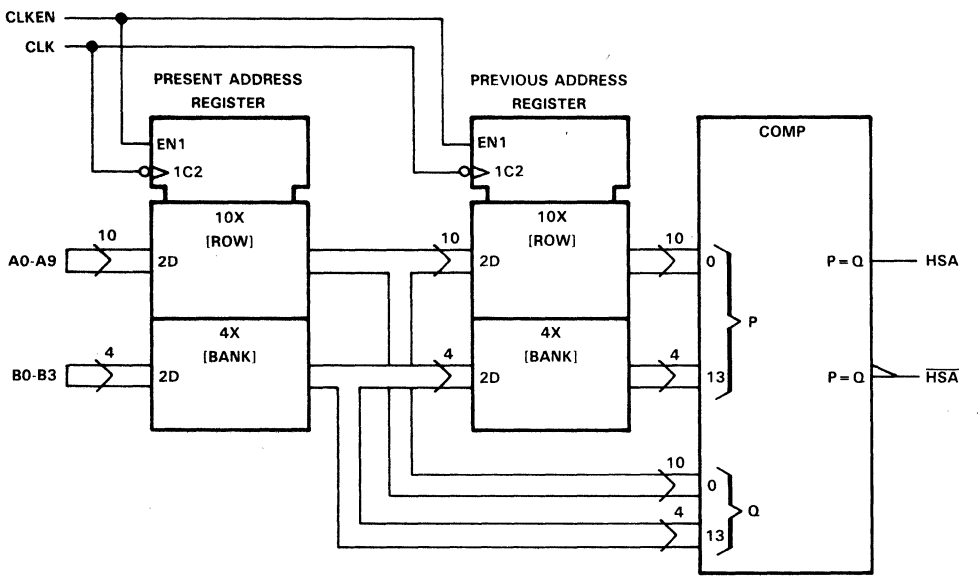
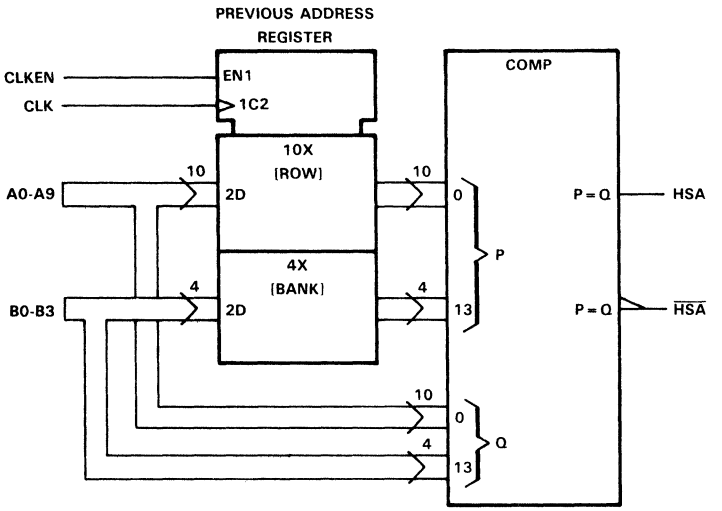
logic diagrams (positive logic)

'ALS6310A



'ALS6311A



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with repect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2.6	mA
I_{OL}	Low-level output current				24	mA
t_w	Pulse duration, CLK high or low		10			ns
t_{su}	Setup time before CLK↓ ('ALS6310A)	A0-A9 or B0-B3	8			ns
		CLKEN high or low	8			
t_{su}	Setup time before CLK↑ ('ALS6311A)	A0-A9 or B0-B3	8			ns
		CLKEN high or low	8			
t_h	Hold time after CLK↓ ('ALS6310A)	A0-A9 or B0-B3	5			ns
		CLKEN	5			
t_h	Hold time after CLK↑ ('ALS6311A)	A0-A9 or B0-B3	5			ns
		CLKEN	5			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA		V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA		2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	CLK, CLKEN			−0.3	mA
			All other inputs			−0.2	
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−30		−112	mA
I_{CC}	V_{CC} = 5.5 V				50	80	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK↓	HSA		12	15	4	18	ns
t_{PHL}				12	15	4	18	ns
t_{PLH}	CLK↓	$\overline{HSA}$		12	15	4	18	ns
t_{PHL}				12	15	4	18	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

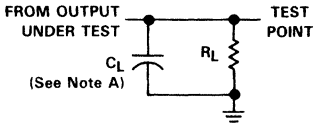
PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA		V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA		2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	CLK, CLKEN			−0.3	mA
			All other inputs			−0.2	
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V		−30		−112	mA
I_{CC}	V_{CC} = 5.5 V				40	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

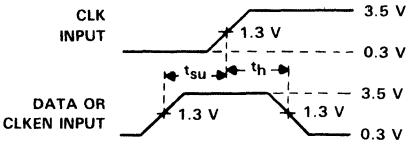
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK↑	HSA		8	10	4	12	ns
t_{PHL}	CLK↑	$\overline{HSA}$		8	10	4	12	ns
t_{PLH}	A0-A9 or B0-B3	HSA		7	10	3	12	ns
t_{PHL}				9	12	4	14	ns
t_{PLH}	A0-A9 or B0-B3	$\overline{HSA}$		9	12	4	14	ns
t_{PHL}				7	10	3	12	ns

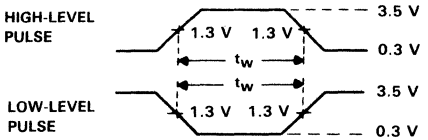
PARAMETER MEASUREMENT INFORMATION



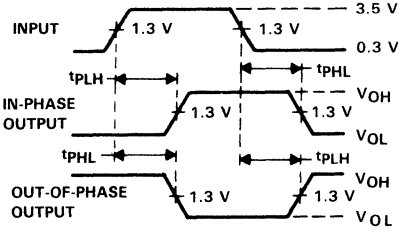
LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.

FIGURE 1

APPLICATION INFORMATION

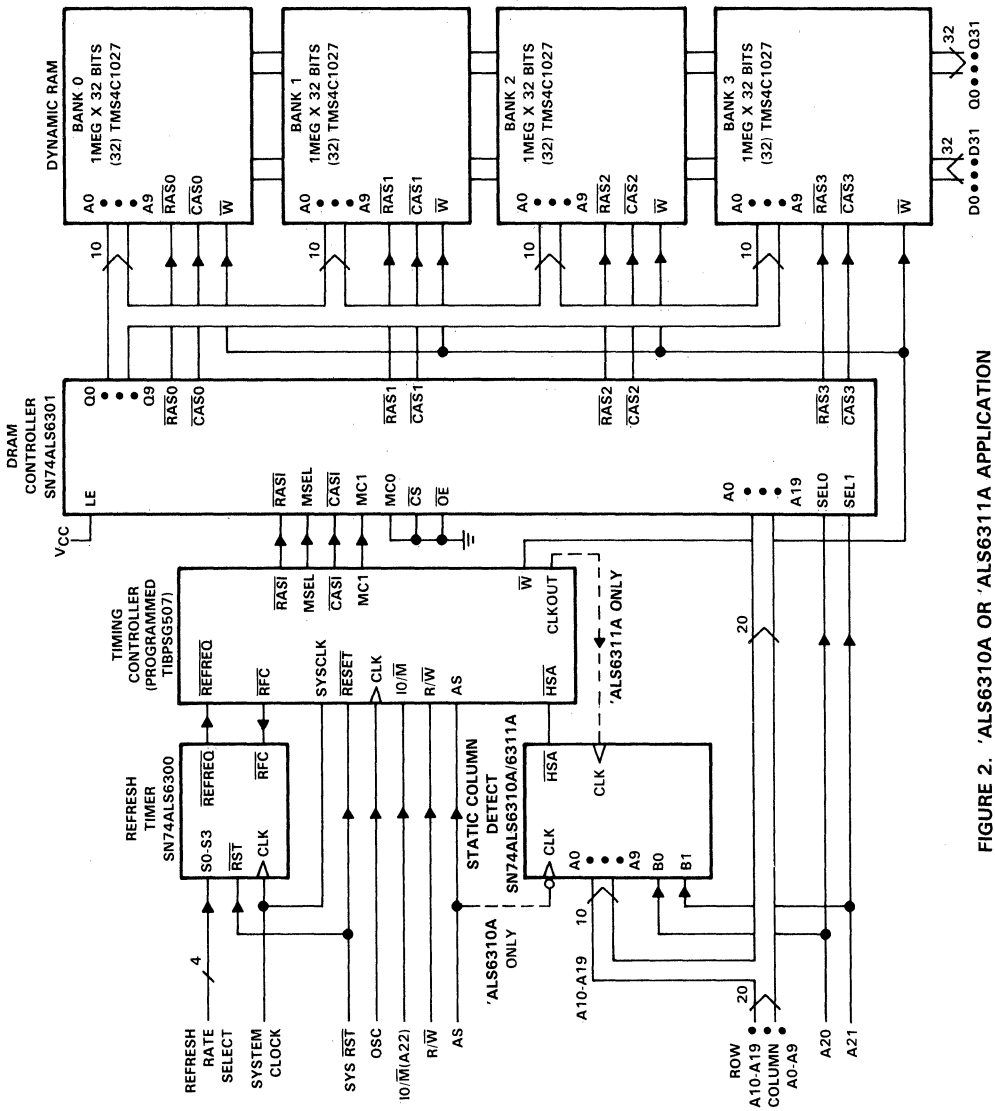


FIGURE 2. 'ALS6310A OR 'ALS6311A APPLICATION

APPLICATION INFORMATION

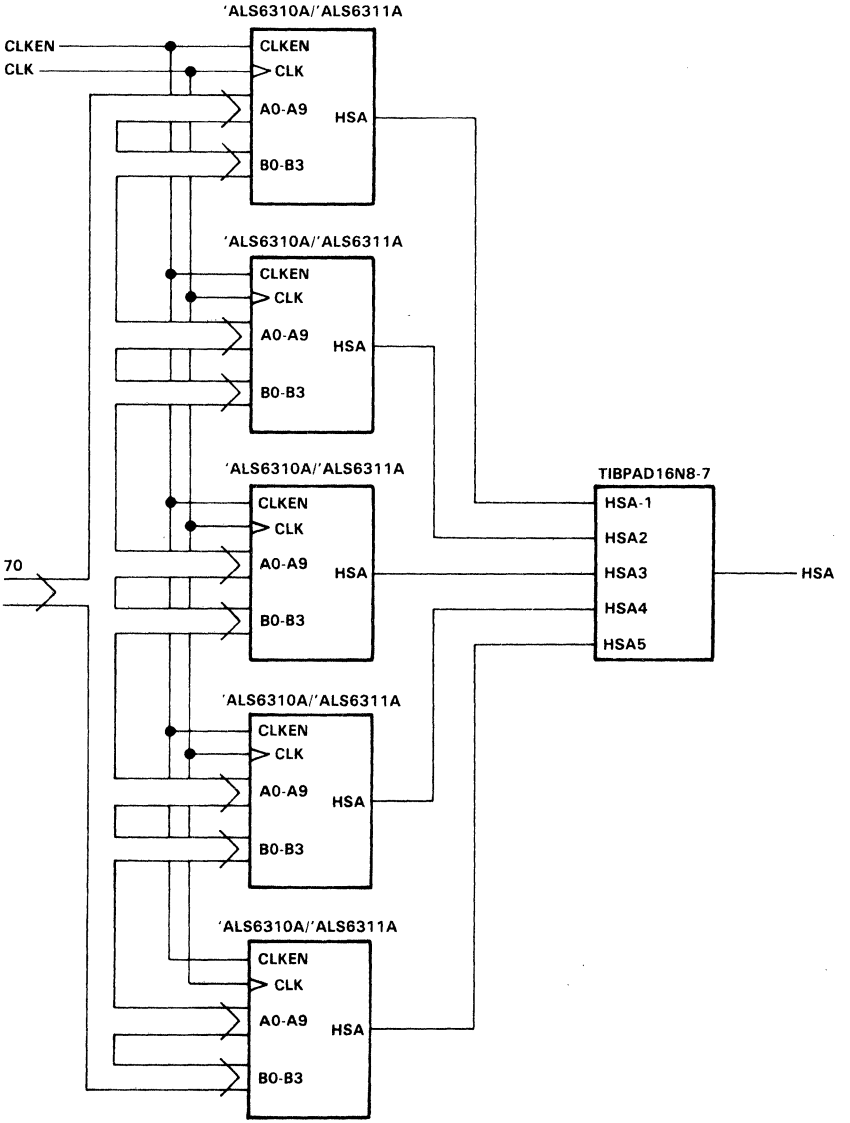


FIGURE 3. WORD LENGTH EXPANSION

Contents

D3396, JANUARY 1986—REVISED JANUARY 1990

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'ALS632B and 'AS632 devices are 32-bit parallel error detection and correction circuits (EDACs). The EDACs use a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

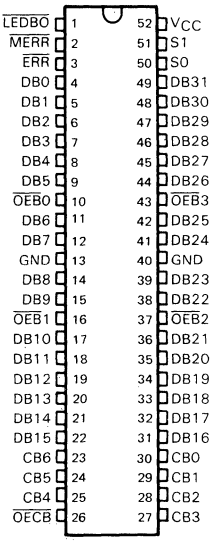
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

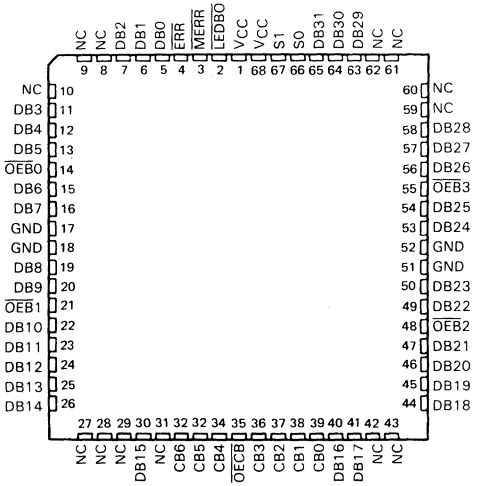
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB}}$0 thru $\overline{\text{OEB}}$3 byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

N OR JD PACKAGE
(TOP VIEW)

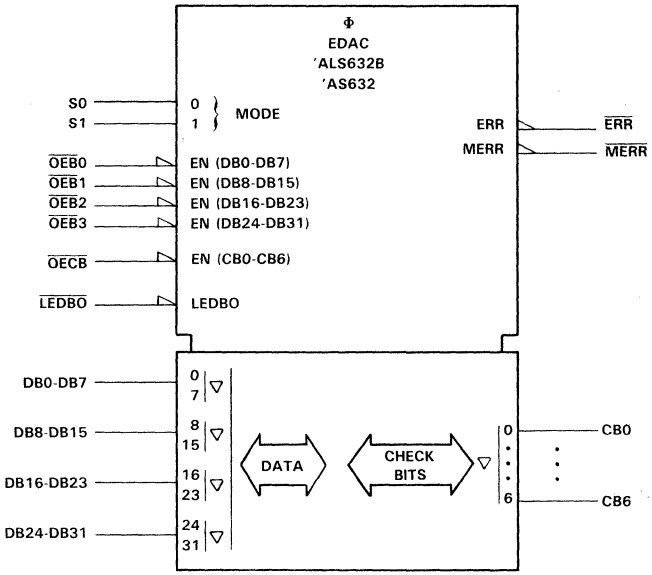


FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
CB0-CB6	Check Bit data port. This 7-bit I/O port is used to output check bits during write cycles and input memory check bits during read cycles.
DB0-DB31	Data port. This 32-bit I/O port is used to input processor data during memory write cycles and used to output corrected data during memory read cycles.
$\overline{ERR}$	Single-Bit Error Flag. This active-low output signals when a single-bit error has occurred. When more than two errors occur, this output is unpredictable.
GND	Ground
$\overline{LEDB0}$	Output Latch Enable. This input controls the output data latch that stores the corrected data word. When low, data is allowed to flow through the latch. When taken high, data present at the inputs of the output data latch is stored.
$\overline{MERR}$	Multiple-Bit Error Flag. This active-low output signals when a double-bit error has occurred. When more than two errors occur, this output is unpredictable.
NC	No internal connection
$\overline{OEB0}$-$\overline{OEB31}$	Data Output Enable controls. These active-low inputs are used to enable data onto the data bus (DB0-DB31). Each input controls 8-bits for byte control operations. $\overline{OEB0}$ controls DB0-DB7, $\overline{OEB1}$ controls DB8-DB15, $\overline{OEB2}$ controls DB16-DB23, and $\overline{OEB3}$ controls DB24-DB31.
$\overline{OECB}$	Check Bit Output Enable control. This active-low input is used to enable the check bits onto the check bit bus (CB0-CB6).
S0,S1	Mode Select controls. These control inputs select the mode of the EDAC. See function tables for details.
V_{CC}	Supply voltage

logic diagram (positive logic)

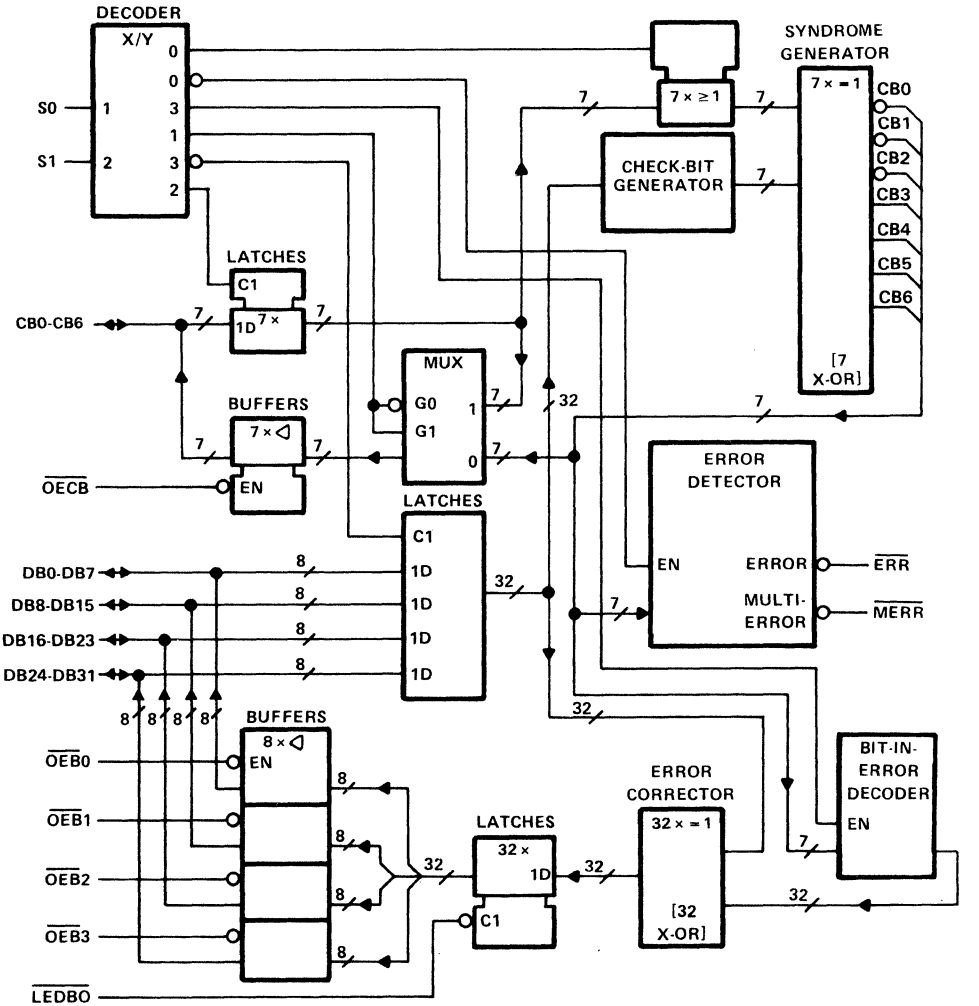


TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction. CB0, CB1 and CB2 are odd parity bits and CB3, CB4, CB5, and CB6 are even parity bits. For example, for a data word of all zeros CB0-CB2 will be high and CB3-CB6 will be low.

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

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TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set low while the dual error flag ($\overline{MERR}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	DATA I/O	DB CONTROL $\overline{OEB}$n OR $\overline{OEDB}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†	
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†	
Read	Output Corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†	

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

TABLE 5. SYNDROME DECODING

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
L	L	L	L	L	L	L	unc	
L	L	L	L	L	L	H	2-bit	
L	L	L	L	L	H	L	2-bit	
L	L	L	L	L	H	H	unc	
L	L	L	L	H	L	L	2-bit	
L	L	L	L	H	L	H	unc	
L	L	L	L	H	H	L	unc	
L	L	L	L	H	H	H	2-bit	
L	L	L	H	L	L	L	2-bit	
L	L	L	H	L	L	H	unc	
L	L	L	H	L	H	L	DB31	
L	L	L	H	L	H	H	2-bit	
L	L	L	H	H	L	L	unc	
L	L	L	H	H	L	H	2-bit	
L	L	L	H	H	H	L	2-bit	
L	L	L	H	H	H	H	DB30	
L	L	H	L	L	L	L	2-bit	
L	L	H	L	L	L	H	unc	
L	L	H	L	L	H	L	DB29	
L	L	H	L	L	H	H	2-bit	
L	L	H	L	H	L	L	DB28	
L	L	H	L	H	L	H	2-bit	
L	L	H	L	H	H	L	2-bit	
L	L	H	L	H	H	H	DB27	
L	L	H	H	L	L	L	DB26	
L	L	H	H	L	L	H	2-bit	
L	L	H	H	L	H	L	2-bit	
L	L	H	H	L	H	H	DB25	
L	L	H	H	H	L	L	2-bit	
L	L	H	H	H	L	H	DB24	
L	L	H	H	H	H	L	unc	
L	L	H	H	H	H	H	2-bit	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
L	H	L	L	L	L	L	2-bit	
L	H	L	L	L	L	H	unc	
L	H	L	L	L	H	L	DB7	
L	H	L	L	L	H	H	2-bit	
L	H	L	L	H	L	L	DB6	
L	H	L	L	H	L	H	2-bit	
L	H	L	L	H	H	L	2-bit	
L	H	L	L	H	H	H	DB5	
L	H	L	H	L	L	L	DB4	
L	H	L	H	L	L	H	2-bit	
L	H	L	H	L	H	L	2-bit	
L	H	L	H	L	H	H	DB3	
L	H	L	H	H	L	L	2-bit	
L	H	L	H	H	L	H	DB2	
L	H	L	H	H	H	L	unc	
L	H	L	H	H	H	H	2-bit	
L	H	H	L	L	L	L	DB0	
L	H	H	L	L	L	H	2-bit	
L	H	H	L	L	H	L	2-bit	
L	H	H	L	L	H	H	unc	
L	H	H	L	H	L	L	2-bit	
L	H	H	L	H	L	H	DB1	
L	H	H	L	H	H	L	unc	
L	H	H	L	H	H	H	2-bit	
L	H	H	H	L	L	L	2-bit	
L	H	H	H	L	L	H	unc	
L	H	H	H	L	H	L	unc	
L	H	H	H	L	H	H	2-bit	
L	H	H	H	H	L	L	unc	
L	H	H	H	H	L	H	2-bit	
L	H	H	H	H	H	L	2-bit	
L	H	H	H	H	H	H	CB6	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
H	L	L	L	L	L	L	2-bit	
H	L	L	L	L	L	H	unc	
H	L	L	L	L	H	L	unc	
H	L	L	L	L	H	H	2-bit	
H	L	L	L	H	L	L	unc	
H	L	L	L	H	L	H	2-bit	
H	L	L	L	H	H	L	2-bit	
H	L	L	L	H	H	H	unc	
H	L	L	H	L	L	L	unc	
H	L	L	H	L	L	H	2-bit	
H	L	L	H	L	H	L	2-bit	
H	L	L	H	L	H	H	DB15	
H	L	L	H	H	L	L	2-bit	
H	L	L	H	H	L	H	unc	
H	L	L	H	H	H	L	DB14	
H	L	L	H	H	H	H	2-bit	
H	L	H	L	L	L	L	unc	
H	L	H	L	L	L	H	2-bit	
H	L	H	L	L	H	L	2-bit	
H	L	H	L	L	H	H	DB13	
H	L	H	L	H	L	L	2-bit	
H	L	H	L	H	L	H	DB12	
H	L	H	L	H	H	L	DB11	
H	L	H	L	H	H	H	2-bit	
H	L	H	H	L	L	L	2-bit	
H	L	H	H	L	L	H	DB10	
H	L	H	H	L	H	L	DB9	
H	L	H	H	L	H	H	2-bit	
H	L	H	H	H	L	L	DB8	
H	L	H	H	H	L	H	2-bit	
H	L	H	H	H	H	L	2-bit	
H	L	H	H	H	H	H	CB5	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
H	H	L	L	L	L	L	unc	
H	H	L	L	L	L	H	2-bit	
H	H	L	L	L	H	L	2-bit	
H	H	L	L	L	H	H	DB23	
H	H	L	L	H	L	L	2-bit	
H	H	L	L	H	L	H	DB22	
H	H	L	L	H	H	L	DB21	
H	H	L	L	H	H	H	2-bit	
H	H	L	H	L	L	L	2-bit	
H	H	L	H	L	L	H	DB20	
H	H	L	H	L	H	L	DB19	
H	H	L	H	L	H	H	2-bit	
H	H	L	H	H	L	L	DB18	
H	H	L	H	H	L	H	2-bit	
H	H	L	H	H	H	L	2-bit	
H	H	L	H	H	H	H	CB4	
H	H	H	L	L	L	L	2-bit	
H	H	H	L	L	L	H	DB16	
H	H	H	L	L	H	L	unc	
H	H	H	L	L	H	H	2-bit	
H	H	H	L	H	L	L	DB17	
H	H	H	L	H	L	H	2-bit	
H	H	H	L	H	H	L	2-bit	
H	H	H	L	H	H	H	CB3	
H	H	H	H	L	L	L	unc	
H	H	H	H	L	L	H	2-bit	
H	H	H	H	L	H	L	2-bit	
H	H	H	H	L	H	H	CB2	
H	H	H	H	H	L	L	2-bit	
H	H	H	H	H	L	H	CB1	
H	H	H	H	H	H	L	CB0	
H	H	H	H	H	H	H	none	

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

TEXAS INSTRUMENTS
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read-modify-write (byte control) operations

The 'ALS632B and 'AS632 are capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	BYTEn†	$\overline{\text{OEBn}}$†	DB OUTPUT LATCH $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

† $\overline{\text{OEB0}}$ controls DB0-DB7 (BYTE0), $\overline{\text{OEB1}}$ controls DB8-DB15 (BYTE1), $\overline{\text{OEB2}}$ controls DB16-DB23 (BYTE2), $\overline{\text{OEB3}}$ controls DB24-DB31 (BYTE3).

diagnostic operations

The 'ALS632B and 'AS632 are capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the check word is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known check word. If the user applies a diagnostic data word with an error in any bit location, the $\overline{\text{ERR}}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{\text{MERR}}$ flag should be low. After the check word is latched into the input latch, it can be verified by taking $\overline{\text{OECB}}$ low. This outputs the latched check word. The diagnostic data word can be latched into the output data latch and verified. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEB}_n$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains output latch	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enable	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bit	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enable	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range: SN74ALS632B, SN74AS632 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			SN74ALS632B			SN74AS632			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4			−0.4	mA
		DB or CB			−2.6			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			8			8	mA
		DB or CB			24			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	20			20			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	5			5			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)‡	30			25			
		(3) $\overline{LEDBO}$ high before the earlier of S0↓ or S1↓‡	0			0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			0			
		(5) Diagnostic data word before S1↑ (S0 = H)	5			5			
		(6) Diagnostic check word before the later of S1↓ or S0↑	7			7			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)§	15			15			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	25			25			ns
		(9) Data and check word after S0↑ (S1 = H)	10			10			
		(10) Data word after S1↑ (S0 = H)	10			10			
		(11) Check word after the later of S1↓ or S0↑	10			10			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)§	0			0			
t_{corr}	Correction time (see Figure 1)¶		37			32			ns
T_A	Operating free-air temperature		0		70	0		70	°C

‡ These times ensure that corrected data is saved in the output data latch.
§ These times ensure that the diagnostic data word is saved in the output data latch.
¶ the t_{corr} specification includes the minimum setup time $t_{su(1)}$. The correction time from S0 going high to valid data is equal to t_{corr} minus $t_{su(1)}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS632B			SN74AS632			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = Open,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5		0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	DB or CB‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	All others‡					20			20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4			−0.4	mA
	All others‡					−0.1			−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 2		157	250		200	300	mA

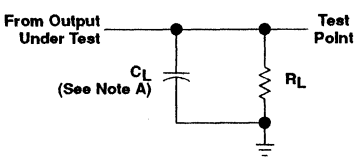
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF†

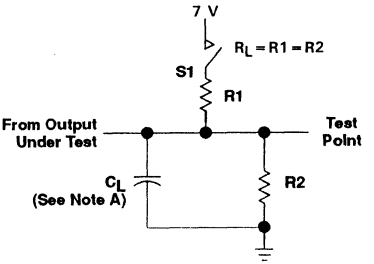
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74ALS632B		SN74AS632		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	5	30	4	25	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	5	30	4	25	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	6	37	5	32	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	6	37	5	32	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	5	32	4	28	
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	3	19	2	17	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	5	30	4	26	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S0 = X, S0 = H, R1 = R2 = 500 Ω	3	18	2	16	ns
t_{pd}	S1↑	CB	S1 = H, R1 = R2 = 500 Ω	4	24	3	20	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	22	1	17	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	20	1	15	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	22	1	17	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	20	1	15	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

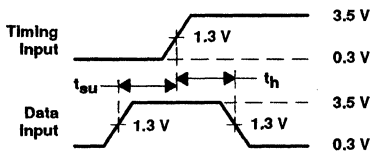
PARAMETER MEASUREMENT INFORMATION



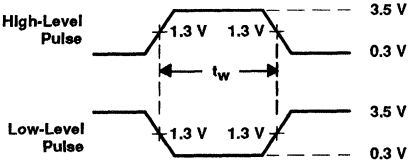
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



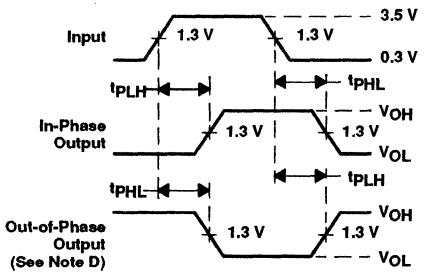
LOAD CIRCUIT FOR 3-STATE OUTPUTS



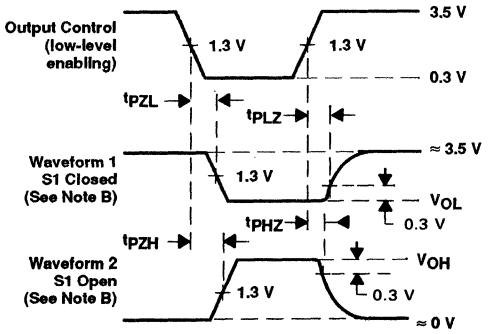
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

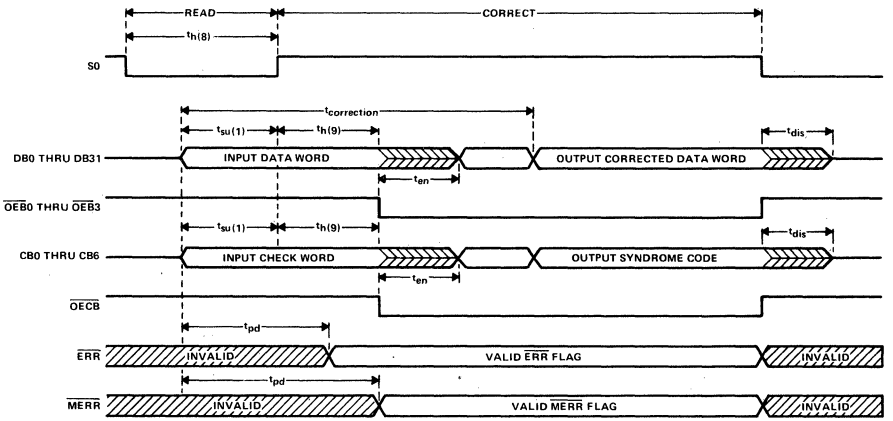


FIGURE 2. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

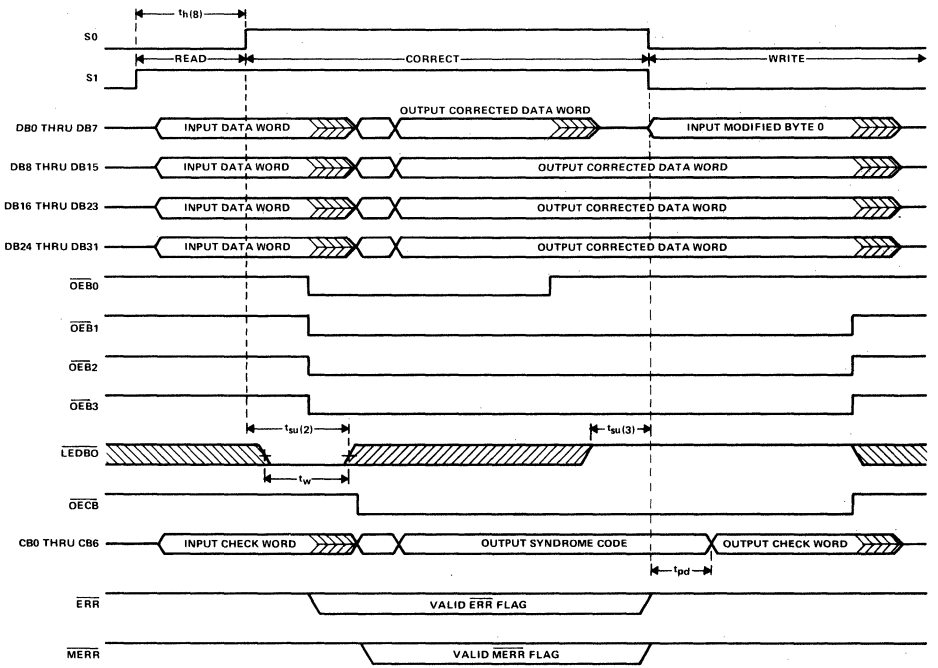


FIGURE 3. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

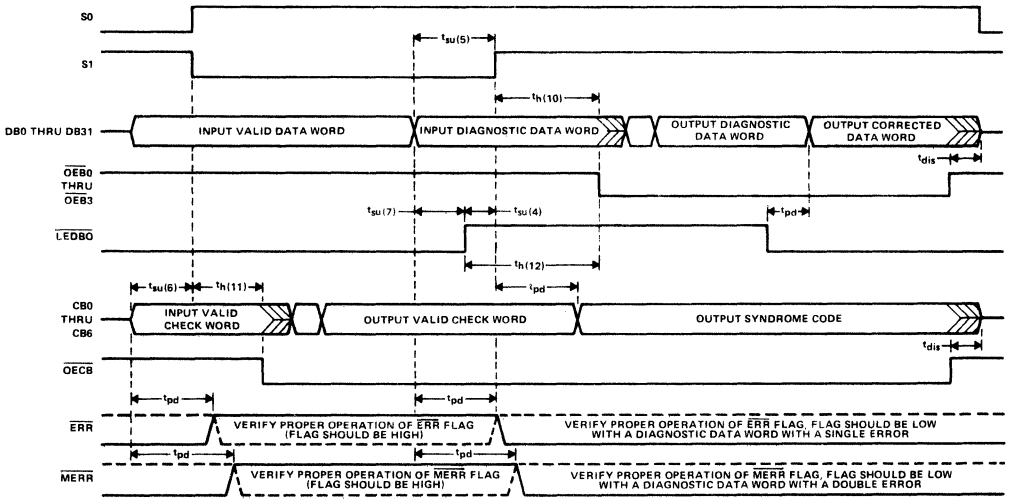


FIGURE 4. DIAGNOSTIC MODE SWITCHING WAVEFORM

D3397, JANUARY 1990

- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Built-In Diagnostic Capability**
- **Fast Write and Read Cycle Processing Times**
- **Byte-Write Capability**
- **Dependable Texas Instruments Quality and Reliability**

description

The 'AS632A device is a 32-bit parallel error detection and correction circuit (EDAC). This EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

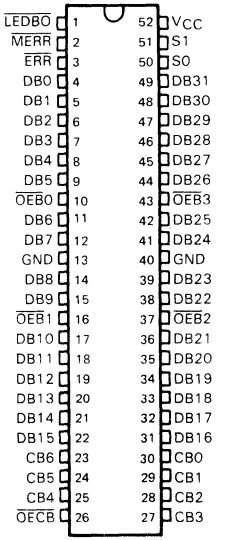
Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit data word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of this device to detect.

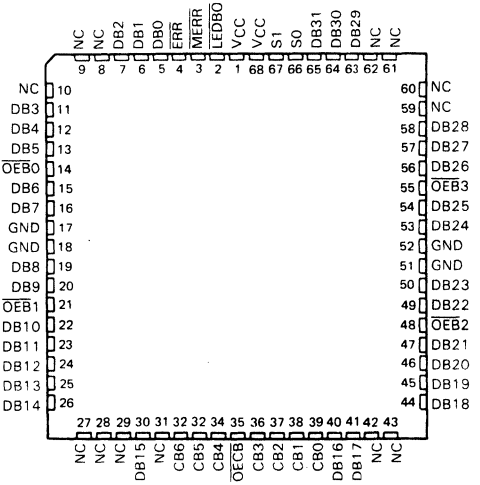
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{\text{LEDBO}}$, and the individual $\overline{\text{OEB0}}$ thru $\overline{\text{OEB3}}$ byte control pins.

Diagnostics are performed on the EDAC by controls and internal paths that allow the user to read the contents of the DB and CB input latches. These will determine if the failure occurred in memory or in the EDAC.

N OR JD PACKAGE
(TOP VIEW)



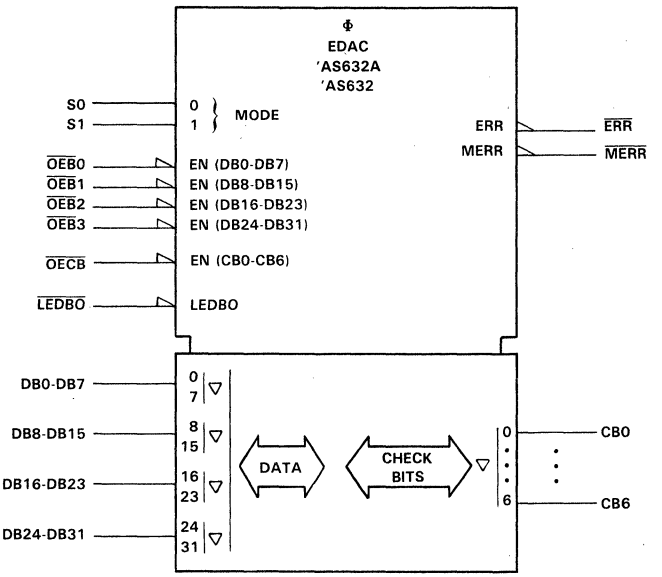
FN PACKAGE
(TOP VIEW)



NC – No internal connection

ADVANCE INFORMATION

logic symbol†

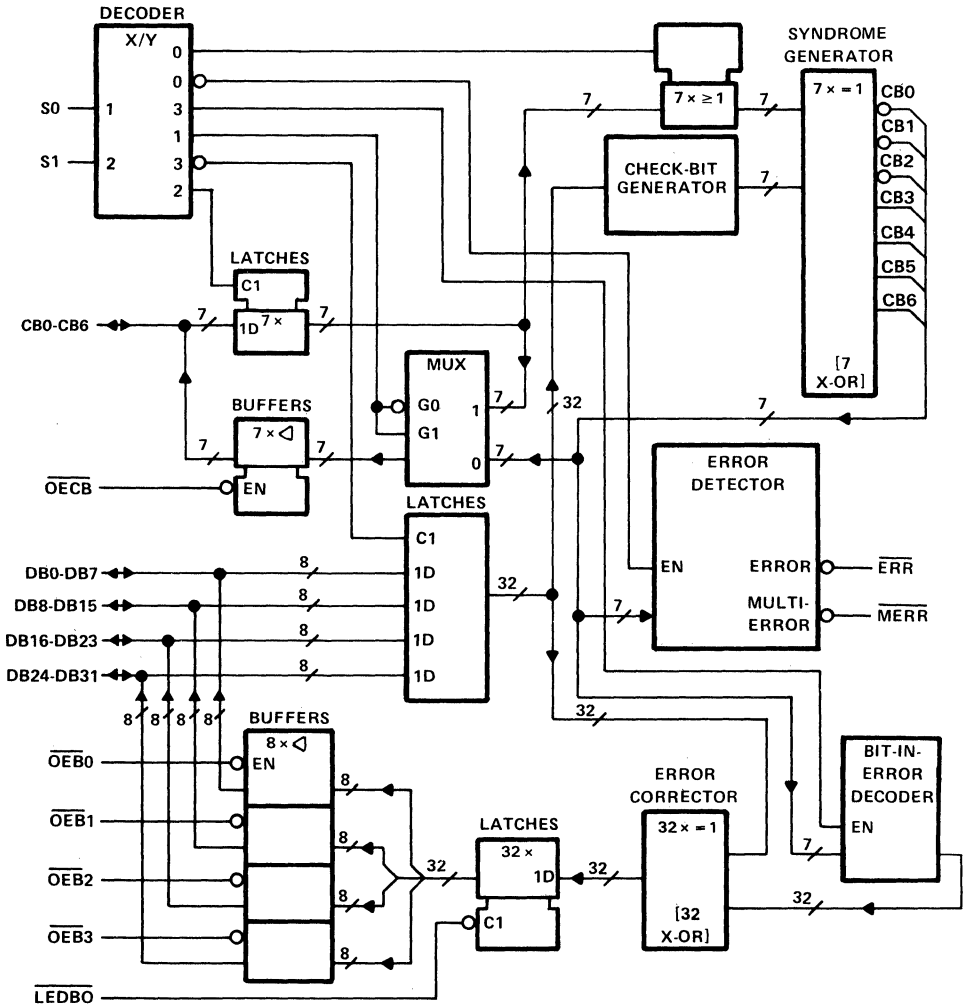


†This symbol is an accordance with ANSI/IEEE-Std 91-1984.

TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
CB0-CB6	Check Bit data port. This 7-bit I/O port is used to output check bits during write cycles and input memory check bits during read cycles.
DB0-DB31	Data port. This 32-bit I/O port is used to input processor data during memory write cycles and used to output corrected data during memory read cycles.
$\overline{ERR}$	Single-Bit Error Flag. This active-low output signals when a single-bit error has occurred. When more than two errors occur, this output is unpredictable.
GND	Ground
$\overline{LEDBO}$	Output Latch Enable. This input controls the output data latch that stores the corrected data word. When low, data is allowed to flow through the latch. When taken high, data present at the inputs of the output data latch is stored.
$\overline{MERR}$	Multiple-Bit Error Flag. This active-low output signals when a double-bit error has occurred. When more than two errors occur, this output is unpredictable.
NC	No internal connection
$\overline{OEB0}$-$\overline{OEB31}$	Data Output Enable controls. These active-low inputs are used to enable data onto the data bus (DB0-DB31). Each input controls 8-bits for byte control operations. $\overline{OEB0}$ controls DB0-DB7, $\overline{OEB1}$ controls DB8-DB15, $\overline{OEB2}$ controls DB16-DB23, and $\overline{OEB3}$ controls DB24-DB31.
$\overline{OECB}$	Check Bit Output Enable control. This active-low input is used to enable the check bits onto the check bit bus (CB0-CB6).
S0,S1	Mode Select controls. These control inputs select the mode of the EDAC. See function tables for details.
V_{CC}	Supply voltage

logic diagram (positive logic)



ADVANCE INFORMATION

TABLE 1. WRITE CONTROL FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	DATA I/O	DB CONTROL $\overline{OEB_n}$ OR $\overline{OEDB}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Write	Generate check word	L	L	Input	H	X	Output check bits†	L	H	H

†See Table 2 for details on check bit generation.

memory write cycle details

During a memory write cycle, the check bits (CB0 thru CB6) are generated internally in the EDAC by seven 16-input parity generators using the 32-bit data word as defined in Table 2. These seven check bits are stored in memory along with the original 32-bit data word. This 32-bit word will later be used in the memory read cycle for error detection and correction. CB0, CB1 and CB2 are odd parity bits and CB3, CB4, CB5, and CB6 are even parity bits. For example, for a data word of all zeros CB0-CB2 will be high and CB3-CB6 will be low.

TABLE 2. PARITY ALGORITHM

CHECK WORD BIT	32-BIT DATA WORD																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X				X	X		X			X	X		X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

error detection and correction details

During a memory read cycle, the 7-bit check word is retrieved along with the actual data. In order to be able to determine whether the data from memory is acceptable to use as presented to the bus, the error flags must be tested to determine if they are at the high level.

The first case in Table 3 represents the normal, no-error conditions. The EDAC presents highs on both flags. The next two cases of single-bit errors give a high on $\overline{MERR}$ and a low on $\overline{ERR}$, which is the signal for a correctable error, and the EDAC should be sent through the correction cycle. The last three cases of double-bit errors will cause the EDAC to signal lows on both $\overline{ERR}$ and $\overline{MERR}$, which is the interrupt indication for the CPU.

ADVANCE INFORMATION

TABLE 3. ERROR FUNCTION

TOTAL NUMBER OF ERRORS		ERROR FLAGS		DATA CORRECTION
32-BIT DATA WORD	7-BIT CHECK WORD	$\overline{ERR}$	$\overline{MERR}$	
0	0	H	H	Not applicable
1	0	L	H	Correction
0	1	L	H	Correction
1	1	L	L	Interrupt
2	0	L	L	Interrupt
0	2	L	L	Interrupt

Error detection is accomplished as the 7-bit check word and the 32-bit data word from memory are applied to internal parity generators/checkers. If the parity of all seven groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be high.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set low. Any single error in the 32-bit data word will change the state of either three or five bits of the 7-bit check word. Any single error in the 7-bit check word changes the state of only that one bit. In either case, the single error flag ($\overline{ERR}$) will be set low while the dual error flag ($\overline{MERR}$) will remain high.

Any two-bit error will change the state of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set low when any two-bit error is detected.

Three or more simultaneous bit errors can cause the EDAC to believe that no error, a correctable error, or an uncorrectable error has occurred and will produce erroneous results in all three cases. It should be noted that the gross-error conditions of all lows and all highs will be detected.

TABLE 4. READ, FLAG, AND CORRECT FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	DATA I/O	DB CONTROL $\overline{OEBn}$ OR $\overline{OEDB}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$ $\overline{MERR}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled†
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled†
Read	Output Corrected data & syndrome bits	H	H	Output corrected data word	L	X	Output syndrome bits‡	L	Enabled†

†See Table 3 for error description.
‡See Table 5 for error location.

As the corrected word is made available on the data I/O port (DB0 thru DB31), the check word I/O port (CB0 thru CB6) presents a 7-bit syndrome error code. This syndrome error code can be used to locate the bad memory chip. See Table 5 for syndrome decoding.

ADVANCE INFORMATION

TABLE 5. SYNDROME DECODING

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
L	L	L	L	L	L	L	unc	
L	L	L	L	L	L	H	2-bit	
L	L	L	L	L	H	L	2-bit	
L	L	L	L	L	H	H	unc	
L	L	L	L	H	L	L	2-bit	
L	L	L	L	H	L	H	unc	
L	L	L	L	H	H	L	unc	
L	L	L	L	H	H	H	2-bit	
L	L	L	H	L	L	L	2-bit	
L	L	L	H	L	L	H	unc	
L	L	L	H	L	H	L	DB31	
L	L	L	H	L	H	H	2-bit	
L	L	L	H	H	L	L	unc	
L	L	L	H	H	L	H	2-bit	
L	L	L	H	H	H	L	2-bit	
L	L	L	H	H	H	H	DB30	
L	L	H	L	L	L	L	2-bit	
L	L	H	L	L	L	H	unc	
L	L	H	L	L	H	L	DB29	
L	L	H	L	L	H	H	2-bit	
L	L	H	L	H	L	L	DB28	
L	L	H	L	H	L	H	2-bit	
L	L	H	L	H	H	L	2-bit	
L	L	H	L	H	H	H	DB27	
L	L	H	H	L	L	L	DB26	
L	L	H	H	L	L	H	2-bit	
L	L	H	H	L	H	L	2-bit	
L	L	H	H	L	H	H	DB25	
L	L	H	H	H	L	L	2-bit	
L	L	H	H	H	L	H	DB24	
L	L	H	H	H	H	L	unc	
L	L	H	H	H	H	H	2-bit	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
L	H	L	L	L	L	L	2-bit	
L	H	L	L	L	L	H	unc	
L	H	L	L	L	H	L	DB7	
L	H	L	L	L	H	H	2-bit	
L	H	L	L	H	L	L	DB6	
L	H	L	L	H	L	H	2-bit	
L	H	L	L	H	H	L	2-bit	
L	H	L	L	H	H	H	DB5	
L	H	L	H	L	L	L	DB4	
L	H	L	H	L	L	H	2-bit	
L	H	L	H	L	H	L	2-bit	
L	H	L	H	L	H	H	DB3	
L	H	L	H	H	L	L	2-bit	
L	H	L	H	H	L	H	DB2	
L	H	L	H	H	H	L	unc	
L	H	L	H	H	H	H	2-bit	
L	H	H	L	L	L	L	DB0	
L	H	H	L	L	L	H	2-bit	
L	H	H	L	L	H	L	2-bit	
L	H	H	L	L	H	H	unc	
L	H	H	L	H	L	L	2-bit	
L	H	H	L	H	L	H	DB1	
L	H	H	L	H	H	L	unc	
L	H	H	L	H	H	H	2-bit	
L	H	H	H	L	L	L	2-bit	
L	H	H	H	L	L	H	unc	
L	H	H	H	L	H	L	unc	
L	H	H	H	L	H	H	2-bit	
L	H	H	H	H	L	L	unc	
L	H	H	H	H	L	H	2-bit	
L	H	H	H	H	H	L	2-bit	
L	H	H	H	H	H	H	CB6	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
H	L	L	L	L	L	L	2-bit	
H	L	L	L	L	L	H	unc	
H	L	L	L	L	H	L	unc	
H	L	L	L	L	H	H	2-bit	
H	L	L	L	H	L	L	unc	
H	L	L	L	H	L	H	2-bit	
H	L	L	L	H	H	L	2-bit	
H	L	L	L	H	H	H	unc	
H	L	L	H	L	L	L	unc	
H	L	L	H	L	L	H	2-bit	
H	L	L	H	L	H	L	2-bit	
H	L	L	H	L	H	H	DB15	
H	L	L	H	H	L	L	2-bit	
H	L	L	H	H	L	H	unc	
H	L	L	H	H	H	L	DB14	
H	L	L	H	H	H	H	2-bit	
H	L	H	L	L	L	L	unc	
H	L	H	L	L	L	H	2-bit	
H	L	H	L	L	H	L	2-bit	
H	L	H	L	L	H	H	DB13	
H	L	H	L	H	L	L	2-bit	
H	L	H	L	H	L	H	DB12	
H	L	H	L	H	H	L	DB11	
H	L	H	L	H	H	H	CB3	
H	L	H	H	L	L	L	2-bit	
H	L	H	H	L	L	H	DB10	
H	L	H	H	L	H	L	DB9	
H	L	H	H	L	H	H	CB2	
H	L	H	H	H	L	L	DB8	
H	L	H	H	H	L	H	CB1	
H	L	H	H	H	H	L	CB0	
H	L	H	H	H	H	H	CB5	

SYNDROME BITS								ERROR
6	5	4	3	2	1	0		
H	H	L	L	L	L	L	unc	
H	H	L	L	L	L	H	2-bit	
H	H	L	L	L	H	L	2-bit	
H	H	L	L	L	H	H	DB23	
H	H	L	L	H	L	L	2-bit	
H	H	L	L	H	L	H	DB22	
H	H	L	L	H	H	L	DB21	
H	H	L	L	H	H	H	2-bit	
H	H	L	H	L	L	L	2-bit	
H	H	L	H	L	L	H	DB20	
H	H	L	H	L	H	L	DB19	
H	H	L	H	L	H	H	2-bit	
H	H	L	H	H	L	L	DB18	
H	H	L	H	H	L	H	2-bit	
H	H	L	H	H	H	L	DB14	
H	H	L	H	H	H	H	CB4	
H	H	H	L	L	L	L	2-bit	
H	H	H	L	L	L	H	DB16	
H	H	H	L	L	H	L	unc	
H	H	H	L	L	H	H	2-bit	
H	H	H	L	H	L	L	DB17	
H	H	H	L	H	L	H	2-bit	
H	H	H	L	H	H	L	2-bit	
H	H	H	L	H	H	H	CB3	
H	H	H	H	L	L	L	unc	
H	H	H	H	L	L	H	2-bit	
H	H	H	H	L	H	L	2-bit	
H	H	H	H	L	H	H	CB2	
H	H	H	H	H	L	L	2-bit	
H	H	H	H	H	L	H	CB1	
H	H	H	H	H	H	L	CB0	
H	H	H	H	H	H	H	none	

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

ADVANCE INFORMATION

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read-modify-write (byte control) operations

The 'AS632A is capable of byte-write operations. The 39-bit word from memory must first be latched into the DB and CB input latches. This is easily accomplished by switching from the read and flag mode (S1 = H, S0 = L) to the latch input mode (S1 = H, S0 = H). The EDAC will then make any corrections, if necessary, to the data word and place it at the input of the output data latch. This data word must then be latched into the output data latch by taking $\overline{\text{LEDBO}}$ from a low to a high.

Byte control can now be employed on the data word through the $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ controls. $\overline{\text{OEB0}}$ controls DB0-DB7 (byte 0), $\overline{\text{OEB1}}$ controls DB8-DB15 (byte 1), $\overline{\text{OEB2}}$ controls DB16-DB23 (byte 2), and $\overline{\text{OEB3}}$ controls DB24-DB31 (byte 3). Placing a high on the byte control will disable the output and the user can modify the byte. If a low is placed on the byte control, then the original byte is allowed to pass onto the data bus unchanged. If the original data word is altered through byte control, a new check word must be generated before it is written back into memory. This is easily accomplished by taking control S1 and S0 low. Table 6 lists the read-modify-write functions.

TABLE 6. READ-MODIFY-WRITE FUNCTION

MEMORY CYCLE	EDAC FUNCTION	CONTROL S1	CONTROL S2	BYTEn†	$\overline{\text{OEBn}}$†	DB OUTPUT LATCH $\overline{\text{LEDBO}}$	CHECK I/O	CB CONTROL	ERROR FLAGS $\overline{\text{ERR}}$	ERROR FLAGS $\overline{\text{MERR}}$
Read	Read & flag	H	L	Input	H	X	Input	H	Enabled	
Read	Latch input data & check bits	H	H	Latched input data	H	L	Latched input check word	H	Enabled	
Read	Latch corrected data word into output latch	H	H	Latched output data word	H	H	Hi-Z	H	Enabled	
							Output Syndrome bits	L		
Modify /write	Modify appropriate byte or bytes & generate new check word	L	L	Input modified BYTE0	H	H	Output check word	L	H	H
				Output unchanged BYTE0	L					

† $\overline{\text{OEB0}}$ controls DB0-DB7 (BYTE0), $\overline{\text{OEB1}}$ controls DB8-DB15 (BYTE1), $\overline{\text{OEB2}}$ controls DB16-DB23 (BYTE2), $\overline{\text{OEB3}}$ controls DB24-DB31 (BYTE3).

diagnostic operations

The 'AS632A is capable of diagnostics that allow the user to determine whether the EDAC or the memory is failing. The diagnostic function tables will help the user to see the possibilities for diagnostic control.

In the diagnostic mode (S1 = L, S0 = H), the check word is latched into the input latch while the data input latch remains transparent. This lets the user apply various data words against a fixed known check word. If the user applies a diagnostic data word with an error in any bit location, the $\overline{\text{ERR}}$ flag should be low. If a diagnostic data word with two errors in any bit location is applied, the $\overline{\text{MERR}}$ flag should be low. After the check word is latched into the input latch, it can be verified by taking $\overline{\text{OECB}}$ low. This outputs the latched check word. The diagnostic data word can be latched into the output data latch and verified. By changing from the diagnostic mode (S1 = L, S0 = H) to the correction mode (S1 = H, S0 = H), the user can verify that the EDAC will correct the diagnostic data word. Also, the syndrome bits can be produced to verify that the EDAC pinpoints the error location. Table 7 lists the diagnostic functions.

TABLE 7. DIAGNOSTIC FUNCTION

EDAC FUNCTION	CONTROL S1	CONTROL S0	DATA I/O	DB BYTE CONTROL $\overline{OEB_n}$	DB OUTPUT LATCH $\overline{LEDBO}$	CHECK I/O	CB CONTROL $\overline{OECB}$	ERROR FLAGS $\overline{ERR}$	ERROR FLAGS $\overline{MERR}$
Read & flag	H	L	Input correct data word	H	X	Input correct check bits	H	H	H
Latch input check word while data input latch remains output latch	L	H	Input diagnostic data word†	H	L	Latched input check bits	H	Enable	
Latch diagnostic data word into output latch	L	H	Input diagnostic data word†	H	H	Output latched check bit	L	Enabled	
						Hi-Z	H		
Latch diagnostic data word into input latch	H	H	Latched input diagnostic data word	H	H	Output syndrome bits	L	Enable	
						Hi-Z	H		
Output diagnostic data word & syndrome bits	H	H	Output diagnostic data word	L	H	Output syndrome bits	L	Enabled	
						Hi-Z	H		
Output corrected diagnostic data word & output syndrome	H	H	Output corrected diagnostic data word	L	L	Output syndrome bits	L	Enabled	
						Hi-Z	H		

†Diagnostic data is a data word with an error in one bit location except when testing the $\overline{MERR}$ error flag. In this case, the diagnostic data word will contain errors in two bit locations.

ADVANCE INFORMATION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CB and DB . . . . . 5.5 V
All others . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	$\overline{ERR}$ or $\overline{MERR}$			−0.4	mA
		DB or CB			−2.6	
I_{OL}	Low-level output current	$\overline{ERR}$ or $\overline{MERR}$			8	mA
		DB or CB			24	
t_w	Pulse duration	$\overline{LEDBO}$ low	14			ns
t_{su}	Setup time	(1) Data and check word before S0↑ (S1 = H)	4			ns
		(2) S0 high before $\overline{LEDBO}$↑ (S1 = H)‡	20			
		(3) LEDBO high before the earlier of S0↓ or S1↓‡	0			
		(4) $\overline{LEDBO}$ high before S1↑ (S0 = H)	0			
		(5) Diagnostic data word before S1↑ (S0 = H)	4			
		(6) Diagnostic check word before the later of S1↓ or S0↑	5			
		(7) Diagnostic data word before $\overline{LEDBO}$↑ (S1 = L and S0 = H)§	12			
t_h	Hold time	(8) Read-mode, S0 low and S1 high	15			ns
		(9) Data and check word after S0↑ (S1 = H)	6			
		(10) Data word after S1↑ (S0 = H)	7			
		(11) Check word after the later of S1↓ or S0↑	7			
		(12) Diagnostic data word after $\overline{LEDBO}$↑ (S1 = L, S0 = H)§	0			
t_{corr}	Correction time (see Figure 1)¶		24			ns
T_A	Operating free-air temperature		0		70	°C

‡These times ensure that corrected data is saved in the output data latch.

§These times ensure that the diagnostic data word is saved in the output data latch.

¶the t_{corr} specification includes the minimum setup time $t_{su(1)}$. The correction time from S0 going high to valid data is equal to t_{corr} minus $t_{su(1)}$

ADVANCE INFORMATION

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = Open,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	DB or CB	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	$\overline{ERR}$ or $\overline{MERR}$	V_{CC} = 4.5 V,	I_{OH} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	DB or CB	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
I_I	S0 or S1	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}	DB or CB‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	All others‡					20	
I_{IL}	S0 or S1	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.4	mA
	All others‡					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 2		215	330	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: I_{CC} is measured with S0 and S1 at 4.5 V and all CB and DB pins grounded.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	DB and CB	$\overline{ERR}$	S1 = H, S0 = L, R_L = 500 Ω	4	18	ns
	DB	$\overline{ERR}$	S1 = L, S0 = H, R_L = 500 Ω	4	18	
t_{pd}	DB and CB	$\overline{MERR}$	S1 = H, S0 = L, R_L = 500 Ω	5	23	ns
	DB	$\overline{MERR}$	S1 = L, S0 = H, R_L = 500 Ω	5	23	
t_{pd}	S0↓ and S1↓	CB	R1 = R2 = 500 Ω	4	20	ns
t_{PLH}	S0↓ and S1↓	$\overline{ERR}$	R_L = 500 Ω	2	12	ns
t_{pd}	DB	CB	S1 = L, S0 = L, R1 = R2 = 500 Ω	4	18	ns
t_{pd}	$\overline{LEDBO}$↓	DB	S0 = X, S0 = H, R1 = R2 = 500 Ω	2	11	ns
t_{pd}	S1↑	CB	S1 = H, R1 = R2 = 500 Ω	3	14	ns
t_{pd}	S0↓	ERR↓	S1 = H, R_L = 500 Ω	4	17	ns
t_{en}	$\overline{OECB}$↓	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	12	ns
t_{dis}	$\overline{OECB}$↑	CB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	10	ns
t_{en}	$\overline{OEB0}$ thru $\overline{OEB3}$↓	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	12	ns
t_{dis}	$\overline{OEB0}$ thru $\overline{OEB3}$↑	DB	S0 = H, S1 = X, R1 = R2 = 500 Ω	1	10	ns

†See Parameter Measurement Information for load circuit and voltage waveforms.

ADVANCE INFORMATION

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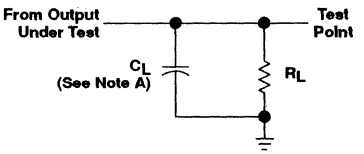
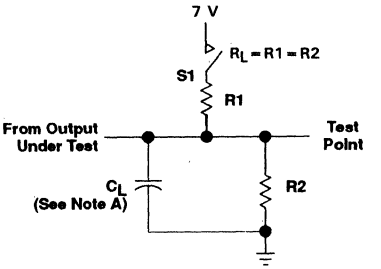
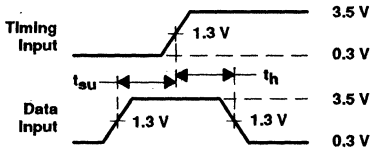
PARAMETER MEASUREMENT INFORMATION



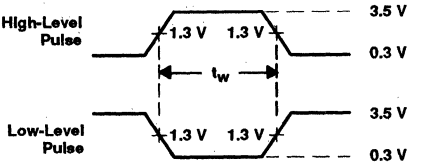
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



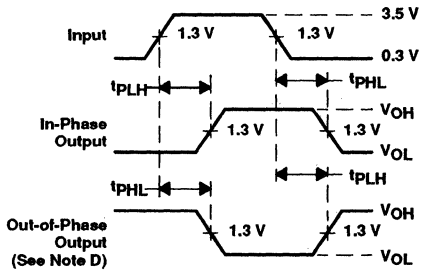
LOAD CIRCUIT FOR 3-STATE OUTPUTS



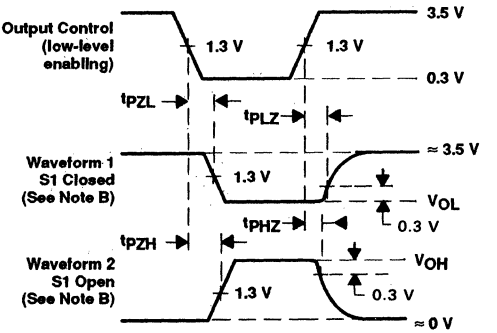
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

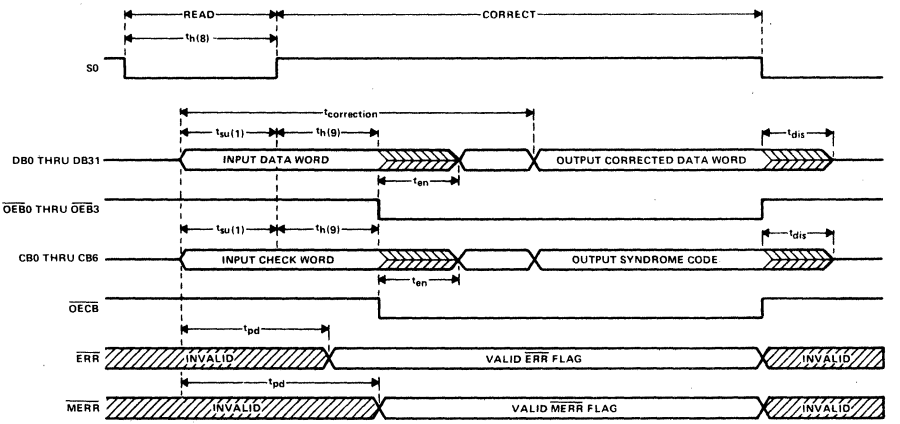


FIGURE 2. READ, FLAG, AND CORRECT MODE SWITCHING WAVEFORMS

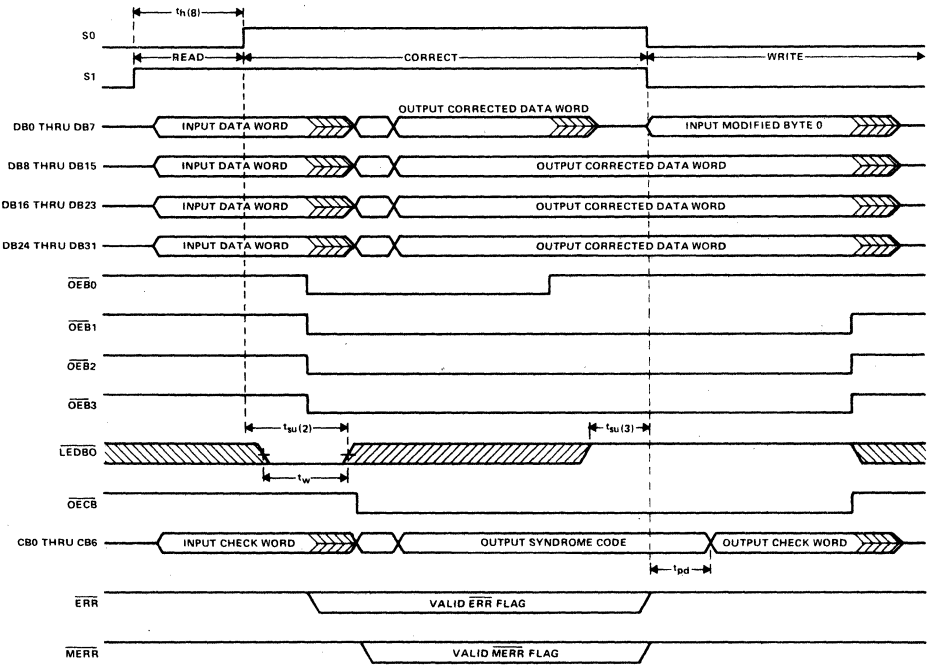


FIGURE 3. READ, CORRECT, MODIFY MODE SWITCHING WAVEFORMS

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PARAMETER MEASUREMENT INFORMATION

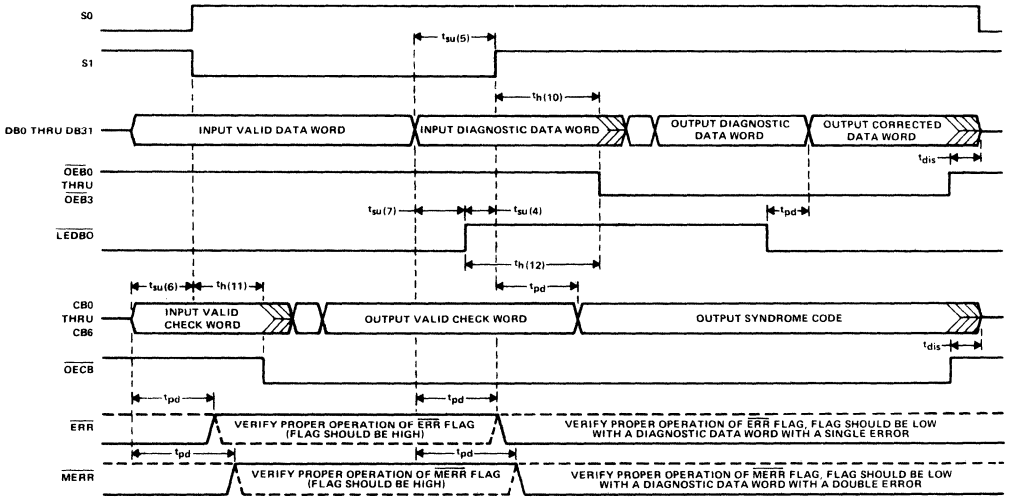


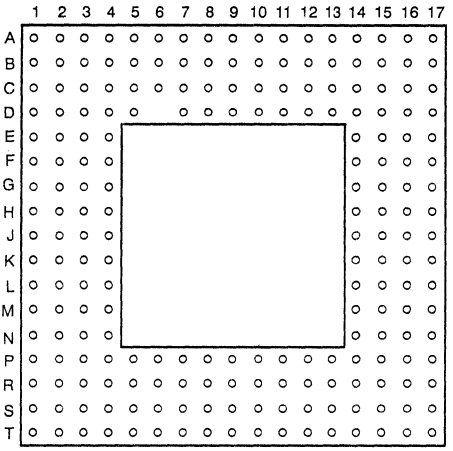
FIGURE 4. DIAGNOSTIC MODE SWITCHING WAVEFORM

ADVANCE INFORMATION

D3312, FEBRUARY 1990–REVISED JUNE 1990

- **12-ns Max Pass-Thru Operation When Used in Correct-Only-On-Error Configurations**
- **Detects and Corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Improved Performance with Flow-Thru Architecture**
- **Simplified Control Logic Matches Standard TTL/HCMOS '245 Bus Transceiver Logic**
- **Byte-Write Capability**
- **Built-In Diagnostic Capability**
- **Memory Initialization**
- **Heavy-Duty 48-mA Drive on Processor Data Bus**
- **Memory Data Bus Features Balanced Output Impedances for Safe Undershoot Characteristics**

17 X 17 GA PACKAGE
(TOP VIEW)



description

The SN74 AS6364 is a 64-bit Parallel Error Detection and Correction circuit (EDAC) featuring a flow-thru architecture for improved performance and ease of control. Two separate 64-bit I/O ports are provided that allow direct interface to the processor and memory data buses. The processor I/O port is designed for 48-mA drive, matching standard Advanced Schottky bus interface performance. The memory I/O port has been designed for balanced output impedances (25 Ω high and low). This feature optimizes the drive low characteristics, based on safe undershoot.

Interfacing to the 'AS6364 has been greatly simplified due to the flow-thru architecture. Data flow is handled in the same manner as used on conventional TTL/HCMOS '245 bus transceivers via a direction-control pin (DIR) and a master enable/disable pin ($\overline{G}$). In its simplest form, the direction-control pin can be driven from the processor R/$\overline{W}$ pin. When the DIR control pin is taken low (write cycle), processor data is allowed to flow through the EDAC unaltered. The 8-bit check word appears on the check word I/O bus after the specified propagation delay.

Pin locations are shown above. Pin location D6 has been omitted for indexing purposes.

Pin assignments for the 207 used pins are given on the following page. Pin-function descriptions are given on the page after.

When the direction-control input is taken high for a read cycle, memory data and its associated check word is allowed to flow into the EDAC. The 8-bit check word is then compared against a new check word generated from the 64-bit data word. The resulting syndrome code is decoded by the error detection logic and signals the occurrence of an error. The single bit Error Flag ($\overline{ERR}$) informs the user that at least a single-bit error has occurred. The Multiple-Bit Error Flag ($\overline{MERR}$) informs the user that at least a double-bit error has occurred. The Correctable Error Flag ($\overline{CERR}$) lets the user know that a correctable, single-bit error has occurred ($\overline{ERR}$ low, $\overline{MERR}$ high). In the cases where multiple-bit errors have occurred, it is possible to fool the EDAC into believing a correctable single-bit error has occurred.

ADVANCE INFORMATION

PIN ASSIGNMENTS

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A1	MD21	C2	MD14	E3	MD10	J15	GND	P1	CB6	S2	D10
A2	MD22	C3	MD15	E4	V_{CC}	J16	SYN5	P2	D4	S3	$\overline{OEB}$1
A3	MD24	C4	MD19	E14	MD54	J17	SYN6	P3	D11	S4	D16
A4	MD28	C5	MD23	E15	MD61	K1	CB1	P4	V_{CC}	S5	D17
A5	MD33	C6	GND	E16	$\overline{ERR}$	K2	CB4	P5	GND	S6	D23
A6	MD29	C7	MD27	E17	SYN3	K3	D1	P6	D18	S7	D27
A7	MD34	C8	GND	F1	MD7	K4	V_{CC}	P7	GND	S8	D25
A8	MD36	C9	GND	F2	MD5	K14	GND	P8	V_{CC}	S9	D29
A9	MD38	C10	GND	F3	MD6	K15	D63	P9	V_{CC}	S10	$\overline{OEB}$3
A10	MD41	C11	MD42	F4	GND	K16	D62	P10	GND	S11	$\overline{OEB}$4
A11	MD43	C12	MD46	F14	GND	K17	D61	P11	GND	S12	D36
A12	MD44	C13	MD48	F15	MD62	L1	$\overline{OEB}$0	P12	GND	S13	D39
A13	MD47	C14	MD52	F16	DIR	L2	D2	P13	GND	S14	D40
A14	MD50	C15	MD58	F17	SYN0	L3	GND	P14	GND	S15	D44
A15	MD55	C16	$\overline{CERR}$	G1	MD2	L4	V_{CC}	P15	D50	S16	$\overline{OEB}$5
A16	MD53	C17	LE	G2	MD3	L14	V_{CC}	P16	D51	S17	$\overline{OEB}$6
A17	MD60	D1	MD11	G3	MD4	L15	V_{CC}	P17	D55	T1	D9
B1	MD18	D2	MD12	G4	GND	L16	D60	R1	D0	T2	D12
B2	MD16	D3	MD13	G14	V_{CC}	L17	D59	R2	D7	T3	D14
B3	MD20	D4	GND	G15	$\overline{DIAG}$	M1	CB2	R3	D15	T4	D19
B4	MD25	D5	GND	G16	SYN2	M2	D5	R4	$\overline{OEB}$2	T5	D20
B5	MD26	D6		G17	SYN7	M3	GND	R5	GND	T6	D24
B6	MD31	D7	V_{CC}	H1	MD1	M4	GND	R6	D21	T7	D28
B7	MD30	D8	V_{CC}	H2	MD0	M14	V_{CC}	R7	D22	T8	D31
B8	MD32	D9	MD35	H3	CB0	M15	GND	R8	D26	T9	D33
B9	MD37	D10	V_{CC}	H4	V_{CC}	M16	D57	R9	D30	T10	D34
B10	MD39	D11	V_{CC}	H14	$\overline{INIT}$	M17	D58	R10	D38	T11	D37
B11	MD40	D12	GND	H15	SNY1	N1	CB5	R11	V_{CC}	T12	D32
B12	MD45	D13	GND	H16	SYN4	N2	D6	R12	V_{CC}	T13	D35
B13	MD49	D14	V_{CC}	H17	$\overline{OEB}$7	N3	D8	R13	D43	T14	D41
B14	MD51	D15	MD56	J1	CORR	N4	D13	R14	D47	T15	D42
B15	MD57	D16	$\overline{MERR}$	J2	CB3	N14	GND	R15	D48	T16	D45
B16	MD59	D17	$\overline{G}$	J3	GND	N15	D56	R16	D49	T17	D46
B17	MD63	E1	MD8	J4	CB7	N16	D53	R17	D52		
C1	MD17	E2	MD9	J14	V_{CC}	N17	D54	S1	D3		

description (continued)

The syndrome code is used by the error decoder and correction logic to fix any single-bit error that may have occurred. If a multiple-bit error has been detected, data is unaltered and passes to the output buffer logic. Data is enabled onto the processor bus via separate output enables ($\overline{OEB}$0-$\overline{OEB}$7). This feature, in conjunction with the input latch, allows the user to perform read-modify-write operations.

In a typical read-modify-write operation, data is first read from memory and corrected as necessary. Each byte of corrected data is then enabled onto the processor bus via individual output enable pins ($\overline{OEB}$0-$\overline{OEB}$7). Any byte that the user wishes to modify is easily accomplished by disabling the appropriate output enable pin and then writing the new byte onto the processor bus. Bytes that have not been modified will continue to be driven onto the processor bus by the EDAC. When the modification process has been completed, the modified data

TERMINAL FUNCTIONS

PIN NAME	DESCRIPTIONS
CB0-CB7	Check Bit data port. This 8-bit I/O port is used to output check bits during write cycles and input memory check bits during read cycles.
$\overline{CERR}$	Correctable Error flag. This active-low output signals when a correctable single-bit error has occured. This signal is the logical equivalent of $\overline{ERR}$ low and $\overline{MERR}$ high. When more than two errors have occured, this output is unpredictable. When disabled by DIR or $\overline{G}$ going high, this output goes high.
CORR	Correct. This active-high input is used to enable error correction during read and diagnostic cycles. When taken inactive (low), error correction is disabled.
$\overline{DIAG}$	Diagnostic. This active-low input is used to enable diagnostic mode operation. In essence, the $\overline{DIAG}$ input simply changes the data flow from the MDx inputs to the input data latch during read cycles.
DIR	Direction control. This input is used to control the data flow through the EDAC. When taken low (write cycle), data flows through the EDAC and check bits are generated after the specified propagation delay. When taken high for a read cycle, data is read from memory and corrected if a single-bit error has occurred. The error syndrome codes are also valid after the specified propagation delay.
D63-D0	Processor Data port. This 64-bit I/O port is used to input processor data during write cycles and used to output corrected data during read cycles.
$\overline{ERR}$	Error. This active-low output signals when all single-bit errors have occurred. When more than two errors have occurred, this output is unpredictable. When disabled by DIR or $\overline{G}$ going high, this output goes high.
$\overline{G}$	Enable. This active-low input is used to enable the two 64-bit buses. When taken inactive (high), all four buses go to the high-impedance state and $\overline{ERR}$, $\overline{MERR}$, and $\overline{CERR}$ go high.
$\overline{INIT}$	Initialization. This active-low input pin forces the inputs to the data latch low. This feature is useful for memory initialization after power-up.
LE	Latch Enable. This input controls the flow of data through the input data latch. When high, data is allowed to flow through the latch. When taken low, the Q outputs will be latched at the levels that were last setup on the processor data bus (D63-D0).
MD63-MD0	Memory Data port. This 64-bit I/O port is used as an input during memory read cycles and used to output processor data during memory write cycles.
$\overline{MERR}$	Multiple Error flag. This active-low output signals when a double-bit error has occurred. When more than two errors have occurred, this output is unpredictable. When disabled by DIR or $\overline{G}$ going high, this output goes high.
$\overline{OEB0}$-$\overline{OEB7}$	Output Enable controls. These active-low inputs are used to enable data onto the processor bus (D0-D63). Each input controls 8-bits for byte control operation. $\overline{OEB0}$ controls D0-D7, $\overline{OEB1}$ controls D8-D15, $\overline{OEB2}$ controls D16-D23, $\overline{OEB3}$ controls D24-D31, $\overline{OEB4}$ controls D32-D39, $\overline{OEB5}$ controls D40-D47, $\overline{OEB6}$ controls D48-D55, and $\overline{OEB7}$ controls D56-D63.
SYN0-SYN7	Syndrome code output port. This 8-bit 3-state output port is used to output syndrome codes during read cycles.

description (continued)

word is saved in the input data latch via the latch enable control pin (LE). The EDAC can then be changed to the write mode (DIR low, $\overline{G}$ low), which causes the new modified data word to be written back into memory along with its new associated check word.

Diagnostics are supported on the 'AS6364 via the Diagnostic ($\overline{DIAG}$) and Correct (CORR) input lines. The $\overline{DIAG}$ pin reverses data flow into the check-bit generator. During read cycles, data is selected from the processor side instead of the memory side when $\overline{DIAG}$ is active (low). Data can be saved in the input latch and compared against a known check word. If the user applies a diagnostic data word with an error in any bit location, the $\overline{ERR}$ flag should respond. Likewise, the error syndrome code should reflect the error location.

The Correct (CORR) input pin is used to enable and disable the error correction circuitry. When taken active (high), all single-bit errors will be corrected. When taken inactive (low), data is allowed to pass through the error correction circuitry unaltered.

During memory write cycles, the check bits (CB7-CB0) are generated using the 64-bit data word as defined in Table 1. These eight check bits are stored in memory, along with the original 64-bit data word. Note that CB0 and CB1 use odd parity, while CB2 through CB7 use even parity. This would mean a data word of all "zeros" would correspond to a check word of 0000 0011 (CB7-CB0).

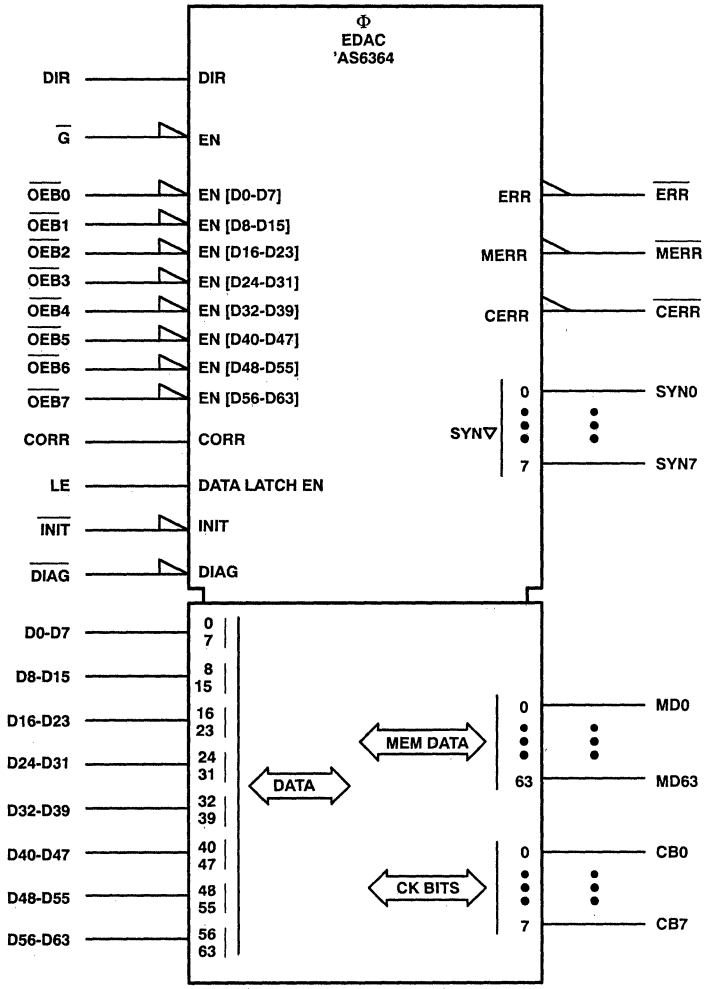
description (continued)

When an error occurs, the syndrome code can be decoded to determine which bit was at fault. The error syndrome code is available every read cycle via the error syndrome bus (SYN7-SYN0). Table 2 defines the error syndrome decoding.

An initialization pin ($\overline{\text{INIT}}$) has been included on the 'AS6364 for the purpose of memory initialization. When this input pin is taken active (low), the inputs to the data latch are forced low. This allows the EDAC to drive a data word of zero, along with its associated check word, when the EDAC is in the check-bit-generation mode (DIR low, LE high).

The initialization mode is useful after power-up when the DRAM contents are random. This feature allows the processor to write all zeros into each memory location along with the appropriate check word.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.

functional block diagram

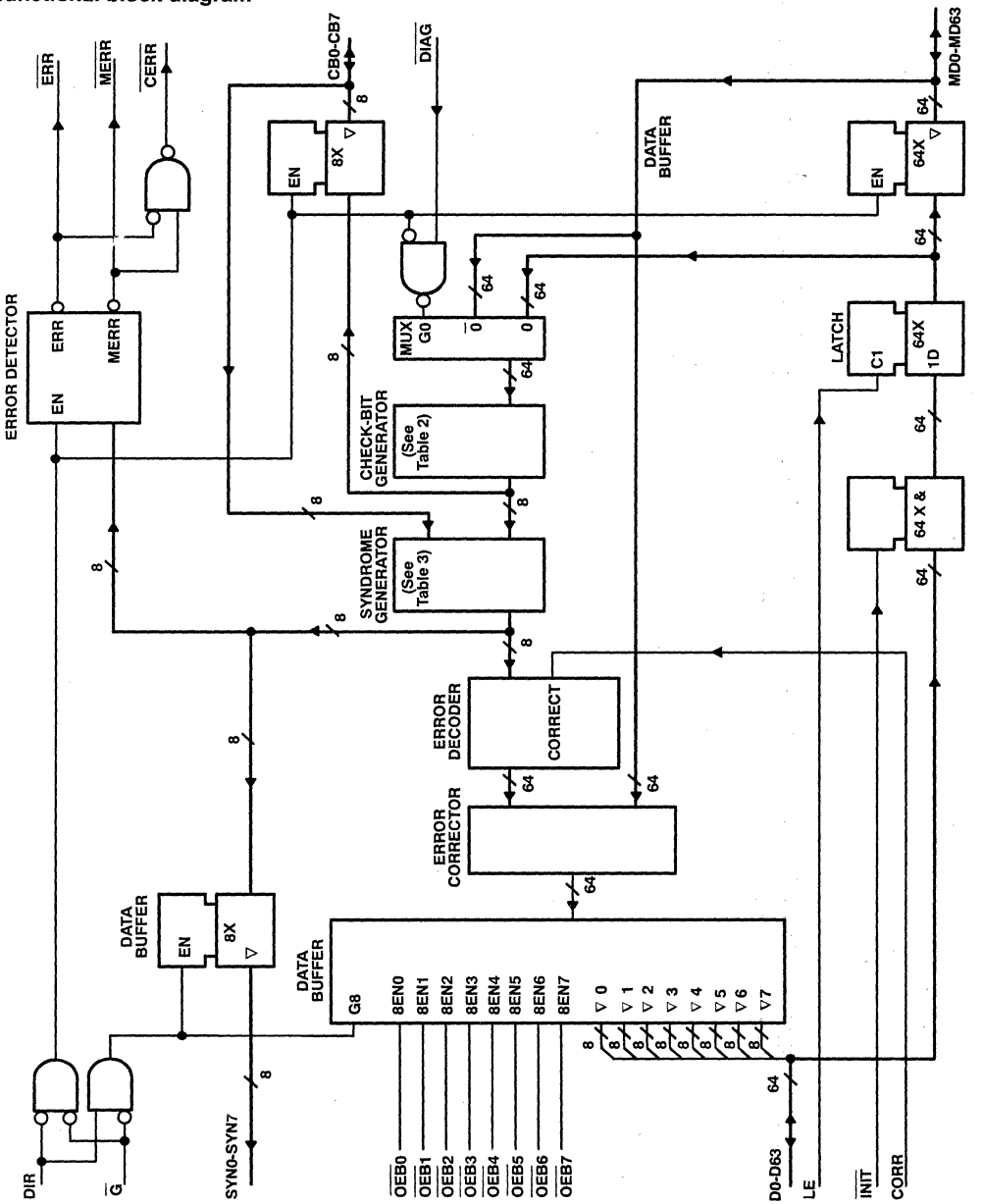


Table 1. Check-Bit-Parity Algorithm

BIT	DATA BIT (PARITY)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	ODD		X	X	X		X			X	X		X			X	
CB1	ODD	X	X	X		X		X		X		X		X			
CB2	EVEN	X			X	X			X		X	X			X		X
CB3	EVEN	X	X				X	X	X				X	X	X		
CB4	EVEN			X	X	X	X	X	X							X	X
CB5	EVEN									X	X	X	X	X	X	X	X
CB6	EVEN	X	X	X	X	X	X	X	X								
CB7	EVEN	X	X	X	X	X	X	X	X								

BIT	DATA BIT (PARITY)	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	ODD		X	X	X		X			X	X		X			X	
CB1	ODD	X	X	X		X		X		X		X		X			
CB2	EVEN	X			X	X			X		X	X			X		X
CB3	EVEN	X	X				X	X	X				X	X	X		
CB4	EVEN			X	X	X	X	X	X							X	X
CB5	EVEN									X	X	X	X	X	X	X	X
CB6	EVEN									X	X	X	X	X	X	X	X
CB7	EVEN									X	X	X	X	X	X	X	X

BIT	DATA BIT (PARITY)	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	ODD	X				X		X	X			X		X	X		X
CB1	ODD	X	X	X		X		X		X		X		X			
CB2	EVEN	X			X	X			X		X	X			X		X
CB3	EVEN	X	X				X	X	X				X	X	X		
CB4	EVEN			X	X	X	X	X	X							X	X
CB5	EVEN									X	X	X	X	X	X	X	X
CB6	EVEN	X	X	X	X	X	X	X	X								
CB7	EVEN									X	X	X	X	X	X	X	X

BIT	DATA BIT (PARITY)	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	ODD	X				X		X	X			X		X	X		X
CB1	ODD	X	X	X		X		X		X		X		X			
CB2	EVEN	X			X	X			X		X	X			X		X
CB3	EVEN	X	X				X	X	X				X	X	X		
CB4	EVEN			X	X	X	X	X	X							X	X
CB5	EVEN									X	X	X	X	X	X	X	X
CB6	EVEN									X	X	X	X	X	X	X	X
CB7	EVEN	X	X	X	X	X	X	X	X								

ADVANCE INFORMATION

Table 2. Error-Syndrome Decoding

ERROR BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SYN0	L	H	H	H	L	H	L	L	H	H	L	H	L	L	H	L	L	H	H
SYN1	H	H	H	L	H	L	H	L	H	L	H	L	H	L	L	L	H	H	H
SYN2	H	L	L	H	H	L	L	H	L	H	H	L	L	H	L	H	H	L	L
SYN3	H	H	L	L	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L
SYN4	L	L	H	H	H	H	H	H	L	L	L	L	L	L	H	H	L	L	H
SYN5	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L
SYN6	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L
SYN7	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L

ERROR BIT	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
SYN0	H	L	H	L	L	H	H	L	H	L	L	H	L	H	L	L	L	H	L
SYN1	L	H	L	H	L	H	L	H	L	H	L	L	L	H	H	H	L	H	L
SYN2	H	H	L	L	H	L	H	H	L	L	H	L	H	H	L	L	H	H	L
SYN3	L	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	H
SYN4	H	H	H	H	H	L	L	L	L	L	L	H	H	L	L	H	H	H	H
SYN5	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L
SYN6	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
SYN7	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L

ERROR BIT	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
SYN0	H	H	L	L	H	L	H	H	L	H	H	L	L	L	H	L	H	H	L
SYN1	H	L	H	L	H	L	H	L	L	L	H	H	H	L	H	L	H	L	H
SYN2	L	H	L	H	H	L	L	H	L	H	H	L	L	H	H	L	L	H	L
SYN3	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	L
SYN4	H	H	L	L	L	L	L	L	H	H	L	L	H	H	H	H	H	H	L
SYN5	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H
SYN6	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
SYN7	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

ERROR BIT	57	58	59	60	61	62	63	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	NO ERRORS
SYN0	L	H	L	H	H	L	H	L	L	L	L	L	L	L	H	L
SYN1	L	H	L	H	L	L	L	L	L	L	L	L	L	H	L	L
SYN2	H	H	L	L	H	L	H	L	L	L	L	L	H	L	L	L
SYN3	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	L
SYN4	L	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L
SYN5	H	H	H	H	H	H	H	L	L	H	L	L	L	L	L	L
SYN6	H	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L
SYN7	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L

H denotes high level, L denotes a low level

ADVANCE INFORMATION

absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, control Inputs ..... 5.5 V
I/O ports ..... 5.5 V
Operating ambient temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	SYNx, $\overline{ERR}$, $\overline{MERR}$, $\overline{CERR}$			−2	mA
		MDx, CBx			−2.6	
		Dx			−15	
I_{OL}	Low-level output current	SYNx, $\overline{ERR}$, $\overline{MERR}$, $\overline{CERR}$			8	mA
		MDx, CBx			12	
		Dx			48	
t_w	Pulse duration, LE high		10			ns
t_{su}	Input setup time, Dx before LE↓		2			ns
t_h	Input hold time, Dx after LE↓		5			ns
T_A	Operating ambient temperature		0		70	°C

ADVANCE INFORMATION

electrical characteristics over recommended operating ambient temperature range (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	SYNx, $\overline{ERR}$, $\overline{MERR}$, $\overline{CERR}$	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = – 2 mA	V_{CC} – 2			V
	MDx, CBx	V_{CC} = 4.75 V,	I_{OH} = – 2.6 mA	2.4	3.2		
	Dx	V_{CC} = 4.75 V,	I_{OH} = – 3 mA	2.4	3.2		
		V_{CC} = 4.75 V,	I_{OH} = – 15 mA	2			
V_{OL}	SYNx, $\overline{ERR}$, $\overline{MERR}$, $\overline{CERR}$	V_{CC} = 4.75 V,	I_{OL} = 8 mA		0.35	0.5	V
	MDx, CBx	V_{CC} = 4.75 V,	I_{OL} = 1 mA		0.15	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 12 mA		0.35	0.8	
	Dx	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}‡	CORR, DIR	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.2	mA
	All others	V_{CC} = 5.25 V,	V_I = 0.4 V			– 0.1	
I_{OZH}	SYNx	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
I_{OZL}	SYNx	V_{CC} = 5.25 V,	V_O = 0.4 V			– 20	µA
I_{OL}	MDx, CBx	V_{CC} = 4.75 V,	V_O = 2 V	30			mA
I_O§		V_{CC} = 5.25 V,	V_O = 2.25 V	– 30		– 112	mA
I_{CC}		V_{CC} = 5.25 V			1.2	1.5	A

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: The SN74AS6364 has been designed to meet these specifications after thermal equilibrium has been established with the circuit in a test socket or mounted on a printed circuit board with transverse air flow greater than 30 meters (100 feet) per minute maintained. Refer to Table 5 for additional information.

ADVANCE INFORMATION

switching characteristics over recommended ranges of supply voltage and operating ambient temperature (unless otherwise noted)†

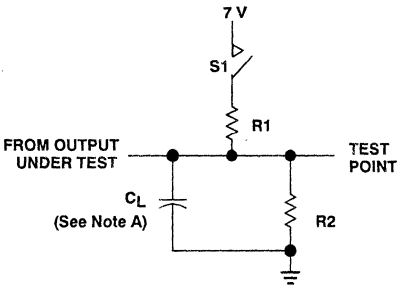
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.75 V to 5.25 V, R1 = R2 = 500 Ω, T_A = 0°C to 70°C			UNIT
			MIN	TYP‡	MAX	
t_{pd}	Dx	MDx		9	16	ns
t_{pd}	Dx	CBx		10	16	ns
t_{pd}	LE↑	MDx		10	15	ns
t_{pd}	MDx and CBx (CORR = L)	Dx		7	12	ns
t_{pd}	MDx and CBx (CORR = H)	Dx		15	20	ns
t_{pd}	MDx and CBx	SYNx		16	20	ns
t_{pd}	CORR	Dx		7	12	ns
t_{pd}	$\overline{INIT}$	CBx, MDx		12	20	ns
t_{pd}	$\overline{DIAG}$	Dx		12	16	ns
t_{pd}	$\overline{DIAG}$	SYNx		12	16	ns
t_{pd}	MDx and CBx	$\overline{ERR}$		10	16	ns
t_{pd}	MDx and CBx	$\overline{MERR}$		15	20	ns
t_{pd}	MDx and CBx	$\overline{CERR}$		15	20	ns
t_{en}	$\overline{OEBx}$↓	Dx		5	10	ns
t_{en}	DIR↓	MDx		9	16	ns
t_{en}	DIR↓	CBx		15	20	ns
t_{en}	$\overline{G}$↓	Dx		7	12	ns
t_{en}	$\overline{G}$↓	MDx		10	15	ns
t_{en}	$\overline{G}$↓	CBx		15	20	ns
t_{en}	$\overline{G}$↓	SYNx		10	15	ns
t_{dis}	$\overline{OEBx}$↑	Dx		4	8	ns
t_{dis}	DIR↑	MDx		5	10	ns
t_{dis}	DIR↑	CBx		5	10	ns
t_{dis}	$\overline{G}$↑	Dx		5	10	ns
t_{dis}	$\overline{G}$↑	MDx		5	10	ns
t_{dis}	$\overline{G}$↑	CBx		5	10	ns
t_{dis}	$\overline{G}$↑	SYNx		5	10	ns

† See Parameter Measurement Information for load circuit and voltage waveforms.

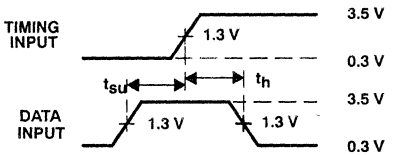
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

ADVANCE INFORMATION

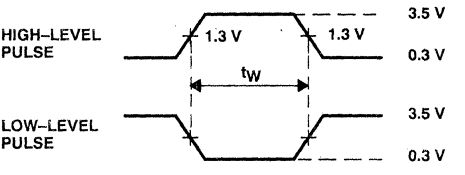
PARAMETER MEASUREMENT INFORMATION



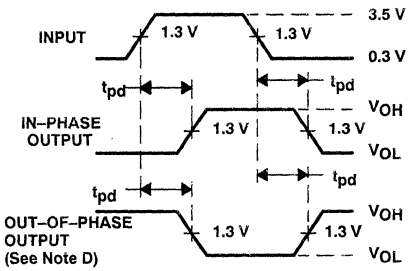
LOAD CIRCUIT FOR
3-STATE OUTPUTS



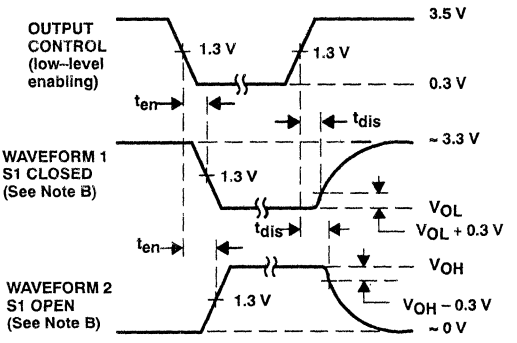
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLED TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is opened.

Figure 1

PARAMETER MEASUREMENT INFORMATION

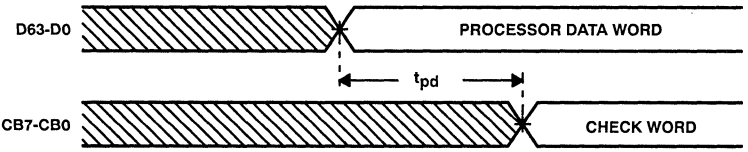


Figure 2. Timing Diagram for Check-Bit Generation

Table 3. Check-Bit Generation

MEMORY CYCLE	EDAC FUNCTION	DIR	$\overline{G}$	D63–D0	$\overline{OEBX}$	LE	$\overline{INIT}$	$\overline{DIAG}$	MD63–MD0	CB7–CB0	SNY0–SNY7	ERROR FLAGS
write	check bit generation	L	L	input	H	H	H	H	output	output	Z	H
write	memory initialization	L	L	x	H	H	L	H	L	output	Z	H

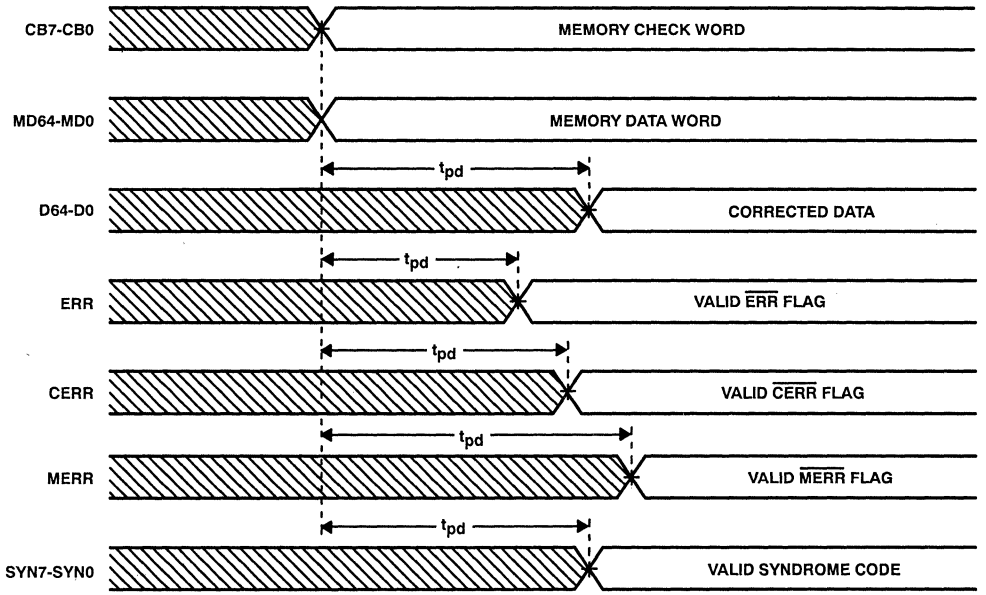


Figure 3. Timing Diagram for Correction Cycle

Table 4. Correction Cycle

MEMORY CYCLE	EDAC FUNCTION	DIR	$\overline{G}$	D63–D0	$\overline{OEBX}$	LE	$\overline{INIT}$	$\overline{DIAG}$	MD63–MD0	CB7–CB0	SNY0–SNY7	ERROR FLAGS
read	correction cycle	H	L	output	L	X	X	H	input	input	output	active

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

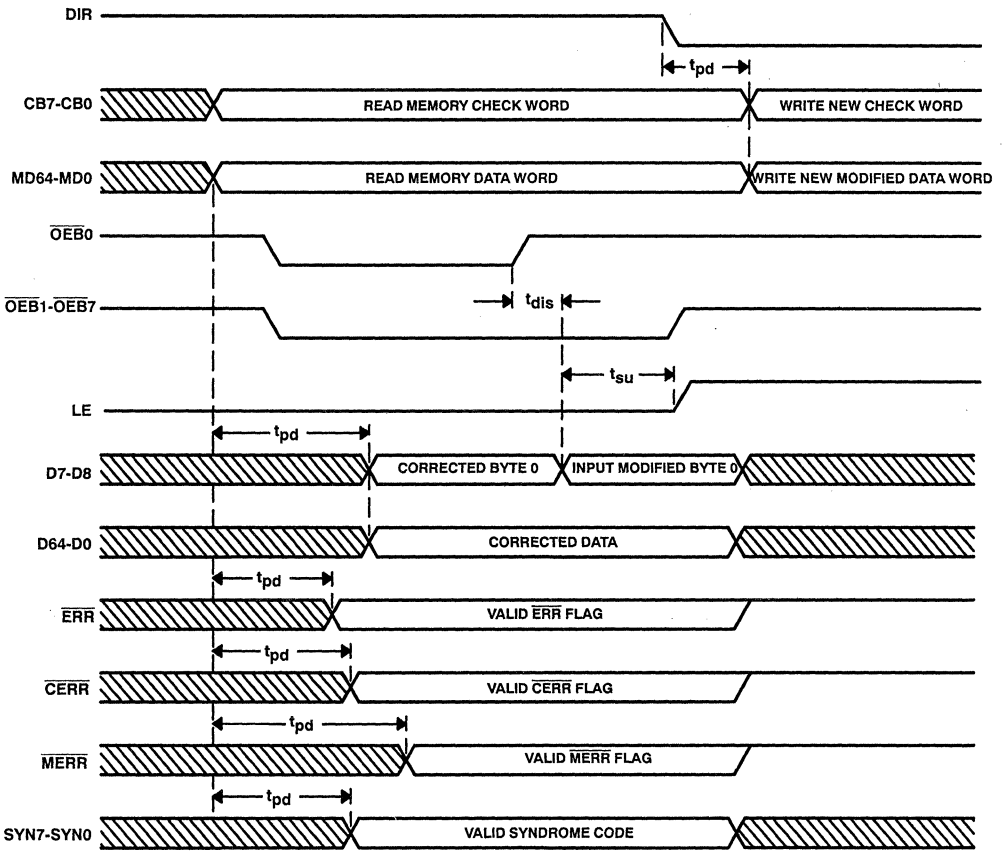


Figure 4. Timing Diagrams for Read Modify Write Cycle (Byte 0)

THERMAL INFORMATION

Table 5. Thermal Resistance and Junction Temperature vs Air Flow

Transverse air flow (m/min)		30	60	90	120	150	180	210	240	270	300
	(linear ft/min)	100	200	300	400	500	600	700	800	900	1000
$R_{\theta JA}$	Junction-to-ambient thermal resistance (°C/W)	8.7	6.8	5.1	4.8	4.5	4.2	3.9	3.7	3.5	3.4
T_J	Virtual junction temperature (°C) (for T_A = 55°C, P = 6 W)	107	96	86	84	82	80	78	77	76	75

APPLICATION INFORMATION

An EDAC is used to help solve the hard and soft errors that are associated with large DRAM memories. A hard error is a physical failure of the actual device. This type of error causes the memory location to be stuck high or low. A soft error is a random memory change caused by alpha particle radiation. This type of error is not permanent and is corrected by writing new data into the memory location. As memory size increases, so does the probability of a system encountering one of these types of failures.

An EDAC is typically implemented into a computer system in either of one of two modes, Correct-Only-on-Error or Correct-Always. In the Correct-Only-on-Error mode, the EDAC first checks for the existence of an error and, if present, the system is halted temporarily while the EDAC corrects the Error. This type of implementation places a premium on error detection time. The theory behind this type of architecture is that soft errors occur relatively infrequently, so a performance penality is paid only during error cycles. However, if the memory failure is a hard error, a correction cycle will always take place.

In the Correct-Always mode, an EDAC performs a correction cycle on every memory access, regardless if an error has occurred. If an error has not occurred, data is simply passed through the EDAC unaltered. This type of implementation places a premium on error correction time. Systems that are striving for maximum performance will generally not use the Correct-Always method. Previous generation EDACs, which utilize common I/O ports, normally have correction times that force wait states on the microprocessor. A large percentage of the correction time in an EDAC having a common I/O port is attributed to turning the bus around from an input to an output. A system designer is seldom able to achieve the level of performance specified by the semiconductor manufacture when using these types EDACs because, in actual usage, it is very difficult to duplicate the precise timing that is required to achieve maximum performance. The flow-thru EDAC architecture used on the 'AS6364 eliminates the need to turn the bus around during correction cycles. This dramatically improves performance at both the device and system level.

One drawback of the Correct-Only-on-Error architecture is that it is harder to implement into a system as compared to the Correct-Always method. In the Correct-Only-on-Error mode, intelligence must be built into the bus controller, based on the status of the EDAC's error flag. When using the Correct-Always architecture, the bus control logic is simplified. In high-performance systems, most designers will choose the Correct-Only-on-Error method because it impacts system performance the least. In systems where DRAM access performance is less of a concern, the Correct-Always architecture is easier to implement.

flow-thru advantage

Because the 'AS6364 can be used in either the Correct-Only-on-Error mode or the Correct-Always mode, its flow-thru architecture does not change the system implementation options as used on previous generation EDACs. However, due to the flow-thru architecture, the 'AS6364 offers higher performance and is easier to implement regardless of the system architecture chosen.

APPLICATION INFORMATION

Figure 5 shows how the 'AS6364 can be implemented into a system using the Correct-Always method. In this configuration, the direction control pin on the 'AS6364 is easily driven by the microprocessor's R/$\overline{W}$ signal or the bus control logic. Since the 'AS6364 also performs the bus interface function, the speed penality for error correction has been greatly reduced.

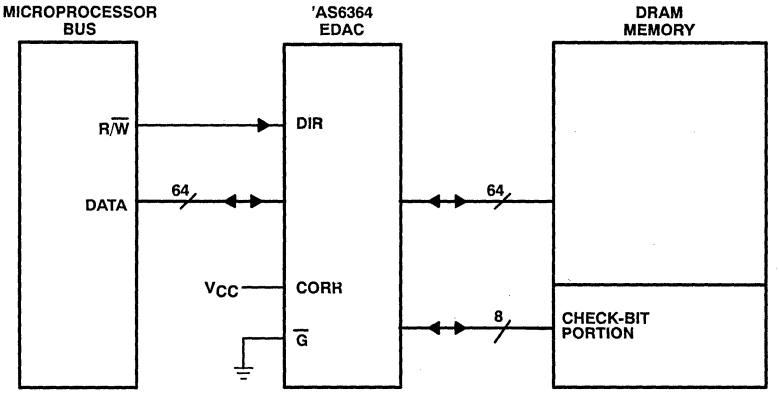


Figure 5. Correct-Always Mode

Figure 6 shows one way in which the 'AS6364 can be implemented into a system using the Correct-Only-on-Error architecture. In this mode of operation, the Correct input pin (CORR) is normally held inactive (low) by the bus control logic, disabling error correction. This has the effect of turning the 'AS6364 into a 64-bit-wide, TTL-style bus transceiver with input latches. The system benefits of this architecture are faster memory access times as compared to the Correct-Always method.

The bus control logic monitors the error flag ($\overline{ERR}$) during every memory read cycle. If an error is detected, the bus control logic is responsible for inserting wait states or halting the processor until corrected data can be generated. Corrected data is easily generated on the 'AS6364 by taking the CORR input active (high).

memory scrubbing

Memory scrubbing is a technique whereby a correction cycle is performed every refresh cycle. The most common type of refresh cycle is the distributed refresh. In this method, one row of memory is refreshed approximately every 15.6 μs.

The premise behind memory scrubbing is that since a refresh cycle has to be performed periodically, why not also perform a correction cycle? This technique typically scrubs out any soft errors before the actual data is needed. In addition, memory scrubbing reduces the risk of soft errors accumulating over time. This situation can occur when normal memory accesses are not occuring on a regular basis. In this method, the system is idle, but is not powered down. In some systems, memory scrubbing is the only form of error detection and correction used.

Memory scrubbing places a premium on error-correction time because the length of each refresh cycle is influenced by the error-correction time. This fact makes the 'AS6364 ideal in memory-scrubbing applications. Figure 7 shows how the 'AS6364 can be implemented into a system using memory scrubbing. In addition, the 'ALS6301 dynamic memory controller supports the memory-scrubbing feature. Please refer to those data sheets for additional details.

APPLICATION INFORMATION

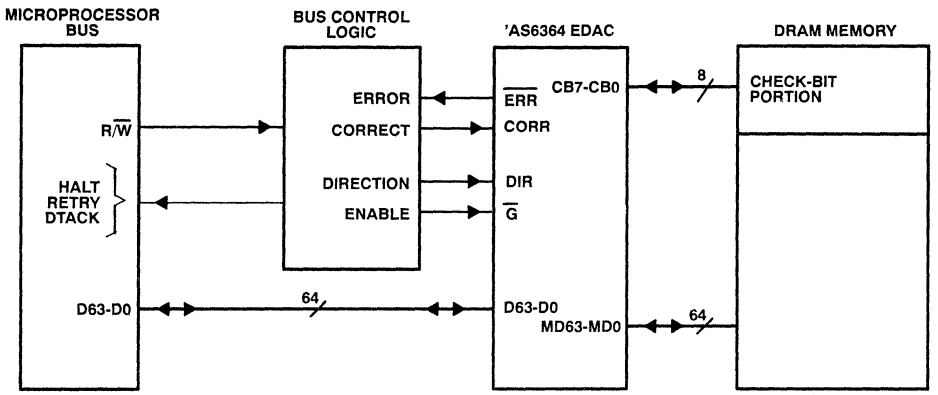


Figure 6. Correct-Only-On-Error Mode

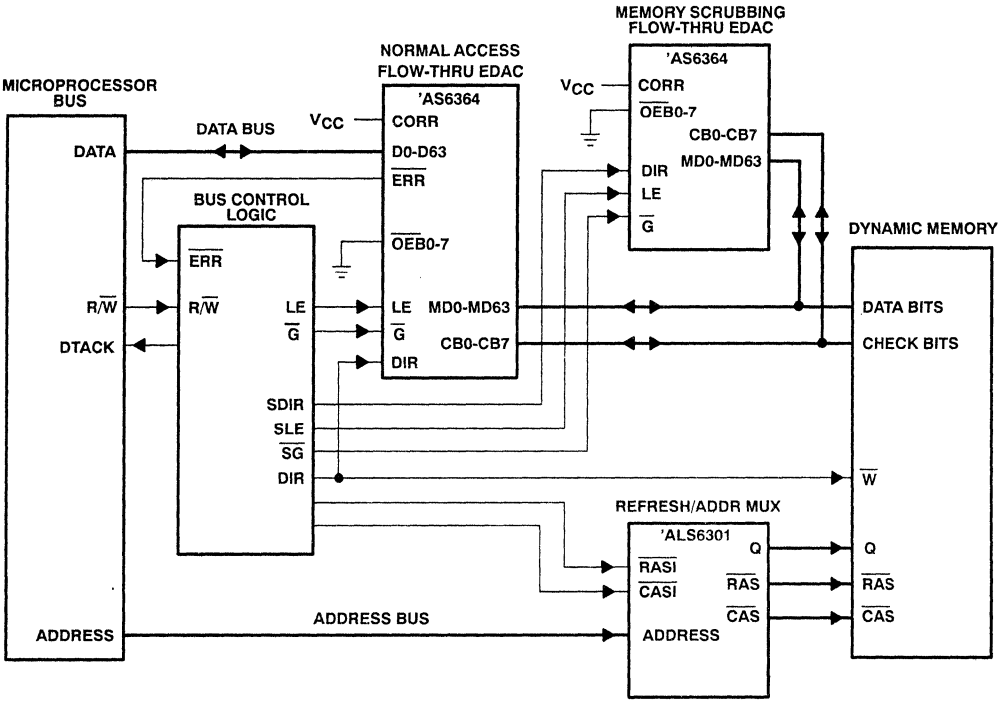


Figure 7. Correct-Always Mode with Memory Scrubbing

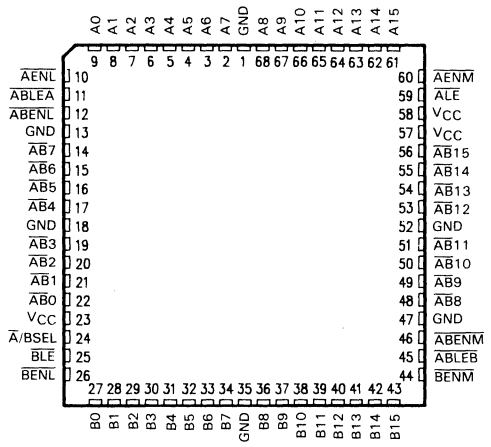
ADVANCE INFORMATION

Contents

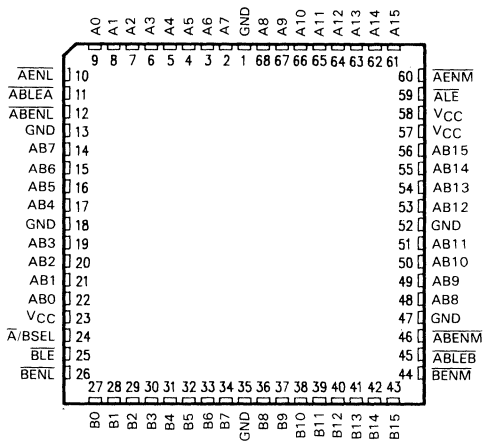
D3305, JULY 1989 · REVISED OCTOBER 1989

- **Multiplexed Real-Time and Latched Data**
- **Byte Control for Byte-Write Applications**
- **Useful in NuBus™ Interface Applications**
- **Useful in Memory Interleave Applications**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas Instruments Quality and Reliability**

SN74BCT2423 . . . FN PACKAGE
(TOP VIEW)



SN74BCT2424 . . . FN PACKAGE
(TOP VIEW)



description

The 'BCT2423 and 'BCT2424 are general-purpose 16-bit bidirectional transceivers with data storage latches and byte control circuitry arranged for use in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor- or bus-interface applications. These devices are also useful in memory-interleaving applications. The 'BCT2423 and 'BCT2424 offer inverted and noninverted data paths, respectively.

The 'BCT2423 and 'BCT2424 were designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics, but also greatly reduces the standby power of the device when disabled. This is valuable when the device is not performing an address or data transfer.

Three 16-bit I/O ports, A15-A0, B15-B0, and AB15-AB0 are available for address and/or data transfer. The $\overline{\text{AENM}}$, $\overline{\text{AENL}}$, $\overline{\text{BENM}}$, $\overline{\text{BENL}}$, $\overline{\text{ABENM}}$, and $\overline{\text{ABENL}}$ inputs control the bus transceiver functions. These control signals also allow byte-control of the most significant byte and least significant byte for each bus.

Address and/or data information can be stored using the internal storage latches. The $\overline{\text{ALE}}$, $\overline{\text{BLE}}$, $\overline{\text{ABLEA}}$, and $\overline{\text{ABLEB}}$ inputs are active low, and are used to control data storage. When the latch enable input is low, the latch is transparent. When the latch enable input goes high, the data present at the inputs is latched, and remains latched until the latch enable input is returned low.

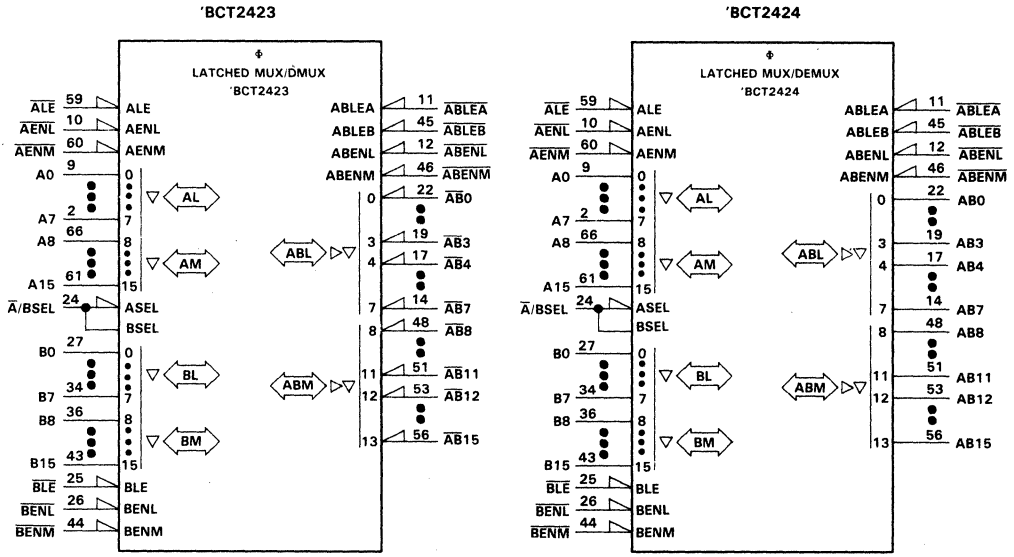
NuBus is a trademark of Texas Instruments Incorporated.

description (continued)

Data on the 'A' bus and 'B' bus are multiplexed onto the 'AB' bus via the $\overline{A}$/BSEL control line. When $\overline{A}$/BSEL is low, A15-A0 is mapped to the AB15-AB0 outputs. When $\overline{A}$/BSEL is high, B15-B0 is mapped to the AB15-AB0 outputs.

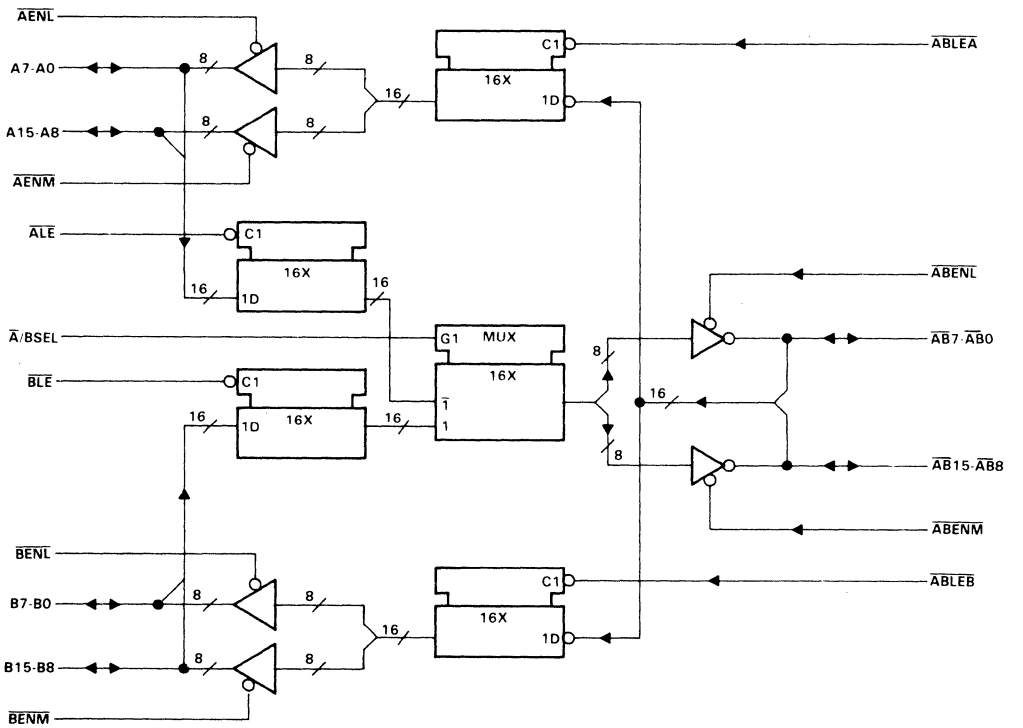
The SN74BCT2423 and SN74BCT2424 are characterized for operation from 0°C to 70°C.

logic symbols†

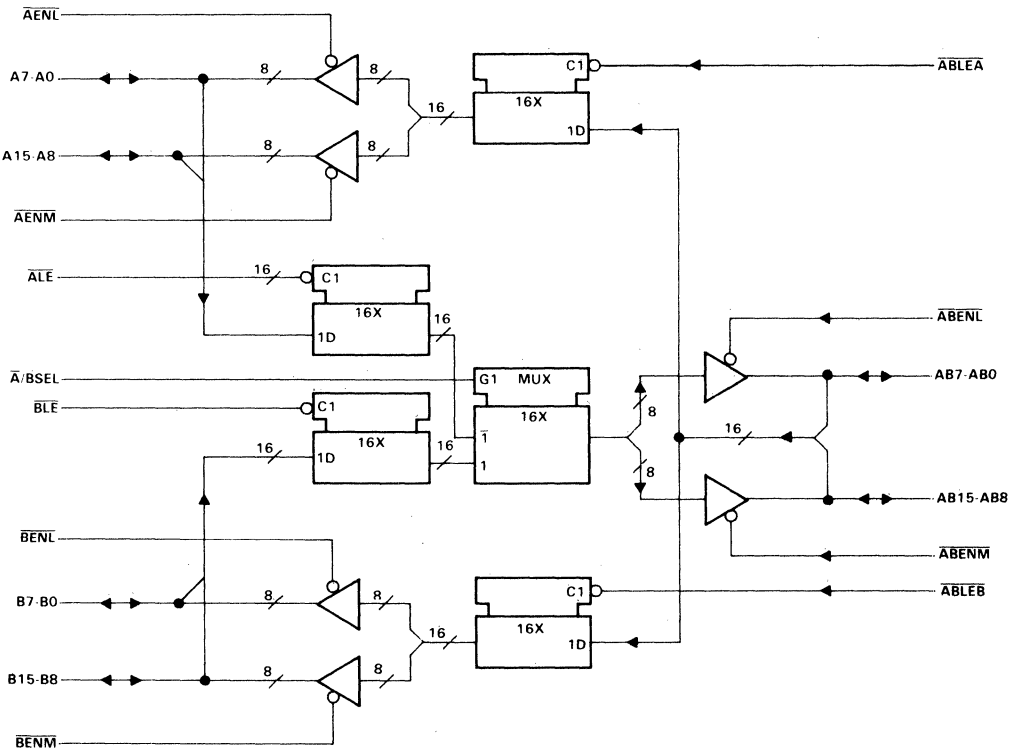


†These logic symbols are in accordance with ANSI/IEEE Std 91-1984.

logic diagram (positive logic)



logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TERMINAL FUNCTIONS

PIN NAME	DESCRIPTION
A15-A0	A Bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the A bus and the AB bus is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{AB}15$-$\overline{AB}0$ ('BCT2423) AB15-AB0 ('BCT2424)	AB Bus. This 16-bit I/O port allows for multiplexed transmission of data and/or address information to or from the A and B buses. Information transfer between the A, B and AB buses is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{ABENL}$	AB Bus Output Enable, Least Significant Byte. This active-low input is used to enable the AB7-AB0 outputs. When this input is high, the AB7-AB0 outputs are in the high-impedance state allowing for data input.
$\overline{ABENM}$	AB Bus Output Enable, Most Significant Byte. This active-low input is used to enable the AB15-AB8 outputs. When this input is high, the AB15-AB8 outputs are in the high-impedance state allowing for data input.
$\overline{ABLEA}$	AB Bus Latch Enable to A Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15-AB0) to be transferred to the A bus (A15-A0). When $\overline{ABLEA}$ is low, the latch is transparent. When $\overline{ABLEA}$ transitions to the high level, the data present at the AB15-AB0 inputs is latched, and remains latched while $\overline{ABLEA}$ is high.
$\overline{ABLEB}$	AB Bus Latch Enable to B Bus. This active-low input is used to control the latch that holds data received from the AB bus (AB15-AB0) to be transferred to the B bus (B15-B0). When $\overline{ABLEB}$ is low, the latch is transparent. When $\overline{ABLEB}$ transitions to the high level, the data present at the AB15-AB0 inputs is latched, and remains latched while $\overline{ABLEB}$ is high.
$\overline{A}$/BSEL	A/B Select Control. This input controls the A/B multiplexer. When the input is low, A15-A0 is selected as input to the AB15-AB0 outputs. When the input is high, B15-B0 is selected as input to the AB15-AB0 outputs.
$\overline{AENL}$	A Bus Output Enable, Least Significant Byte. This active-low input is used to enable the A7-A0 outputs. When this input is high, the A7-A0 outputs are in the high-impedance state allowing for data input.
$\overline{AENM}$	A Bus Output Enable, Most Significant Byte. This active-low input is used to enable the A15-A8 outputs. When this input is high, the A15-A8 outputs are in the high-impedance state allowing for data input.
$\overline{ALE}$	A Bus Latch Enable. This active-low input is used to control the latch that holds data received from the A bus (A15-A0). When $\overline{ALE}$ is low, the latch is transparent. When $\overline{ALE}$ transitions to the high level, the data present at the A15-A0 inputs is latched and remains latched while $\overline{ALE}$ is high.
B15-B0	B Bus. This 16-bit I/O port allows for transmission of data and/or address information to or from the AB bus. Information transfer between the B bus and the AB bus is inverting for the 'BCT2423 and noninverting for the 'BCT2424.
$\overline{BENL}$	B Bus Output Enable, Least Significant Byte. This active-low input is used to enable the B7-B0 outputs. When this input is high, B7-B0 outputs are in the high-impedance state allowing for data input.
$\overline{BENM}$	B Bus Output Enable, Most Significant Byte. This active-low input is used to enable the B15-B8 outputs. When this input is high, the B15-B8 outputs are in the high-impedance state allowing for data input.
$\overline{BLE}$	B Bus Latch Enable. This active-low input is used to control the latch that holds data received from the B bus (B15-B0). When $\overline{BLE}$ is low, the latch is transparent. When $\overline{BLE}$ transitions to the high level, the data present at the B15-B0 inputs is latched and remains latched while $\overline{BLE}$ is high.

FUNCTION TABLES

DIRECTION A OR B TO AB										
INPUTS							OUTPUTS			
							'BCT2423		'BCT2424	
Ax	Bx	$\overline{ALE}$	$\overline{BLE}$	A/$\overline{BSEL}$	$\overline{ABENM}$	$\overline{ABENL}$	$\overline{AB}$15-8	$\overline{AB}$7-0	AB15-8	AB7-0
H	X	L	X	L	L	L	L		H	
L	X	L	X	L	L	L	H		L	
X	X	H	X	L	L	L	$\overline{AB}_0$		AB_0	
X	H	X	L	H	L	L	L		H	
X	L	X	L	H	L	L	H		L	
X	X	X	H	H	L	L	$\overline{AB}_0$		AB_0	
X	X	X	X	X	L	L	Active	Active	Active	Active
X	X	X	X	X	L	H	Active	Z	Active	Z
X	X	X	X	X	H	L	Z	Active	Z	Active
X	X	X	X	X	H	H	Z	Z	Z	Z

DIRECTION AB TO A OR B								
INPUTS					OUTPUTS			
					'BCT2423		'BCT2424	
$\overline{ABx}$ ABx	$\overline{ABLEA}$	$\overline{ABLEB}$	$\overline{AENL}$† $\overline{AENM}$†	$\overline{BENL}$† $\overline{BENM}$†	Ax	Bx	Ax	Bx
H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	H	L	L
H	L	H	L	L	L	B_0	H	B_0
L	L	H	L	L	H	B_0	L	B_0
H	H	L	L	L	A_0	L	A_0	H
L	H	L	L	L	A_0	H	A_0	L
X	H	H	L	L	A_0	B_0	A_0	B_0
X	X	X	L	L	Active	Active	Active	Active
X	X	X	L	H	Active	Z	Active	Z
X	X	X	H	L	Z	Active	Z	Active
X	X	X	H	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedence,
A_0, B_0, AB_0, $\overline{AB}_0$ = no change since the controlling latch enable went high
†The least significant bytes (A7-A0 and B7-B0) and the most significant bytes (A15-A8 and B15-B8) can be independently enabled and disabled, as was illustrated for the $\overline{AB}$ and AB bytes in the upper function table.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (all inputs and I/O ports) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			SN74BCT2423			SN74BCT2424			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Ax, Bx outputs			−15			−15	mA
		$\overline{ABx}$ or ABx outputs			−15			−15	
I_{OL}	Low-level output current	Ax, Bx outputs			24			24	mA
		$\overline{ABx}$ or ABx outputs			48			48	
t_w	Pulse duration	$\overline{ABLEA}$, $\overline{ABLEB}$ high or low	12.5			12.5			ns
		$\overline{ALE}$, $\overline{BLE}$ high or low	12.5			12.5			
t_{su}	Setup time	Data before $\overline{xLEx}$ ↑	10			10			ns
t_h	Hold time	Data after $\overline{xLEx}$ ↑	2			2			ns
T_A	Operating free-air temperature		0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	SN74BCT2423			SN74BCT2424			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V, I_{OH} = −400 μA	V_{CC}−1.5			V_{CC}−1.5			V
		V_{CC} = 4.5 V, I_{OH} = −3 mA	2.8	3.6		2.8	3.6		
		V_{CC} = 4.5 V, I_{OH} = −15 mA	2			2			
V_{OL}	Ax, Bx outputs	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA		0.35	0.5		0.35	0.5	
	ABx, $\overline{ABx}$ outputs	V_{CC} = 4.5 V, I_{OL} = 24 mA		0.25	0.4		0.25	0.4	
		V_{CC} = 4.5 V, I_{OL} = 48 mA		0.35	0.5		0.35	0.5	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V			100			100	μA
I_{IH}§		V_{CC} = 5.5 V, V_I = 2.7 V	−100		20	−100		20	μA
I_{IL}§		V_{CC} = 5.5 V, V_I = 0.4 V			−200			−200	μA
I_O¶		V_{CC} = 5.5 V, V_O = 0 V	−60		−225	−60		−225	mA
I_{CC}	Enabled	V_{CC} = 5.5 V, V_{IL} = 0.5 V,			190			190	mA
	Disabled	V_{IH} = 3 V, Outputs open			50			50	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameter I_{IH} and I_{IL} include the offstate output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

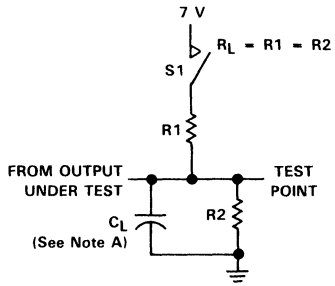
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS†	SN74BCT2423			SN74BCT2424			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	$\overline{AB}$x, ABx	Ax	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_1 = 500 Ω, R_2 = 500 Ω, T_A = MIN to MAX		10	18		10	18	ns
t_{pd}	$\overline{AB}$x, ABx	Bx			10	18		10	18	ns
t_{pd}	Ax	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	Bx	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{ALE}$ ↓	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{BLE}$, ↓	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{pd}	$\overline{ABLEA}$ ↓	Ax			10	18		10	18	ns
t_{pd}	$\overline{ABLEB}$ ↓	Bx			10	18		10	18	ns
t_{pd}	ABSEL	$\overline{AB}$x, ABx			10	18		8	15	ns
t_{en}	$\overline{AENM}$, $\overline{AENL}$	Ax			10	18		10	18	ns
t_{en}	$\overline{BENM}$, $\overline{BENL}$	Bx			10	18		10	18	ns
t_{en}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{AB}$x, ABx			10	18		10	18	ns
t_{dis}	$\overline{AENM}$, $\overline{AENL}$	Ax			5	10		5	10	ns
t_{dis}	$\overline{BENM}$, $\overline{BENL}$	Bx			5	10		5	10	ns
t_{dis}	$\overline{ABENM}$, $\overline{ABENL}$	$\overline{AB}$x, ABx			5	10		5	10	ns

†See Parameter Measurement Information for load circuits and voltage waveforms.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

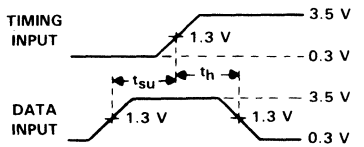
PARAMETER MEASUREMENT INFORMATION

SWITCH POSITION TABLE

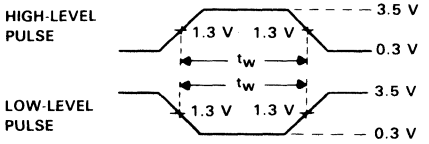
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



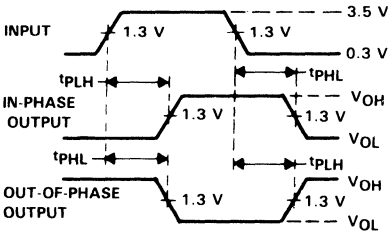
LOAD CIRCUIT



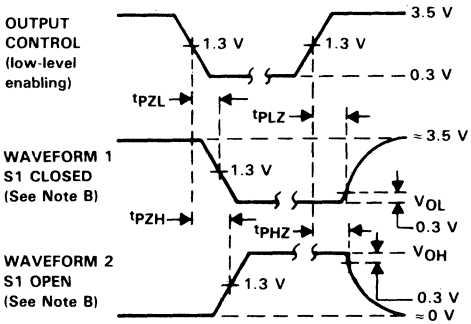
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

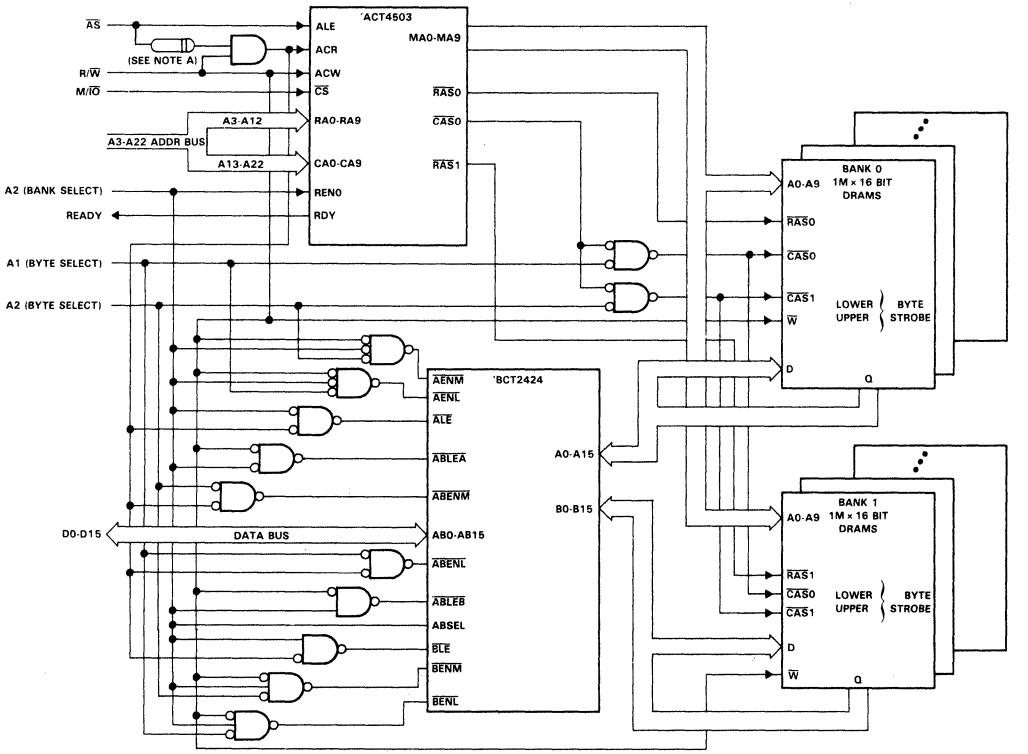


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1

APPLICATION INFORMATION



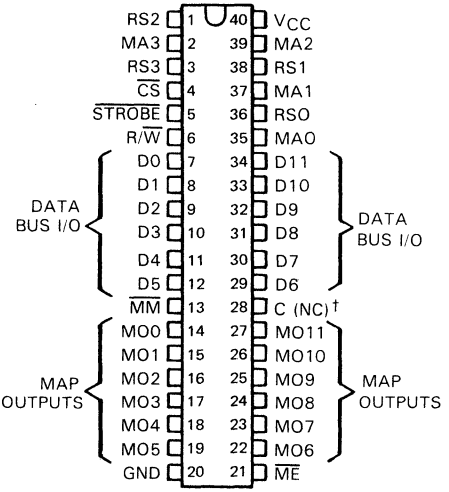
NOTE A: The value of this delay element is dependent on the speed of the microprocessor.

FIGURE 2. TYPICAL MEMORY INTERLEAVE APPLICATION

D2549, JANUARY 1981—REVISED APRIL 1990

- **Expands 4 Address Lines to 12 Address Lines**
- **Designed for Paged Memory Mapping**
- **Output Latches Provided on 'LS610**
- **3-State Map Outputs**
- **Compatible with TMS9900 and Other Microprocessors**

JD OR N PACKAGE
(TOP VIEW)



†This pin has no internal connection on the 'LS612.

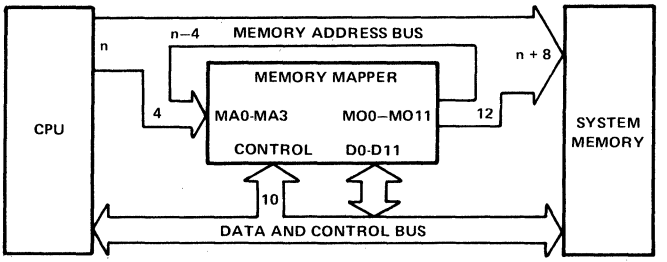
description

Each 'LS610 and 'LS612 memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. Each 'LS610 also contains 12 latches with an enable control.

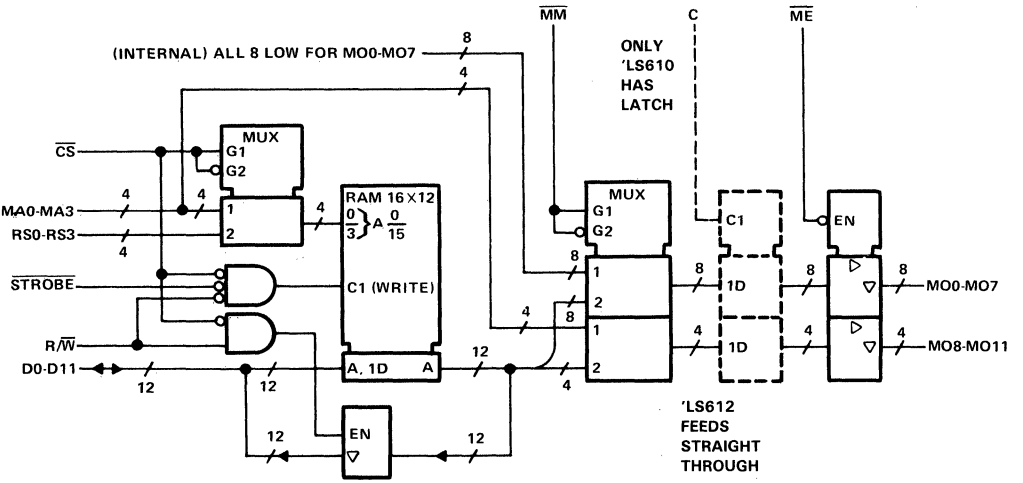
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see System Block Diagram) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus. This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation: read, write, map, and pass. Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 output stages are transparent in this mode, while the 'LS610 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at M08-M011, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.

system block diagram



logic diagram (positive logic)



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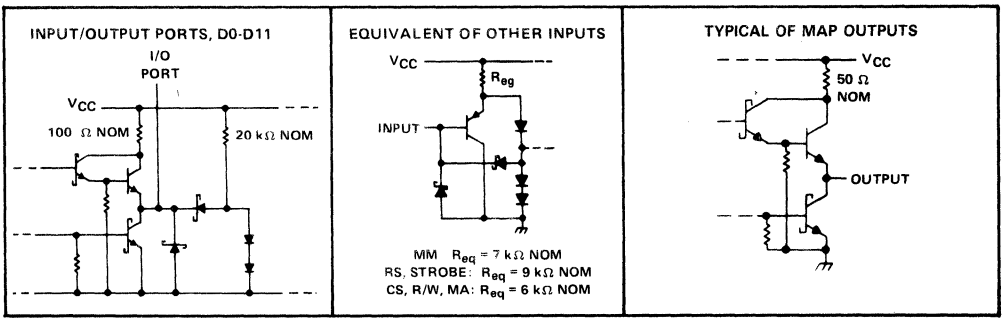
TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
C	28	Latch enable input for the 'LS610 (no internal connection for 'LS612). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
$\overline{CS}$	4	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
D0 thru D11	7-12 29-34	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
MA0 thru MA3	35, 37, 39, 2	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
$\overline{ME}$	21	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
$\overline{MM}$	13	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
MO0 thru MO11	14-19, 22-27	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
RS0 thru RS3	36, 38, 1, 3	Register select inputs for I/O operations.
R/$\overline{W}$	6	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
$\overline{STROBE}$	5	Strobe input used to enter data into the selected map register during I/O operations.
V_{CC}, GND	40, 20	5-V power supply and network ground (substrate) pins

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: Data Bus I/O . . . . . 5.5 V
All other inputs . . . . . 7 V
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current		MO			−15	mA
			D			−2.6	
I_{OL}	Low-level output current		MO			24	mA
			D			8	
t_{AVCL}	Address setup time (AV before C low)	'LS610 only	See Figure 2	30			ns
t_{SLSH}	Duration of strobe input pulse		See Figure 1	75			ns
t_{CSLSL}	$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low)			20			ns
t_{WLSL}	R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low)			20			ns
t_{RVSL}	RS setup time (RS valid to strobe low)			20			ns
t_{DVSH}	Data setup time (D0-D11 valid to strobe high)			75			ns
t_{SHCSH}	$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high)			20			ns
t_{SHWH}	R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high)			20			ns
t_{SHRX}	RS hold time (Strobe high to RS invalid)			20			ns
t_{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5	V
V_{OH}	MO	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OH} = −3 mA	2.4			V
				I_{OH} = MAX	2			
	D			I_{OH} = MAX	2.4			
V_{OL}	MO	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
	D			I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = MAX, V_{IL} = MAX,	V_{IH} = 2 V, V_O = 2.7 V				20	μA
I_{OZL}	MO	V_{CC} = MAX, V_{IL} = MAX,	V_{IH} = 2 V, V_O = 0.4 V				−20	μA
	D						−400	
I_I	D	V_{CC} = MAX		V_I = 5.5 V			0.1	mA
	All others			V_I = 7 V			0.1	
I_{IH}		V_{CC} = MAX, V_I = 2.7 V					20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V					−0.4	mA
I_{OS}§	MO	V_{CC} = MAX			−40		−225	mA
	D				−30		−130	
I_{CC}		V_{CC} = MAX	Outputs high			112	180	mA
			Outputs low			112	180	
			Outputs disabled			180	230	

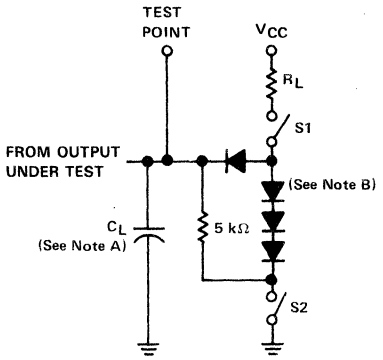
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D0-11	R_L = 2 kΩ, See Figure 1, See Notes 2 and 3		28	50		26	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D0-11			20	35		20	35	ns
t_{RVDV}	Access time	RS	D0-11			49	75		39	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D0-11			32	50		30	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D0-11			42	65		38	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO0-11	R_L = 667 Ω, See Figure 2, See Notes 2 and 3		19	30		17	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO0-11			56	85		48	85	ns
t_{MLQV}	Access time	$\overline{MM}$↓	MO0-11			25	40		22	40	ns
t_{CHQV}	Access time	C↑	MO0-11			24	40				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO0-11			46	70		39	70	ns
t_{MHQV}	Access time	$\overline{MM}$↑	MO0-11			24	40		22	40	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO8-11			19	30		13	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO0-11			14	25		14	25	ns

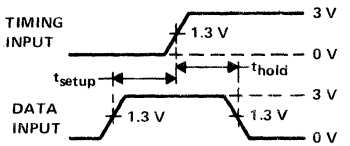
NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.
3. Load circuits and voltage waveforms are shown in Parameter Measurement Information.

PARAMETER MEASUREMENT INFORMATION

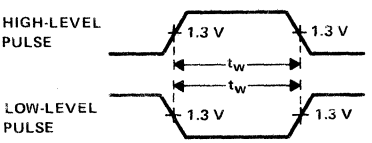


LOAD CIRCUIT FOR 3-STATE OUTPUTS

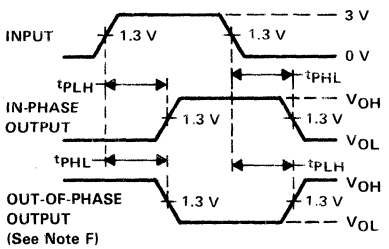
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.



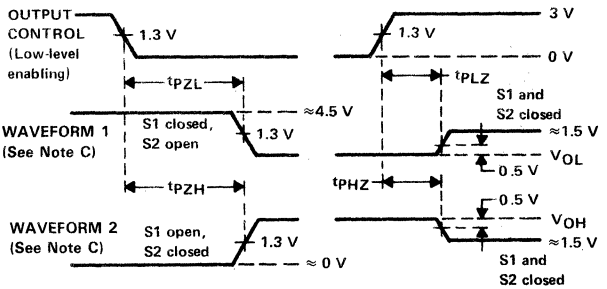
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

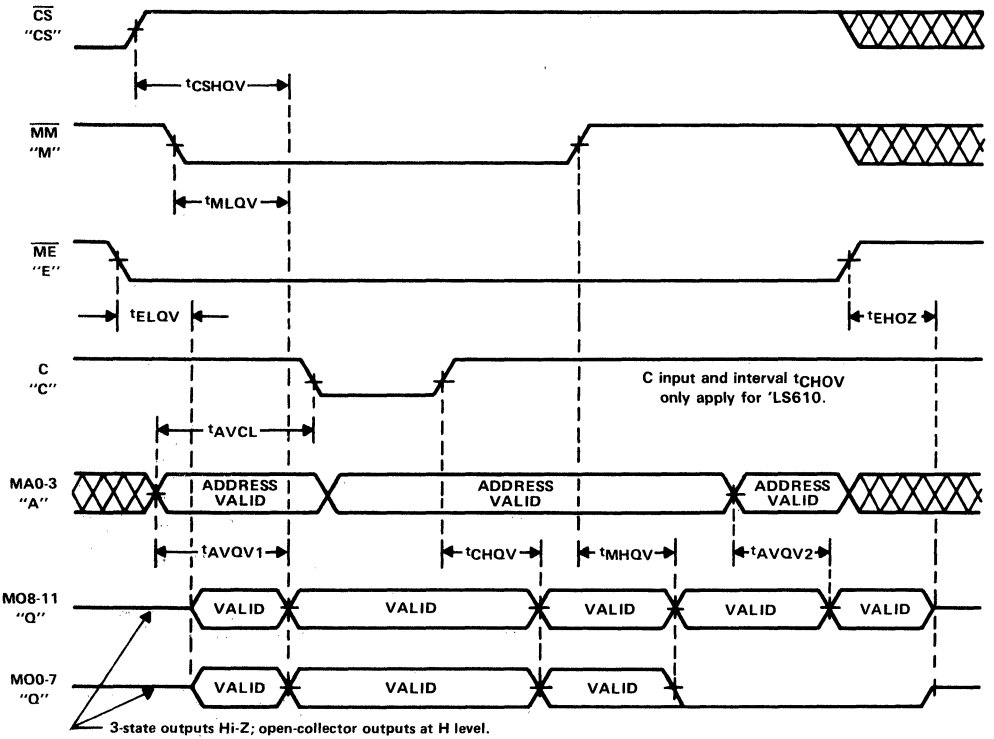


FIGURE 2. MAP AND PASS MODES

PARAMETER MEASUREMENT INFORMATION

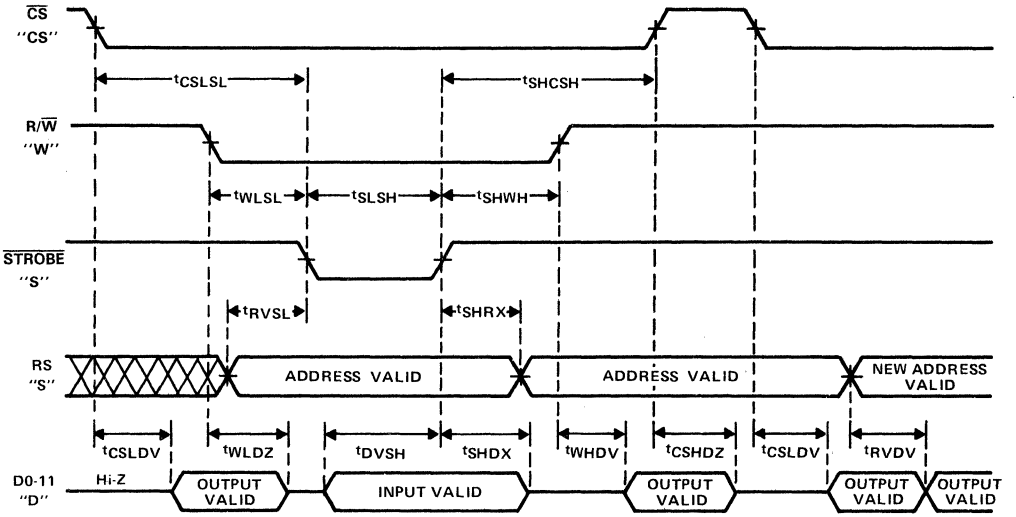


FIGURE 3. WRITE AND READ MODES

EXPLANATION OF LETTER SYMBOLS

This data sheet uses a new type of letter symbol based on JEDEC Standard 100 to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

- H = high or transition to high
- L = low or transition to low
- V = a valid steady-state level
- X = unknown, changing, or "don't care" level
- Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT	SIGNAL NAME	A AND C SUBSCRIPT
C	C	$\overline{ME}$	E
$\overline{CS}$	CS	$\overline{MM}$	M
D0—11	D	R/$\overline{W}$	W
MA0—MA3	A	RS0—RS3	R
MO0—MO11	Q	$\overline{STROBE}$	S

Contents

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Glossary of Cache Terms

TEXAS INSTRUMENTS

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Access Time
The time interval between the request for information and the instant this information is available.

Address
A number of bits used to identify memory locations in which data can be stored or from which it can be retrieved.

Bank
A bank is a memory used to store data or address information.

Block
(see Line)

Block Size
(see Line Size)

Buffered Writes
(see Posted Writes)

Bus Watcher
The bus watcher is a mechanism used to monitor or snoop system address buses to assure coherency in the data stored in cache and main memory.

Byte
A byte consists of eight bits.

Cache
A cache is a small, high-speed memory used to provide a temporary storage location for data most likely to be requested by the CPU. This allows for quick access of data and improved CPU performance (i.e., zero wait states).

Cache Address Comparator
A cache address comparator is a memory device used to store and compare addresses which map data that is stored in cache.

Cache Hit
A cache hit is said to occur when data being requested by the CPU resides in cache.

Cache Miss
A cache miss is said to occur when data being requested by the CPU does not reside in cache.

Cache Size

Cache size is defined by the number of bytes of data that can be stored in a cache memory. Cache size is one of the parameters that most strongly affects cache performance.

Cache Tag

(see Cache Address Comparator)

Cascade

In regards to cache memories, the term cascade refers to the use of several cache tags to expand the cache size (depth) and/or the main memory coverage (width).

Copy-Back Cache

This term describes a type of cache design in which memory writes initially only modify the cache and can later be copied back to main memory. Copy-back caches improve CPU read and write performance and decrease system bus traffic.

Data

Any information stored or retrieved from a memory device

Data Coherency

Data coherency is necessary when a system has multiple memories. If several memories contain the same data word, modifying that data word in one memory causes the data to be incoherent with the data stored in the other memories. Therefore, the other memories that have a copy of that same data word must either update or invalidate their copy. If this is not done, data remains inconsistent or incoherent.

Direct Mapped Cache

A direct mapped cache is the simplest form of set associative cache architecture, one way set associative. In a direct mapped cache, an index identifies only one line of data, (i.e., only one member of a set may exist in cache at a given time). (see Set Associativity)

Dirty Bit

A dirty bit is a status bit used in copy-back caches to identify data which has been modified and is different from that which is stored in main memory.

Flushed

A cache memory location that is written back into shared memory and then replaced is said to be flushed.

Hit
(see Cache Hit)

Hit Rate
(see Hit Ratio)

Hit Ratio
A measure of cache memory performance and is equal to the number of cache hits times 100%, divided by the number of memory accesses.

Index
The portion of the main memory address bits used to address a location in the cache tag RAM and a line of data in the cache data RAM. The index usually consists of the lower order address bits.

Line
A line is the fixed unit of information transfer between cache and main memory.

Line Size
Line size refers to the amount of information in a line and is defined as a number of bytes. Line size is one of the parameters that most strongly affects cache performance.

Match
(see Cache Hit)

Memory
A medium capable of storage and/or retrieval of information

Memory Thrashing
If a CPU requests a series of data, where each data word has the same index but resides in a different page in main memory, then a cache miss will occur for each memory access request. This condition is known as memory thrashing and seriously affects the efficiency of cache. The use of 2-way and 4-way set associative caches can reduce or eliminate the possibility of memory thrashing.

Miss
(see Cache Miss)

Multiplexing
The ability to transmit two or more signals over a single channel. Often done when transferring data from a large bus into a cache.

Posted Writes

In a write-through cache, read cycles are accelerated but write cycles are not. Through the use of a write buffer, write cycles can also be accelerated. The process of buffering or storing address and data in a write buffer is referred to as a posted write or buffered write.

Replacement Algorithm

The method used to determine when and where to write data into a cache memory. Two common replacement algorithms are LRU (Least Recently Used) and Random.

Set

A set is made up of all the locations in main memory corresponding to a given index.

Set Associativity

This term describes a mapping technique used in cache design. This technique allows data from anywhere in main memory to be stored in a much smaller cache memory. This is accomplished by defining sets of data in main memory. Each set of data is associated with an indexed memory location in cache.

Snoop

(see Bus Watcher)

Snooping

(see Bus Watcher)

Store-Through

(see Write-Through)

Tag

The portion of the main memory address bits that is stored (along with data) in the cache memory. The tag is stored in the cache tag RAM at the location addressed by the index. The tag usually consists of the high-order address bits. The tag is compared to the CPU's high-order address bits during a memory access cycle to determine a cache hit or miss.

Thrashing

(see Memory Thrashing)

Wait States

The term wait state refers to the clock periods where the processor is stopped to wait for the memory to respond. Cache memories are commonly used to eliminate wait states so that the processor can operate at maximum speed.

Word
A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write-Back
(see Copy-Back)

Write Buffer
Memory devices used for temporary storage of address and data during a CPU write cycle. A write buffer usually consists of latches or FIFOs. Write buffers are commonly used in write through cache design and improve CPU performance by as much as 5%.

Write-Through Caches
This term describes a type of cache design in which the memory read cycle is accelerated (the write cycle is not accelerated). With a write-through cache, every time data is written into the cache, it is also written into main memory.

2-Way Set Associative
In a 2-way set associative cache, an index identifies two lines of data (i.e., only two members of a set may exist in cache at a given time). This design provides significant performance improvement in comparison to direct mapped caches as measured by the hit ratio. (see Set Associativity).

4-Way Set Associative
In a 4-way set associative cache, an index identifies four lines of data (i.e., only four members of a set may exist in cache at a given time). This design provides significant performance improvement in comparison to direct mapped or 2-way set associative caches as measured by the hit ratio. (see Set Associativity).

Cache Memory Systems

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Contents

List of Illustrations

Introduction

As the typical operating speeds of processors have increased to provide for the ever increasing need for computing power, the necessity of developing a memory hierarchy (the incorporation of two or more memory technologies in the same system) has become apparent. One of these memory technologies is selected on the basis of fast access time (with associated high cost per bit) to allow minimum system cycle time. The other technologies are chosen with the lowest possible cost per bit relative to speed in order to achieve the maximum system memory capacity. In a system with a multiple level hierarchy, the speed-to-cost relationship depends upon the frequency of access and the total memory requirement at that level. By proper use of this hierarchy through coordination of hardware, system software, and in some cases user software, the overall memory system will reflect the characteristics that approximate the fast access time of the fast memory technology and the low cost per bit of the low cost memory technology. Large computer systems have made use of this memory optimization technique to maintain very large data bases and high throughput (see Figure 1). Many smaller processor systems use this technique to allow mass storage of data, where a tape or a disk is the low-cost memory and Random Access Memory (RAM) is the fast memory technology.

Because of the increase in processor speeds, memory hierarchy is now extending to the RAM memory used in microcomputer systems. Typically, Dynamic RAM (DRAM) is used as the bulk or main memory and High-Speed Static RAM (HSS) serves as the fast-access memory. This HSS RAM is typically 1K to 256K words deep and serves as a fast buffer memory between the processor and the main memory. This small fast buffer memory is called "cache" memory because it is the storage location for a carefully selected portion of the data from the main memory. The addresses for that portion of memory currently in the buffer memory is saved in the cache tag RAM (a small memory that is used to store the addresses of the data that has been mapped to cache).

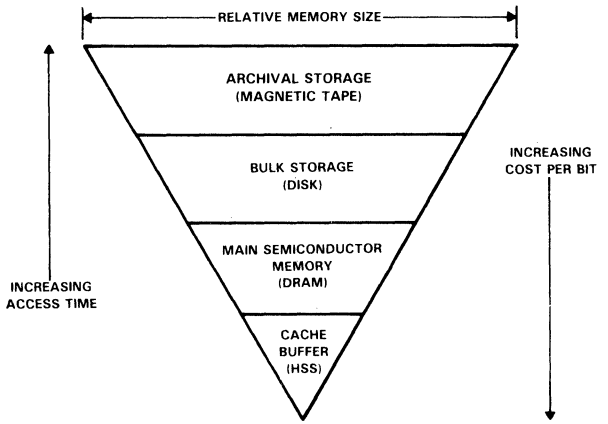


Figure 1. Memory Size vs Access Time and Cost per Bit

Memory Systems with Cache

When the processor accesses main memory, the processor address is compared to the addresses currently present in the cache tag RAM. When a match occurs, the required data is resident in the cache and the access is called a "hit" and is completed in the cycle time of the fast memory. When a match does not occur (a "miss"), the main memory is accessed and the processor must be delayed to allow for the slower access cycle of the main memory. Whether a hit has occurred is determined by the cache-tag RAM. Figure 2 shows the relative placement of the processor, main memory, cache, and cache-tag RAM within a system.

Since there must be comparisons made between the current processor address and the addresses in the cache, the cache-tag RAM must have a very fast access time to prevent the degradation of processor accesses even when a match occurs. Previously, the memory used for the cache-tag RAM was the same as that used for the cache, which (because of added delays through comparison logic) meant that the full benefits of the cache were not realized.

The Cache Address Comparators were designed to reduce this cache access degradation to a minimum by incorporating the matching logic on-chip. This provides match-recognition times that are compatible to the access time of the cache-buffer memory.

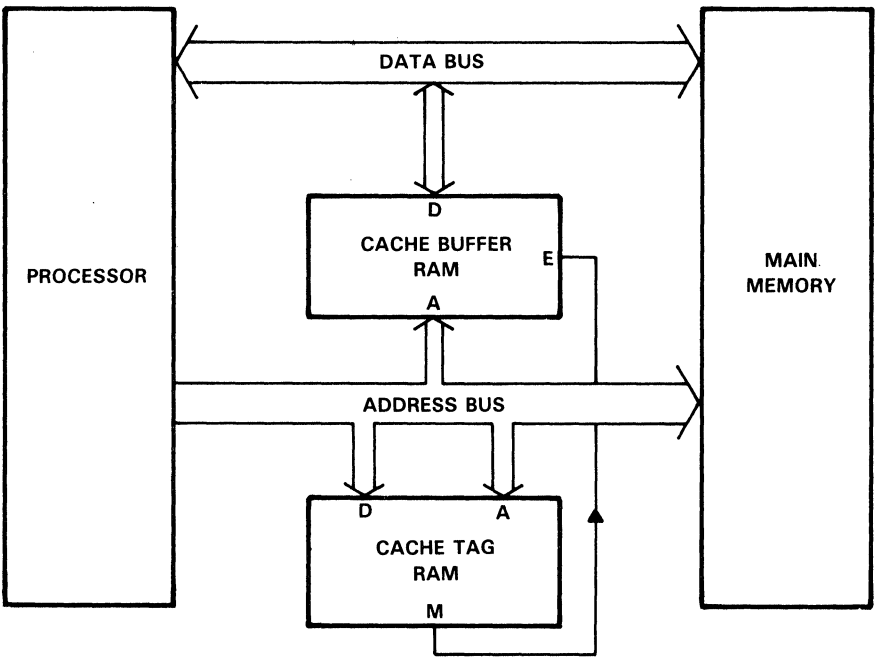
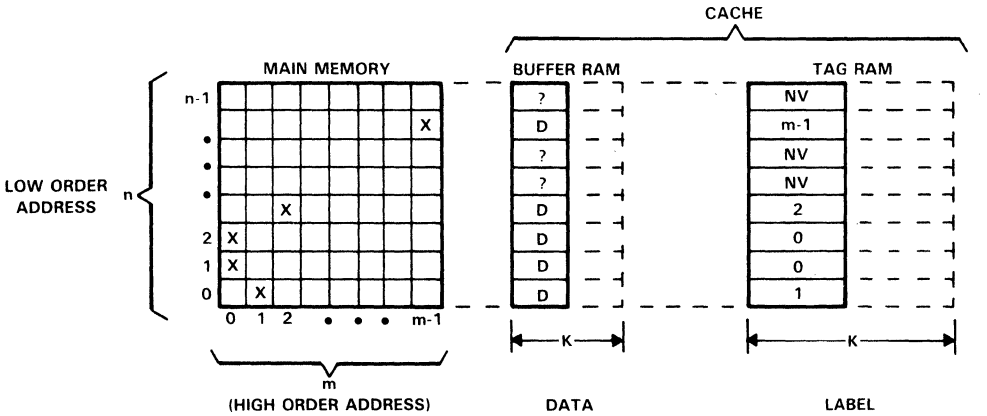


Figure 2. Typical Memory System with Cache

Set-Associative Cache Address Matching

The 'ACT2151 and 'ACT2152 implement the set-associative type of cache address matching. This algorithm may be more clearly understood by considering main memory as an (m) by (n) array of blocks and the cache is an (n) by (k) array (see Figure 3). Each block is composed of (x) words, and transfers between main memory and cache memory always move all (x) words in that block. Corresponding to every block in the buffer RAM is a tag address specifying which block of main memory is currently resident in the buffer RAM at that location. The set-associative algorithm maps each modulo (n) group of (m) blocks into the corresponding (n) row of the cache. The low-order address lines of the processor covering the sets (n) select a row of the cache buffer and the corresponding row in the tag RAM. The data is stored in the cache buffer and the high-order address specifying the block (m) is saved in the tag RAM. The high-order address then becomes the tag.



K = Number of BUFFER/TAG groups for multiple cache systems
X = Blocks moved to cache
D = Valid data from main memory
? = Areas of cache that have not been loaded from main memory
NV = Code to indicate non-valid label
0, 1, 2, m-1 = Labels from high order address specifying the block moved from main memory.

Figure 3. Set-Associative Cache Address Matching

Cycle Time Improvement

There are several algorithms used to determine which areas of main memory should be resident in cache and which should be replaced (first-in, first-out; least recently used; or random). Since programs typically have the property of locality (over short periods of time, most accesses are to a small group of memory addresses), these replacement algorithms can make the cache have the majority of processor accesses resulting in hits. The hit ratio (number of hits × 100%/number of memory accesses) runs 90% and higher in systems with well coordinated memory to cache mapping routines. As the block size (x) increases, the replacement mapping algorithm options have greater impact on the cache performance. (The terms block and block size are also referred to as line and line size.)

When running at maximum frequency, many microprocessors are operating with memory access times of 100 ns or less. After allowing for address buffering, decoding, and propagation delays through data buffers, the maximum access time that can be tolerated is 60 ns or less before processor throughput is affected. For large memory systems, DRAM can be used to achieve a cost-effective memory.

However, these cannot meet a 60-ns access requirement. If the actual system throughput for a system with cache and one without cache are compared, the advantages of cache become obvious.

For comparison of the two architectures, assume that a processor is implemented in which 30% of the active cycle involve main memory (the other 70% used for instruction decoding and internal operations). Also assume that the processor cycles at 125 ns with a required memory access time of 60 ns. If the memory is not ready, the cycle time is extended by 125-ns increments till satisfied. This processor using 120-ns DRAMs would require one delay increment on main memory accesses and 200-ns DRAMs would require two delay increments. The average cycle time can be calculated for each memory speed as follows:

$$\text{Average Cycle Time} = [(\text{INT}) \times (\text{CYC})] + [(\text{MEM}) \times (\text{CYC} + \text{DEL})]$$

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns

For a processor using 120-ns DRAMs:

$$\text{Average Cycle Time} = [(70\%) \times (125 \text{ ns})] + [(30\%) \times (125 + 125)]$$
$$\text{Average Cycle Time} = 163 \text{ ns}$$

For a processor using 200-ns DRAMs:

$$\text{Average Cycle Time} = [(70\%) \times (125 \text{ ns})] + [(30\%) \times (125 + 250)]$$
$$\text{Average Cycle Time} = 200 \text{ ns}$$

For the same system with cache memory, assume a 90% hit ratio with 60-ns cache and 120-ns DRAM:

Average Cycle Time = [INT × CYC] + [MEM × [(HIT × CAC) + (MIS × (CYC + DEL))]]

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns
HIT = percent of memory accesses hit cache
MIS = percent of memory accesses miss cache
CAC = cache memory access cycle time

Average Cycle Time = [70% × 125] + [30% × [(90% × 125) + (10% × 125 + 125))]]
Average Cycle Time = 129 ns

This value represents a 20% improvement with 120-ns devices over the non-cache implementation with 120-ns devices and 35% using 200-ns devices. This performance improvement can be further demonstrated for those systems using custom or bit-slice processors where the memory cycle time as well as access time is of concern. For this example, consider a processor with a cycle time of 50 ns and main memory cycle time of 100 ns (use the same access ratios as in the previous example):

Average Cycle Time = [(70%) × (50)] + [(30%) × (100)] = 65 ns (Without Cache)

Average Cycle Time = [70% × 50] + [30% × [(90% × 50) + (10% × 100)]
(With Cache) = 52 ns

This represents a 20% decrease in average cycle time for the processor using 50-ns cache memory. If the main memory was rated at a cycle time of 200 ns, either using slow main memory or due to allocation of alternate cycles for some other activity (multiprocessors, direct memory access, display refresh, etc.), the cache would still give an average cycle time of 55 ns. This is an improvement of 63% over the 95 ns average cycle time for a non-cache system.

Cache Memory Configurations

Figures 4, 5, and 6 illustrate applications for the 'ACT2151 and the 'ACT2152 in cache memory systems. Figure 4 shows a cache-memory configuration that has a 512M-byte main memory with a block size of 4 32-bit words. In this particular application, a cache containing 1024 four-word blocks was chosen thus defining the main (n) × (m) array as being 1024 sets of 32,728 four word blocks. The 128M-word memory requires an address bus of 27 lines. The least bits (A2-A3) are used as a word select for one of

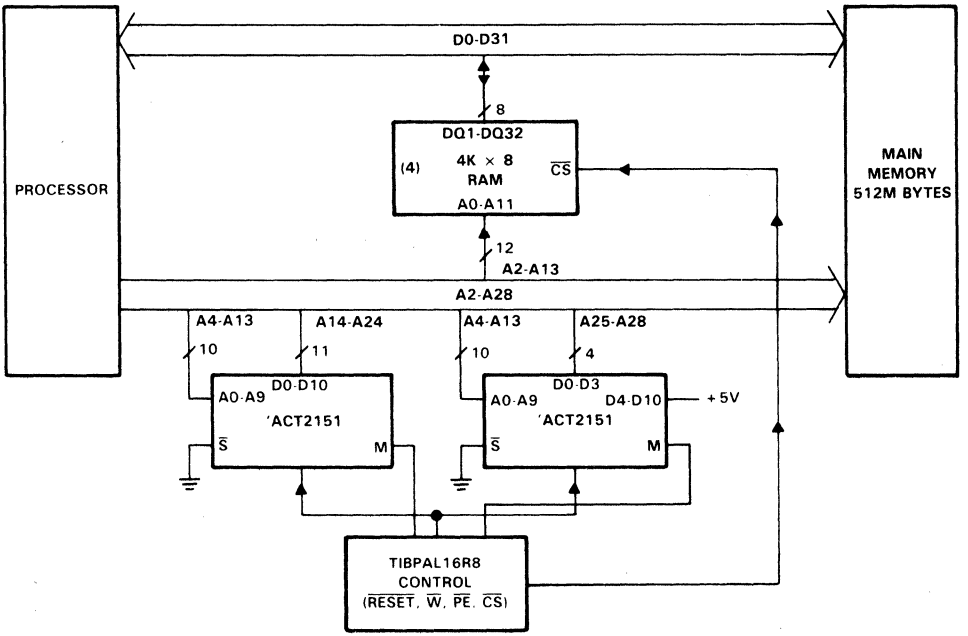


Figure 4. Cache Memory Configuration; Line Size = 16 Bytes, Cache Size = 16K Bytes

the four words in each block. The next least significant address lines (A4-A13) are used as the set select inputs to the cache buffer RAM and the cache tag RAM. The remaining high-order address lines (A14-A28) form the label or tag which is stored and compared by the tag RAM.

Since the label in this example is composed of 15 address lines, two 'ACT2151 devices are used to expand the tag. The 15 address lines are the data inputs to the tag RAM. The other data inputs are tied to 5 V so that, after Reset, invalid data cannot force a match. The match output of the two 'ACT2151 devices are combined to form the enable for the cache data buffer. If the contents of either 'ACT2151 do not contain a match, the cache is not enabled. These signals are also used by the control circuits to inform the system that the address is not present in the cache so that main memory might be accessed. The control circuit also resets the cache upon power-up. This is accomplished by taking the $\overline{\text{RESET}}$ input of the 'ACT2151 low. After reset, no matches will occur at any locations until that location has been written.

In the application shown in Figure 5, the expansion of the tag RAM is carried out in both depth (more sets) and width (wider tag). The block size is chosen as one such that the 4K cache now represents 4096 blocks of one word each. The high-order addresses are still used as the label to the tag RAM. A11 is used to select between two 'ACT2152

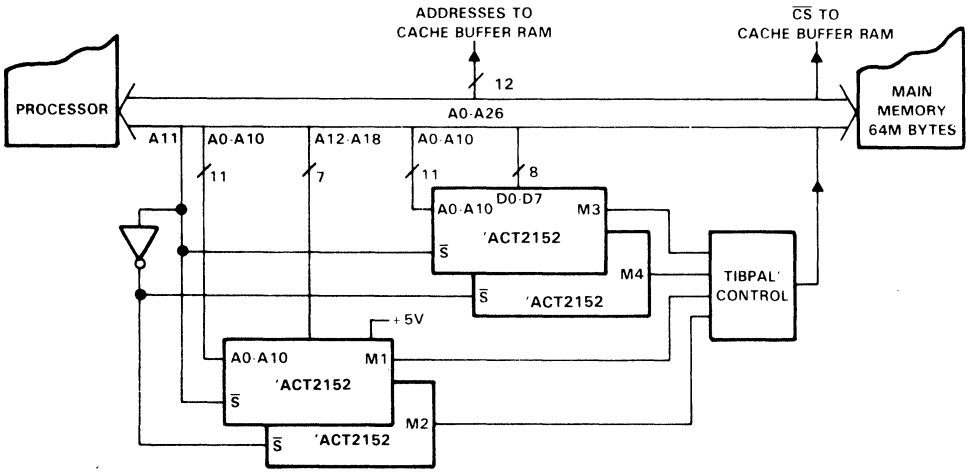


Figure 5. Cache Memory Configuration, Line Size = 4 Bytes

pairs. Each pair contains labels for 2048 of the cache-memory blocks. Address lines A2 thru A12 are used as the set-address inputs. If the chip select ($\overline{CS}$) is at a logic high (deselected), the 'ACT2152 match output (M) is high. An AND function can be used to enable the cache data buffers and also notify the control circuit if access needs to be made into the main memory. The logic for this system illustrates that the upper pair are compared for the first 2048 blocks within cache and the lower pair are compared for the second depending on the state of address A11.

A 2-way cache structure (K = 2) is shown in Figure 6. The 4M-word memory is divided into 4096 sets of 1024 one-word blocks. In this example, A0 and A1 are used to select which one of the four bytes within a block are accessed. A2-A12 select which of the 2048 block labels are to be compared. Addresses A14-A21 form the eight-bit label for the block. Address A13 is used by the cache control logic in conjunction with the possible processor status lines as chip select inputs. The match outputs from the two 'ACT2152 devices, A1 and A2, are NANDed to form an active-low enable to the cache data buffers and to serve as a request to the control logic. The match outputs from B1 and B2 also are NANDed to perform a similar function for cache RAM B. If no match is found in cache RAM A or B, the control logic will initiate an access from main memory. The purpose of the 2-way-cache architecture is to allow for rapid switching between multiple tasks or programs since the processor can have access to two blocks in any one set in cache at the same time. The 2-way cache approach also yields more replacement options than the single-cache architecture. When an access results in a miss in the single-cache system, the data in cache is replaced by the current data even though the old data may still be useful. By using independent caches, the control can determine which data is most expendable and replace that block while the other caches keep their potentially useful data.

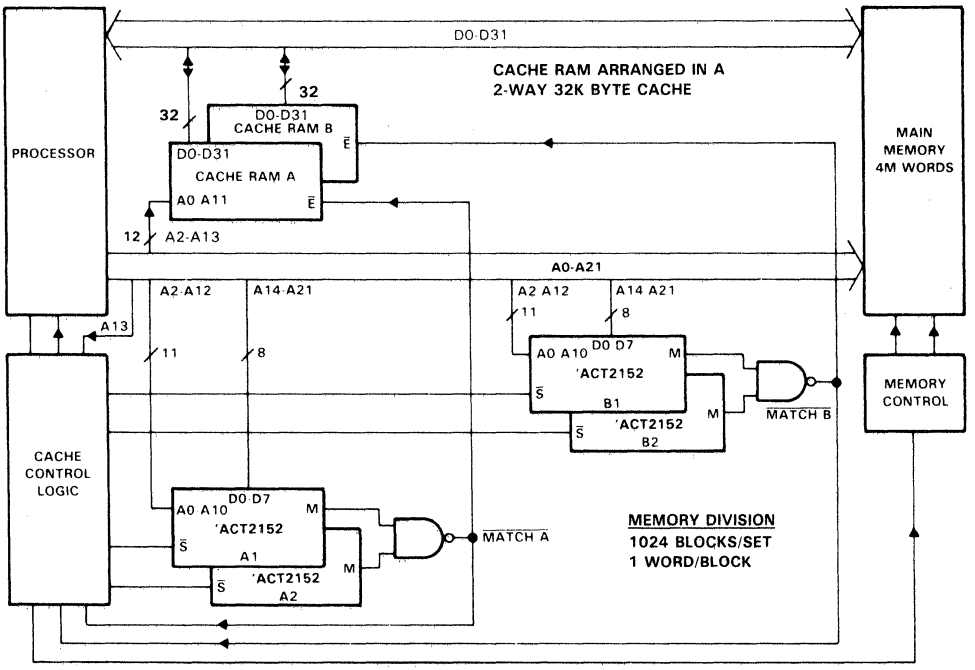


Figure 6. Cache Memory Configuration, 2-Way Cache (K = 2)

Summary

Cache-memory architecture can enhance the throughput of many microprocessor systems. This allows large low-cost memory to perform like a high-speed RAM. The 'ACT2151 and 'ACT2152 reduce the tag memory implementation cost and complexity and provides label comparison times comparable to the access times of high-speed memories. These additional benefits make high-performance microprocessor designs that can use the same techniques of optimizing cost, memory size, and throughput that had previously been available only in larger computer applications.

Advantages of Creating Your Own Cache Solution

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To Obtain Price/Performance Flexibility and Control

Programmable Array or ASIC control logic can be designed to control a wide range of SRAMs and cache address comparators, commonly referred to as cache tags. This provides for both high-end/medium cost and low-end/ low-cost solutions. The price of some systems can be varied by using this flexibility to provide a range of cache options for the customer.

Control of Architectural Features to Differentiate a System

Cache size, line size, set associativity, main memory update scheme (write-through or copy-back), bus-watching methodology, buffering and system control are variables that can be used to optimize each cache solution and differentiate your system. For example, integrated cache controller solutions are usually forced into making performance tradeoffs because of silicon limitations. These solutions usually dictate the line size necessary to achieve a given cache size. Line size is one of the variables that most greatly affects cache performance. Through the use of a TI cache tag RAM and control logic (ASIC or Programmable Array) a line size can be chosen based on the system architecture to provide optimized system performance.

Achieve Complete Most Efficient Use of Cache Memory

Integrated solutions normally use a sub-block approach for mapping cache data. For example, one tag and 8 valid bits were used in the 82385 cache controller to map eight 32-bit words in the cache data RAMs. This was done to reduce the amount of on-chip memory needed to implement an integrated cache controller. This is a good approach but for the best performance, the line size used must match the number of valid bits (in this example, the line size must be 32 bytes or eight 32-bit words). If the line size is less than the number of valid bits, then every tag miss will result in empty cache locations. If the line size is one 32-bit word or 4 bytes and each tag maps 8 32-bit words or 32 bytes, then each tag miss will result in 7 empty cache locations or 28 waisted bytes. This can not be efficient. The use of TI cache tag RAMs allows the designer to assign one tag per line or one tag per word optimizing the cache performance.

Cache Solutions for the Intel i486™ Microprocessor

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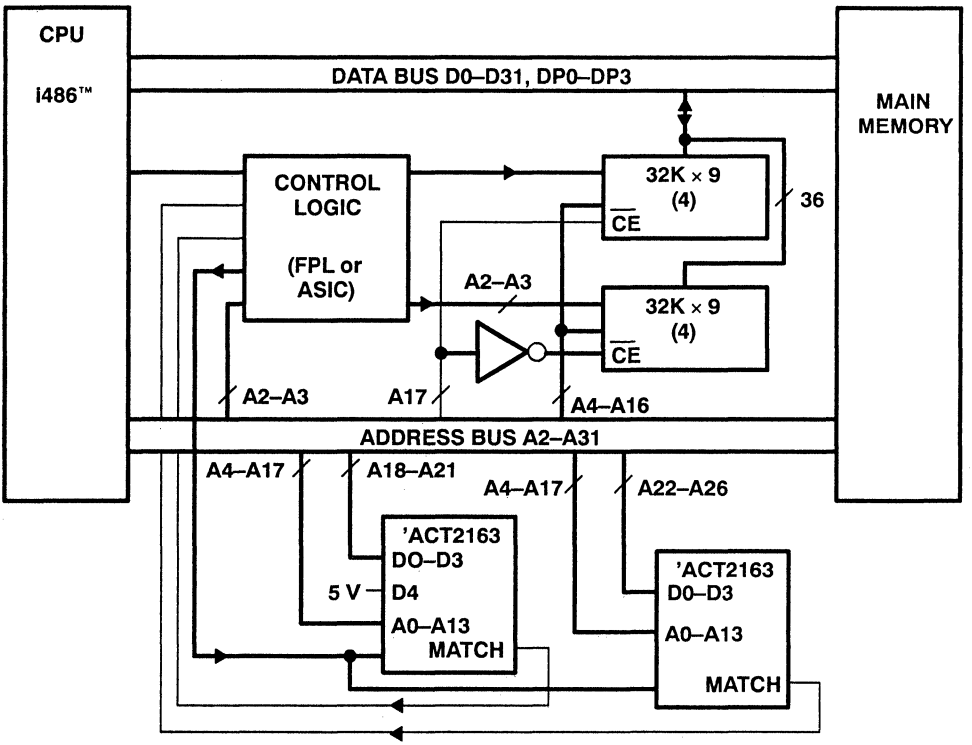
Contents

Introduction

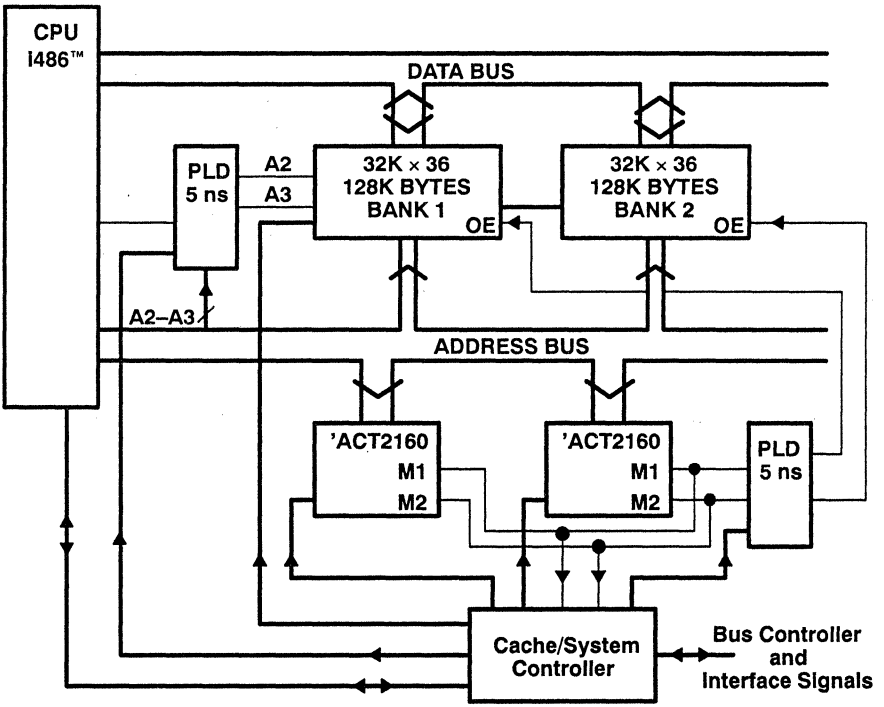
This application report deals with an explanation of how to interface TI's SN74ACT2163 and SN74ACT2160 cache tags with the Intel i486™. A discussion of the cache critical path design, cache coherency solutions for the Intel i486™, and copy-back or buffered writes is included to assist in the design.



NOTE: Cache main memory coverage with two 'ACT2163s, a line size of 16 bytes, and one valid bit is 32M (128M bytes). One additional 'ACT2163 will cover total address range. This design can supply zero wait state cache data to the Intel i486™ in the burst mode.

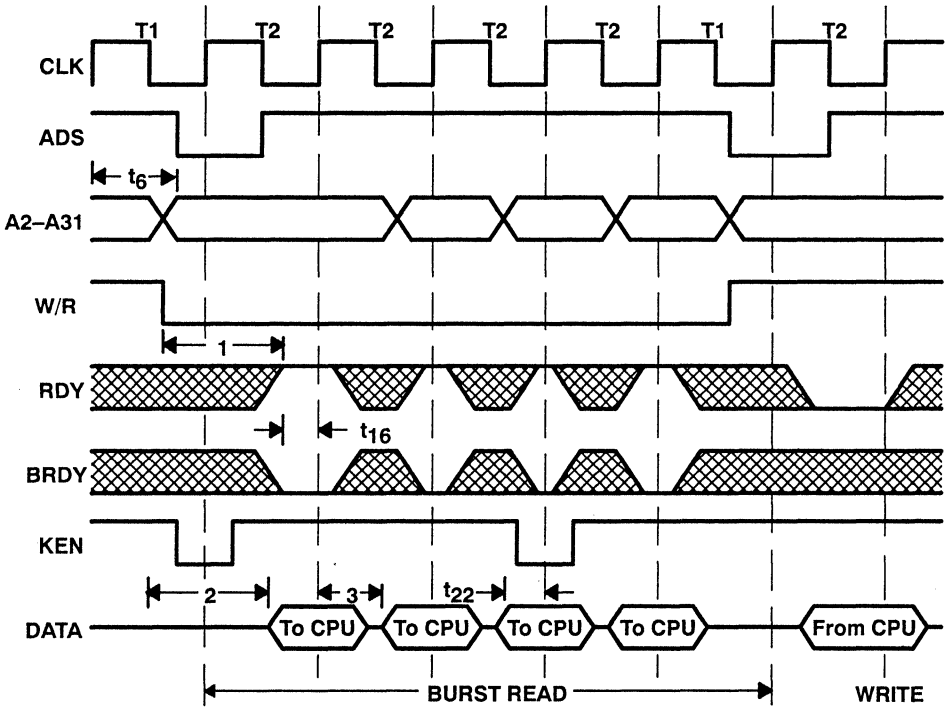
Figure 1. 256K Byte Direct-Mapped Cache for the i486™ Using the TI SN74ACT2163 Line Size = 16 Bytes

i486 is a trademark of Intel Corporation.



NOTE: The number of 'ACT2160s required depends on the amount of main memory covered. The 'ACT2160 can be cascaded in depth to provide even bigger caches. This design can supply zero wait state cache data to the i486™ in the burst mode.

Figure 2. 256K Byte 2-Way Cache for the i486™ Using the SN74ACT2160 2-Way Cache Tag Line Size = 16 Bytes



NOTE: Preliminary Intel 33 MHz Intel i486™ specs. t_6 = 16 ns MAX, t_{16} = 5 ns MIN, t_{22} = 5 ns MIN.

Figure 3. Intel i486™ Timing Diagram

Cache Design Critical Paths

1. Address valid to RDY and BRDY:
   (CLK period × 2) – t_6 – t_{16} = 60 – 16 – 5 = 39 ns
2. Address valid to data setup (first word):
   (CLK period × 2) – t_6 – t_{22} = 60 – 16 – 5 = 39 ns
3. Burst address valid to data setup (2^{nd}, 3^{rd}, 4^{th} word):
   (CLK period × 1) – t_6 – t_{22} = 30 – 19 – 5 = 6 ns
   To achieve zero wait state reads, the burst address must be generated manually.
   CLK period × 1 – t_{22} = 30 – 5 = 25 ns

Therefore:

1. RDY and BRDY are easily generated within 39 ns.
2. t_{pd} tag RAM + t_{pd} control logic + t_{oe} SRAM < 39
   This can be achieved using a 17-20 ns cache tag, a 5-7 ns programmable logic device (PLD), and an SRAM with an 8-10 ns t_{oe} time. Or for direct mapped cache designs with zero wait state reads, it is reasonable to assume a hit and enable the cache SRAM early. Using this assumption, this critical path then becomes t_{pd} tag RAM + t_{pd} control logic < 39 ns. This method allows slower control logic to be used in the critical path (i.e., 10-15 ns programmable logic).
3. t_{pd} manual burst control + t_{AA} SRAM < 25 ns. The HM67B932 has 10-13 ns row address access time allowing about 10 ns for burst control. Another solution would be to multiplex 4 banks of SRAM using the chip select or output enable inputs.

Cache Coherency Solutions for the Intel i486™

When designing a second level cache for the Intel i486™, special consideration must be given to the coherency solution. The internal Intel i486™ cache is 4-way set associative. Bus watching or snooping is achieved with the Intel i486™ by applying the snoop address to the Intel i486™ address bus and asserting the EADS' signal. If an internal snoop hit occurs, the appropriate cache entry is invalidated. Other Intel i486™ operations are put on hold during an invalidation cycle. There are two basic methods of insuring coherency when using a second level cache.

1. This method allows data to reside in the Intel i486™ cache that is not in the second level cache.

   During a bus snoop cycle, the snoop address is applied to both the Intel i486™ and to the second level cache. When a snoop hit occurs, the matching cache entries are invalidated. This method causes the Intel i486™ to hold every time

bus snooping is performed. This method is probably acceptable to DOS applications since the CPU is held up during DMA.

2. This method insures that data in the Intel i486™ cache always resides in the second level cache.

   During a bus snoop cycle, the snoop address is applied only to the second level cache. When a snoop hit occurs, the snoop address is then applied to the Intel i486™ for invalidation. This method requires an Intel i486™ invalidation cycle during each second level read miss cycle. This can be achieved by applying the index and stored tag of the cache data that will be replaced to the Intel i486™, while data is being fetched from main memory.

Copy-Back or Buffered Writes

Since the Intel i486™ has 8K bytes of write-through cache, a high percentage of the traffic seen on the Intel i486™ bus will be write cycles. Because of this, each write cycle must be handled as quickly as possible to achieve maximum processor performance. Minimum write cycle time can be achieved through use of a copy-back cache design or a write buffer. A dirty bit is required for each tag in a copy-back design. Cache tags can be used in copy-back designs if the tag RAM has a read function. The dirty bit must be stored in a RAM separate from the tag bits unless the tag RAM was designed for dirty bit storage. TI FIFOs are a potential solution for write buffer designs. The SN74ALS2233 is a 64 × 9 FIFO and the SN74ALS2238 is a bidirectional 32 × 9 FIFO with a 9-bit selectable flow-through path.

SN74ACT2155/56 Cache Enhances MC68030 Processor Performance

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Contents

List of Illustrations

Abstract

When 32-bit microprocessor speeds advanced into the high-end performance spectrum, designers discovered that to capitalize on the performance of these microprocessors, cache memories must be incorporated into their designs. Although most of the new cache address comparators are covered, this report covers the SN74ACT2155 in detail. The sole purpose of the SN74ACT2155 is to maximize the performance of the newly released Motorola MC68030 (hereinafter MC68030) 32-bit microprocessor. The cache requirements of the MC68030 and the associated benefits of the SN74ACT2155 are presented. A functional description of the SN74ACT2155 is provided. In addition, support documentation illustrating the cache interface to the MC68030 is provided. Advanced cache schemes such as copy-back and bus-watching implementations are also addressed through the use of this intelligent cache address comparator.

Larger Caches Using the SN74ACT2156

Since the first printing of this applications note, a deeper version of the SN74ACT2155 has been made available. The SN74ACT2156 is designed with a 16K × 5 Static RAM array. The SN74ACT2156 includes all the control and interface logic that is incorporated in the SN74ACT2155. The SN74ACT2156 is ideal for cache sizes of 64K bytes and greater.

Introduction

The speed of the new 32-bit microprocessors has dramatically exceeded the speed capabilities of the current dynamic random access memories (DRAMs). At frequencies of 20 MHz and above, the access times of commodity DRAMs are the constraining factor in the 32-bit processors reaching their full performance potential. At 20-MHz operating speed, the basic clock cycle is only 50 ns. For most memory-access schemes, these microprocessors require a minimum of one and a half to two clock cycles to access data from main memory. When the CPU performs a memory operation, the DRAM-access time coupled with propagation delays, multiple levels of address decoding, and other timing control delays provide a considerable overhead to the CPU cycle time. The combination of all these extra timing delays results in the unavoidable inclusion of wait states that degrade overall system performance. Therefore, designers must adopt certain architectural refinements to fully capitalize on the performance of the 32-bit microprocessor. Static memories have been considered the solution to this memory bottleneck, but static RAMs are far more costly, more bulky, and require more power than DRAMs. Only the highest-performance applications can justify using static RAMs for main memory. DRAMs continue to be the most effective means of designing system memories with regards to power, board space, and cost per bit.

For microprocessors that operate in the 16-MHz range, it is possible to design zero-wait-state systems by using fast DRAMs and techniques that incorporate interleaving. As

the microprocessor speed increases into the 20-MHz, 25-MHz, and 33-MHz ranges, it is evident that designers must adopt certain architectural refinements in their system design. One refinement is to employ a hierarchical memory scheme in which high-speed cache or buffer memory is inserted between the microprocessor and main memory. The cache or buffer memory holds the most frequently used portions of main memory.

Cache memories are the accepted method of achieving SRAM performance from large DRAM memory arrays. The inclusion of cache memory buffers in a system can eliminate the overhead of wait states and increase system performance dramatically.

The ideal place for incorporating a cache memory is within the microprocessor. This approach is incorporated in the MC68030 32-bit microprocessor, which includes internal 256-byte instruction and 256-byte data caches. Although the size of these caches partially improves the MC68030 performance, they are not large enough to provide the processor with the performance that is usually desired. Maximizing the cache hit rate or the probability of finding referenced data in the cache is the key requirement for optimizing the design of a cache memory. In order to achieve 75% to 95% hit rates, cache sizes of 8K bytes or more are usually required. Adding such a cache size along with the required cache management logic to a single chip microprocessor is practically impossible with current technology.

Therefore, a practical solution is to extend the architecture outside the microprocessor. This allows the designer to incorporate any given size or design of cache memory based on system cost, speed requirements, and board space limitations. An external cache built to interface with the on-chip cache of the microprocessor actually complements the internal cache. The MC68030 burst-mode feature is a means by which information can be quickly loaded into the internal caches. The burst-mode feature of the MC68030 is explained in the following paragraphs.

MC68030 Cache Burst-Fill Requirement

The burst mode of the MC68030 allows a block of four long words to be loaded into the internal caches very quickly. It allows the processor to latch external data in as little as one clock cycle for each 32 bits. Before designing a cache for the MC68030, it is important to understand how the burst cycle operates.

During an MC68030 cache burst-fill cycle, the MC68030 outputs one address for the first long word it is requesting. This one address is then used externally to identify the block of four long words that the MC68030 will load on the next four clock edges (assuming zero-wait states). Address bits A3 and A2 identify the first word the processor is requesting. The first data word is received by the MC68030 on the first falling clock edge after $\overline{\text{STERM}}$ is asserted. $\overline{\text{STERM}}$ is an MC68030 input signal. When $\overline{\text{STERM}}$ is low, it indicates to the MC68030 that data may be latched on the next falling clock edge. On the second clock edge, the MC68030 receives a second long word provided that $\overline{\text{STERM}}$ is low. The operation is repeated until the four words have been loaded into the MC68030 internal cache. During a cache burst fill, the MC68030 sequentially loads the internal cache.

That is, if A3,A2 are initially 1,0, A3,A2 must be externally incremented from 1,0 to 1,1 to 0,0 to 0,1. If the information cannot be retrieved in one clock cycle, wait states can be added by taking $\overline{\text{STERM}}$ high to provide the extra time necessary to access the data. A low level on the BERR input of the MC68030 during a burst cycle terminates the burst cycle and the MC68030 processes the portion of the addressed block of data that is in the internal cache.

To efficiently address the burst-fill requirement of the MC68030 while maintaining zero-wait states, the requested data must reside in a fast-cache memory. The use of a properly designed external cache not only provides zero-wait state burst operation but also allows single accesses to be performed in two clock cycles. In addition, the external cache can be designed to significantly reduce main memory bus traffic.

Several methods exist for designing a cache that will support the cache burst-fill requirements of the MC68030. A brief description of these methods provides the basis for assessing the various advantages/disadvantages affiliated with each method. The SN74ACT2155 cache address comparator and SRAM, which will be described in detail, has been designed specifically to meet the requirements of the MC68030 cache burst mode and to eliminate the disadvantages associated with the other methods.

By evaluating these methods, it will be seen that the SN74ACT2155 is the best cache approach for high-speed MC68030 microprocessors. As with most cache designs, it is desirable to build a cache so that it can be easily upgraded. When deciding which method to use, the designer needs to be assured that the method used will work with faster MC68030s as they become available.

Methods of MC68030 Cache Design

Before attempting to design a cache that will efficiently serve the MC68030, system timing must be considered to determine the critical speed paths. If the cache system is to be compatible with MC68030 speed upgrades, an estimate of delay times must be made. Figure 1 shows an MC68030 synchronous read cycle. If a cache read is to be performed in two clock cycles, the amount of time available to compare addresses and tell the microprocessor whether to force wait states is t_{pd1}. The t_{pd1} values for different microprocessor speeds are as follows:

1. 20 MHz, t_{pd1} = 25 ns
2. 25 MHz, t_{pd1} = 20 ns
3. 33 MHz, t_{pd1} = 15 ns
4. 40 MHz, t_{pd1} = 12.5 ns.

As shown by the estimated delay times, the high-frequency microprocessors offer a challenge to the cache-memory designer. For a cache to supply data to the MC68030 with zero-wait states, both the cache data buffers and the tag comparison or directory portions of the cache must be considered.

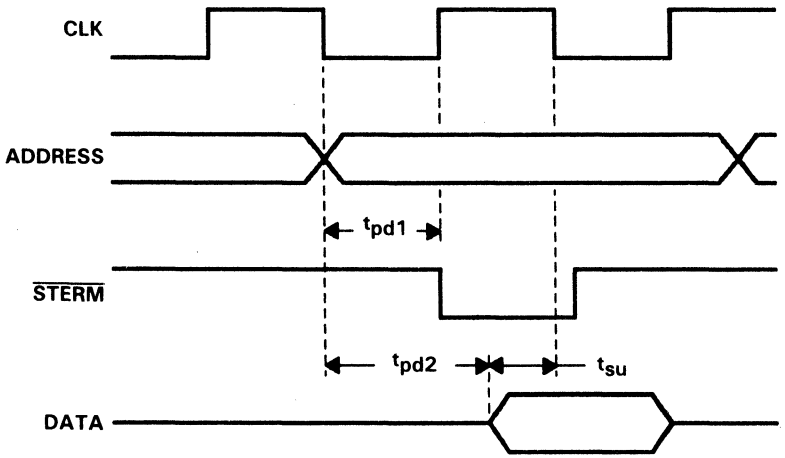


Figure 1. MC68030 Synchronous Read Cycle

There are several ways that the cache data buffer can be arranged to support the burst mode. The first way is to use a counter/multiplexer circuit to drive the A1,A0 inputs of the data RAMs. (See Figure 2)

The two-bit counter must be able to load the initial A3,A2 from the MC68030 and increment sequentially to address the next three long words in cache. As shown in Figure 1, t_{pd2} is the maximum delay time from the address through the counter/multiplexer circuit and SRAM back to the MC68030. The t_{pd2} values for different microprocessor speeds are as follows:

1. 20 MHz, t_{pd2} = 45 ns
2. 25 MHz, t_{pd2} = 35 ns
3. 33 MHz, t_{pd2} = 29 ns
4. 40 MHz, t_{pd2} = 22.5 ns.

The circuit in Figure 2 can be implemented at slower microprocessor speeds by using fast SRAMs and programmable logic and still obtain zero-wait-state operation. However, as the clock frequency is increased, the delay through a discrete counter/multiplexer and SRAM implementation makes a zero-wait-state burst-fill cycle questionable. Another method of arranging the cache buffer is to use four banks of data with each bank storing one of the four long words. (See Figure 3)

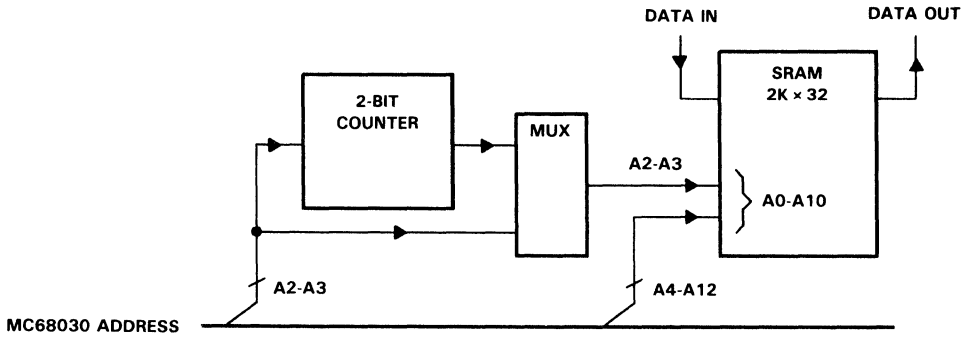


Figure 2. Counter/Multiplexer Required to Provide Data to the MC68030 During Burst Mode

With this approach, all four long words are addressed in parallel and address bits A3,A2 are used to determine which of the four banks should drive the data bus. If main memory is arranged in a similar manner, a block of four words is loaded very quickly into cache reducing cache miss delay. This approach also improves bus bandwidth. The disadvantage of this approach is that extra parts and board space are required for implementation.

The tag storage and comparison circuits must be able to indicate whether the requested block of data resides in the cache buffer. There are several ways this can be done. In a simple write-through cache, standard cache-tag chips could be used to indicate whether an addressed block of four long words is in cache. See Figure 4.

The TI SN74ACT21XX family of cache address comparators can be used to indicate whether the block exists in cache. The match output is gated with other signals and fed back to the MC68030 to allow data to be latched into the microprocessor when a hit occurs. The delay path consists of the address to match time plus the delay through the MC68030 interface logic. This is a viable tag solution for microprocessor speeds in the 16-MHz to 20-MHz range. However, the tag and logic must be very fast to run with a faster MC68030 and still achieve zero-wait-state operation.

If bus watching is required to guarantee data coherency or if the unit of transfer between main memory and cache is not always four long words or a multiple of four long words, each long word must be checked for cache residency before it is loaded into the MC68030. There are two ways the tag directory can be organized to check for cache residency: by using one tag and four valid bits per four long words or by using one tag per long word.

When using one tag and four valid bits (see Figure 5), the tag is used to indicate whether the requested block is in cache. The four valid bits indicate the validity of each of the four words in the block.

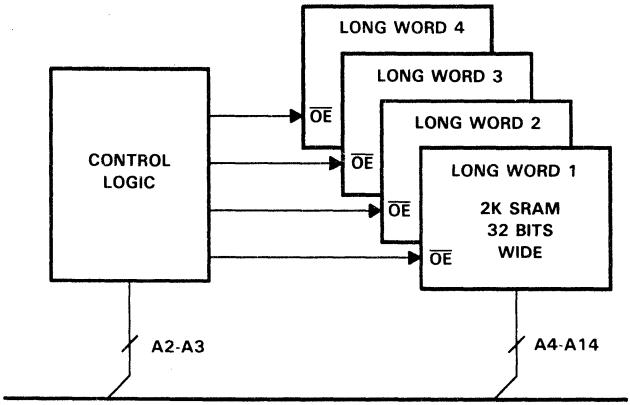


Figure 3. Four SRAM Banks Used in Parallel to Supply Four Long Words for MC68030 Burst Mode

Address bits A3 and A2 are used to select the proper one-of-four valid bits for the addressed word. When a valid bit is high, the requested data is resident in cache. As long as the rest of the address matches with the stored tag and the selected valid bit remains high, the addressed cache data can be sent to the microprocessor. While the first long word is being checked for validity, the other three valid bits can be monitored to give the status of the three sequential long words. Again, timing becomes a question with a faster MC68030. The delay consists of the address-to-match time of the tag RAM plus the delay required to combine the valid bit with the match signal and tell the microprocessor whether to force a wait state. Another disadvantage to this approach is a potential decrease in the hit rate. When a tag miss occurs requiring the cache to be updated, all four long words in the block must be replaced. If only one long word is replaced, the other three long words in the block must be invalidated. This results in a number of empty cache locations and the hit rate is reduced.

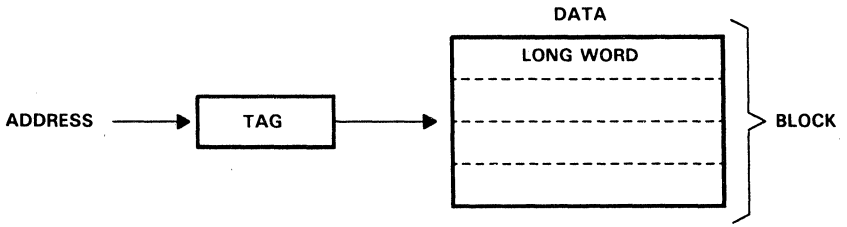


Figure 4. One TAG per Block. Each Block Contains Four Long Words

The other method is to use one tag per long word and use a counter/multiplexer to increment from tag to tag during a cache burst-fill cycle (see Figure 6).

A bit per each tag stored in the tag RAM can be used as a valid bit eliminating extra delay. When a miss occurs, standard logic can be used to monitor the match output and force wait states. Standard cache tag chips and programmable logic can be used to implement this, but timing becomes an obstacle at faster clock frequencies. The delay paths are through the counter/multiplexer, the cache tag chip, and interface logic. The SN74ACT2155 integrates the counter/multiplexer, tag logic, and interface logic mentioned in this method to minimize the overall delay and provide a cache that meets the timing requirements of the MC68030.

SN74ACT2155

The SN74ACT2155 is designed specifically to meet the requirements of the MC68030 cache-burst mode. It consists of a high-speed 2K × 9 Static RAM array, 2-bit burst counter and control circuits, parity generator, parity checker, and an 8-bit high-speed comparator. The SN74ACT2155 is designed to supply a tag and data RAM that interfaces directly with the MC68030. The overall system performance is optimized by eliminating the added delays that are incurred when implementing the cache discretely. The SN74ACT2155 is a building block that provides the architectural flexibility that cache designers require. The SN74ACT2155 can be used for write-through or copy-back caches, for bus watching, and as both the tag and data RAM. The SN74ACT2155 is cascadable for various cache depths and tag widths. Figure 7 is a logic diagram of the SN74ACT2155.

SN74ACT2155 Counter/Multiplexer Circuit

The 2-bit counter and multiplexer circuit is designed into the SN74ACT2155 without any increase in access or address to match time. As shown in Figure 8, the counter/multiplexer circuit is controlled through use of the MC68030 signals $\overline{\text{CBREQ}}$, $\overline{\text{CBACK}}$, and $\overline{\text{STERM}}$ and is clocked using the system clock (PCLK).

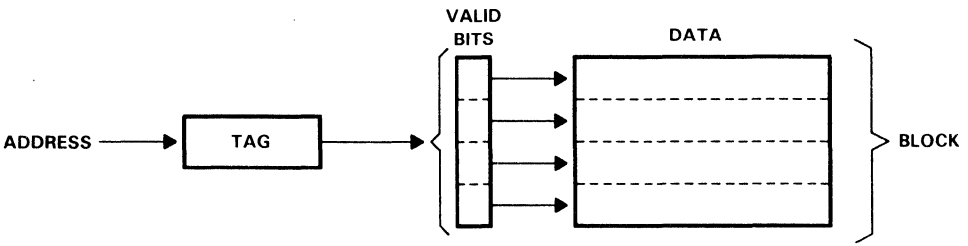


Figure 5. One TAG and Four Valid Bits per Block

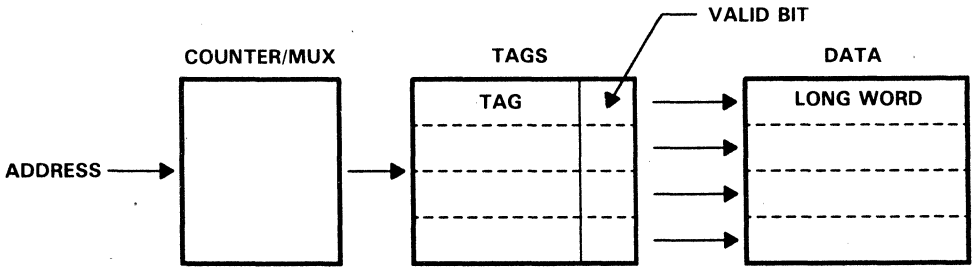


Figure 6. One TAG with One Valid Bit per Long Word

The burst control register (BCR) is used to control the multiplexer that selects address bits A2 and A3 from the address bus or from the internal 2-bit counter. When either $\overline{\text{CBREQ}}$ or $\overline{\text{CBACK}}$ are high, the burst-control register is asynchronously reset causing the multiplexer to select address bus inputs A3 and A2 (A1 and A0 on the SN74ACT2155). With $\overline{\text{CBREQ}}$ and $\overline{\text{CBACK}}$ low, the burst control register is set high when $\overline{\text{STERM}}$ is low during a PCLK falling edge. Simultaneously, the incremented value of A3 and A2 is loaded into the counter and the counter output addresses the next memory location. As long as $\overline{\text{STERM}}$ is low, the counter will advance to the next memory location in the four-word block.

SN74ACT2155 Tag RAM and MC68030 Direct Interface

The SN74ACT2155 is designed as a tag comparator that uses one tag per each long word in cache. The data stored in cache is mapped in the SN74ACT2155 tag RAM by storing upper order address bits (referred to as the tag) into the RAM locations addressed by the lower-order address bits (A2-A12). When the processor performs an access, the lower-order address bits address a memory location and the stored tag is compared to the current upper order address bits. If a match occurs, the requested data is in the cache. During a burst mode, the counter/multiplexer circuit is used to advance from tag to tag until the burst is completed. Each tag is compared to determine if the requested word is resident in cache and is valid. By directly interfacing with the MC68030, the tag comparison can be done without adding wait states. This direct interface is described in the following paragraphs.

When a cache is designed properly, most of the microprocessor accesses will be to the cache rather than to main memory. Therefore, it is reasonable to use cache control logic that assumes a hit will occur every time an access is started for cacheable data. This is accomplished by asserting the MC68030 input signal $\overline{\text{STERM}}$ at the beginning of the access cycle, (at or before t_{pd1}max) rather than waiting for the cache directory to indicate whether to insert wait states. When a miss does occur, MC68030 input signals BERR and HALT can be forced low at the last nanosecond causing the MC68030 to retry or "rerun" the access cycle. As shown in Figure 9, the maximum allowable delay time from address to required cache response is increased from t_{pd1} to t_{pd3}. This approach saves at least 10 nanoseconds ($t_{pd3} - t_{pd1}$) at all processor speeds.

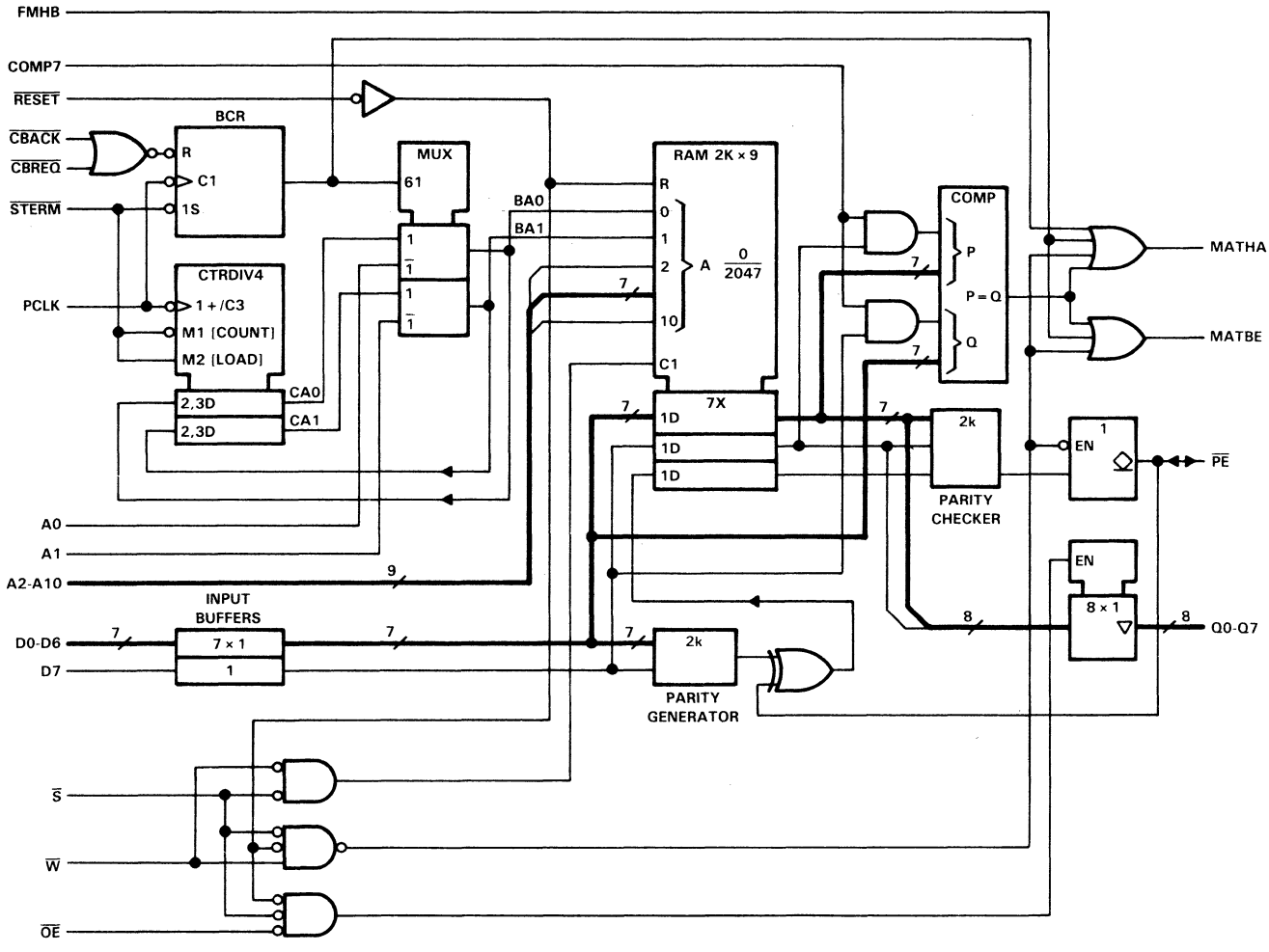


Figure 7. SN74ACT2155 Logic Diagram

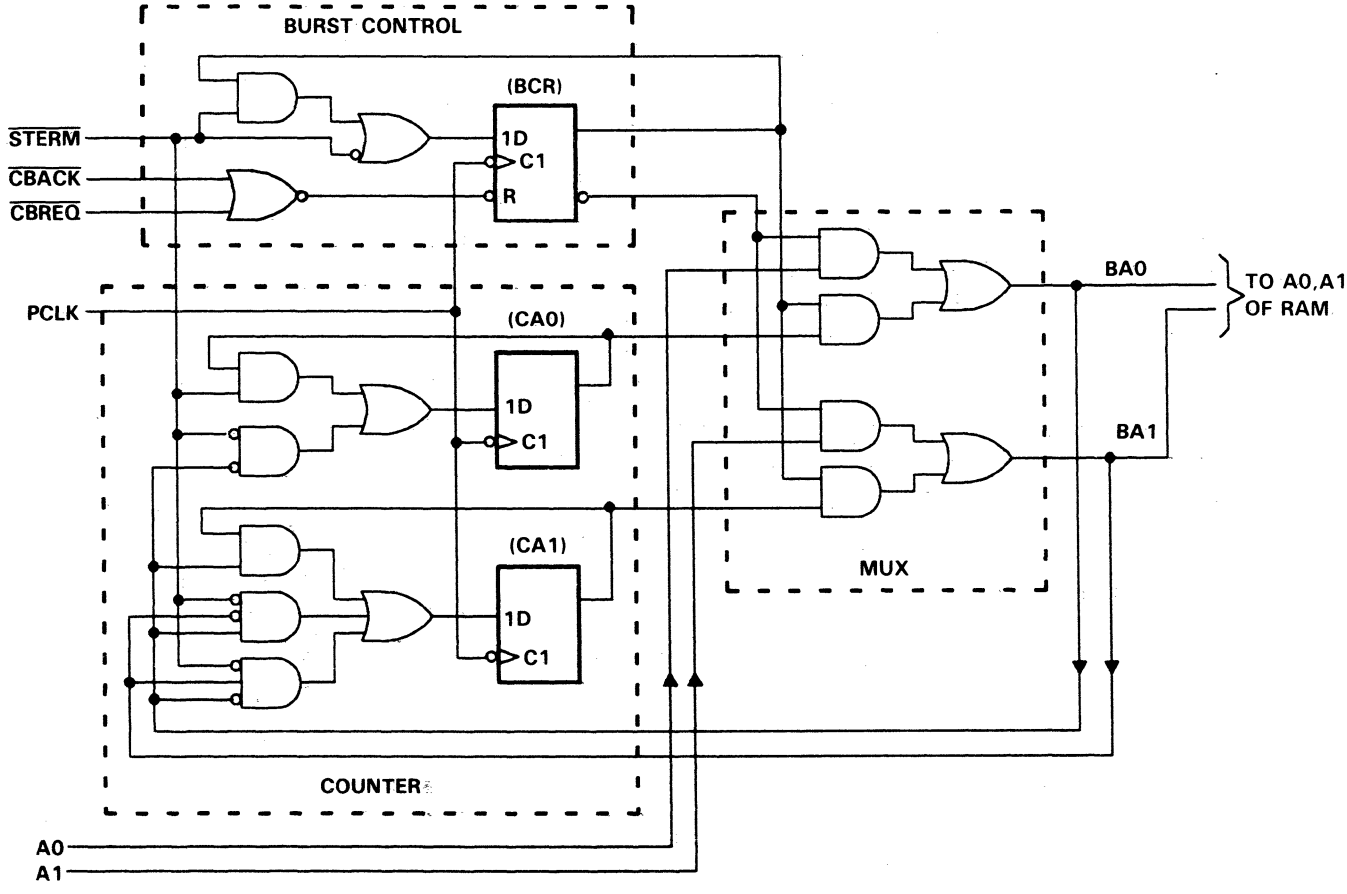


Figure 8. SN74ACT2155 Counter/Multiplexer Circuit

As a tag comparator, the SN74ACT2155 uses the rerun feature of the MC68030 and its direct interface to take advantage of the extra 10 ns. The SN74ACT2155 has two match outputs, MATBE and MATHA, that tie directly to MC68030 inputs BERR and HALT respectively (see Figure 10). When a match occurs, MATBE and MATHA go high driving BERR and HALT high and the MC68030 loads in the cached data without added wait states. When a match occurs during a cache burst mode, the MATHA output is forced high (driving HALT high) after the first word is loaded into the MC68030.

If a miss occurs as each of the next three words are compared, MATBE goes low driving BERR low. When BERR goes low during the burst mode, the bus cycle is terminated and the MC68030 runs with the data it received. When a miss occurs during a regular access or during the first word of a cache burst access, MATBE and MATHA go low driving BERR and HALT low. When both BERR and HALT are low simultaneously, the MC68030 will retry (or rerun) the bus cycle. The FMHB input of the SN74ACT2155 is used to force MATBE and MATHA high during the retry to prevent continuous rerun and the data is then retrieved from main memory. At the same time that data from main memory is being loaded into the MC68030, the new tag (and data) is written into the SN74ACT2155. The same falling clock edge that latches data into the MC68030 advances

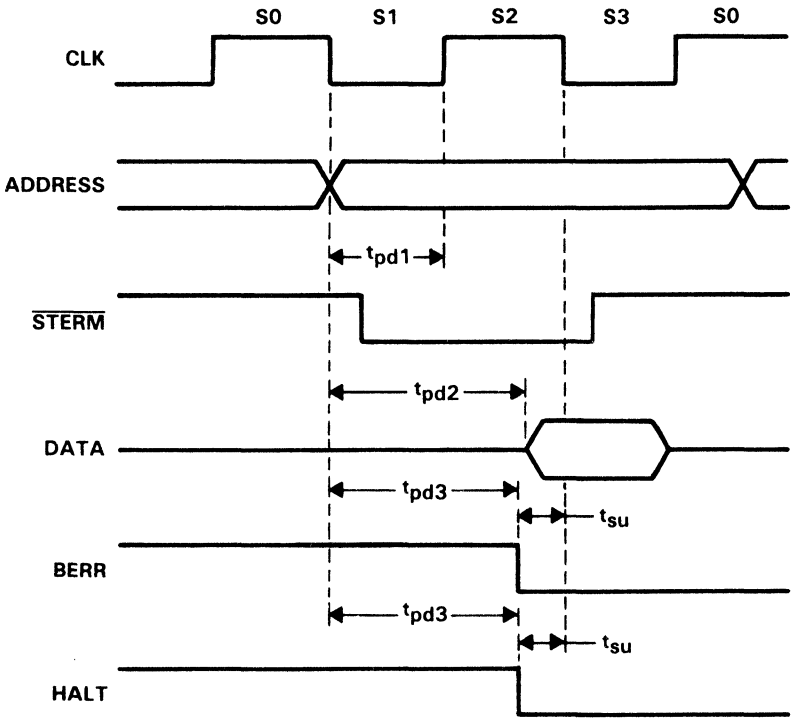


Figure 9. MC68030 Synchronous Access Cycle Using Late Rerun

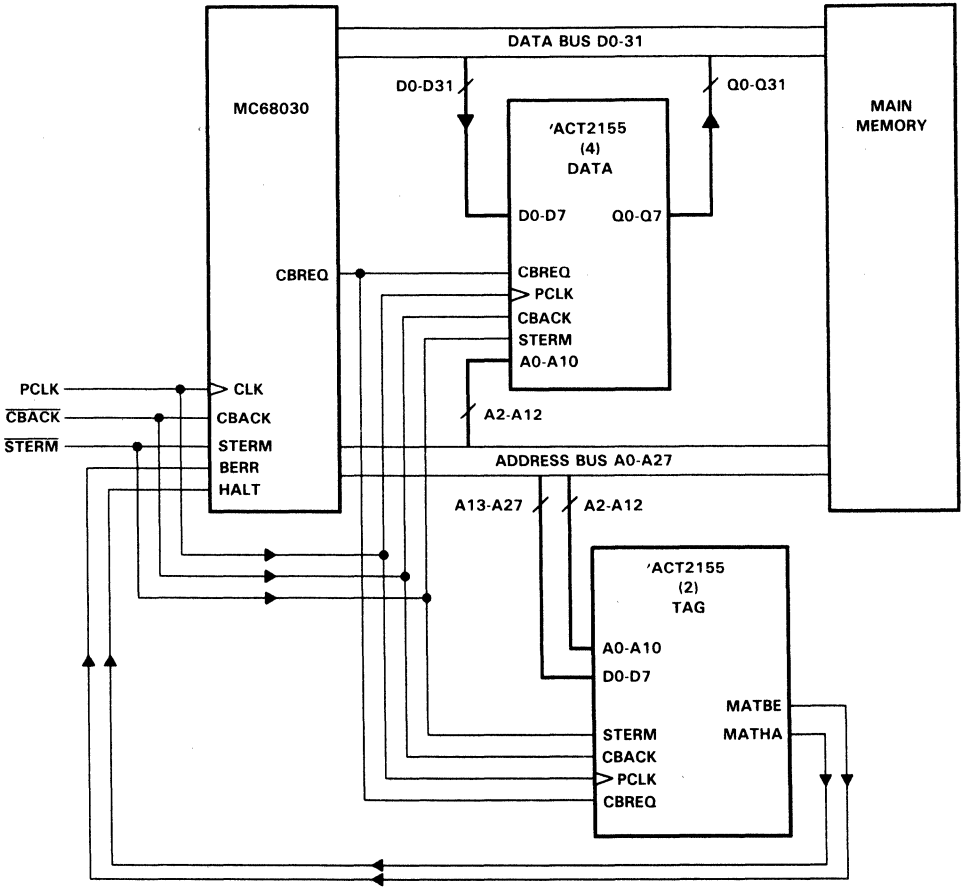


Figure 10. SN74ACT2155/MC68030 Interface

the internal counter so that the next long word and tag from main memory can be written into the SN74ACT2155 (i.e., when $\overline{\text{STERM}}$ is low, a falling clock edge advances the counter). By interfacing directly with the MC68030, the only cache delay path is through the SN74ACT2155.

Using the SN74ACT2155 as the Cache Data SRAM

By using the SN74ACT2155 as the cache data RAM, the only delay path is through the SN74ACT2155. When the MC68030 performs a burst cycle, the processor address selects data that is immediately sent to the MC68030 (assuming a hit). The same falling clock edge that is used to load the data into the MC68030, loads the incremented value of A3 and A2 into the 2-bit counter and switches the multiplexer so that the counter drives

A1 and A0 of the RAM. The counter is incremented on each clock falling edge (with $\overline{\text{STERM}}$ low) until the cache burst cycle is completed. Since the counter/multiplexer does not slow down the RAM access time, the data is returned to the MC68030 without added wait states. When a miss occurs on the first word of the burst mode, the data must be retrieved from main memory. Since the SN74ACT2155 counter only advances when $\overline{\text{STERM}}$ is low, data is easily loaded into cache at the same time it is loaded into the MC68030. Timing diagrams for the burst mode with data in external cache and with data only in main memory are shown in Figures 11 and 12, respectively.

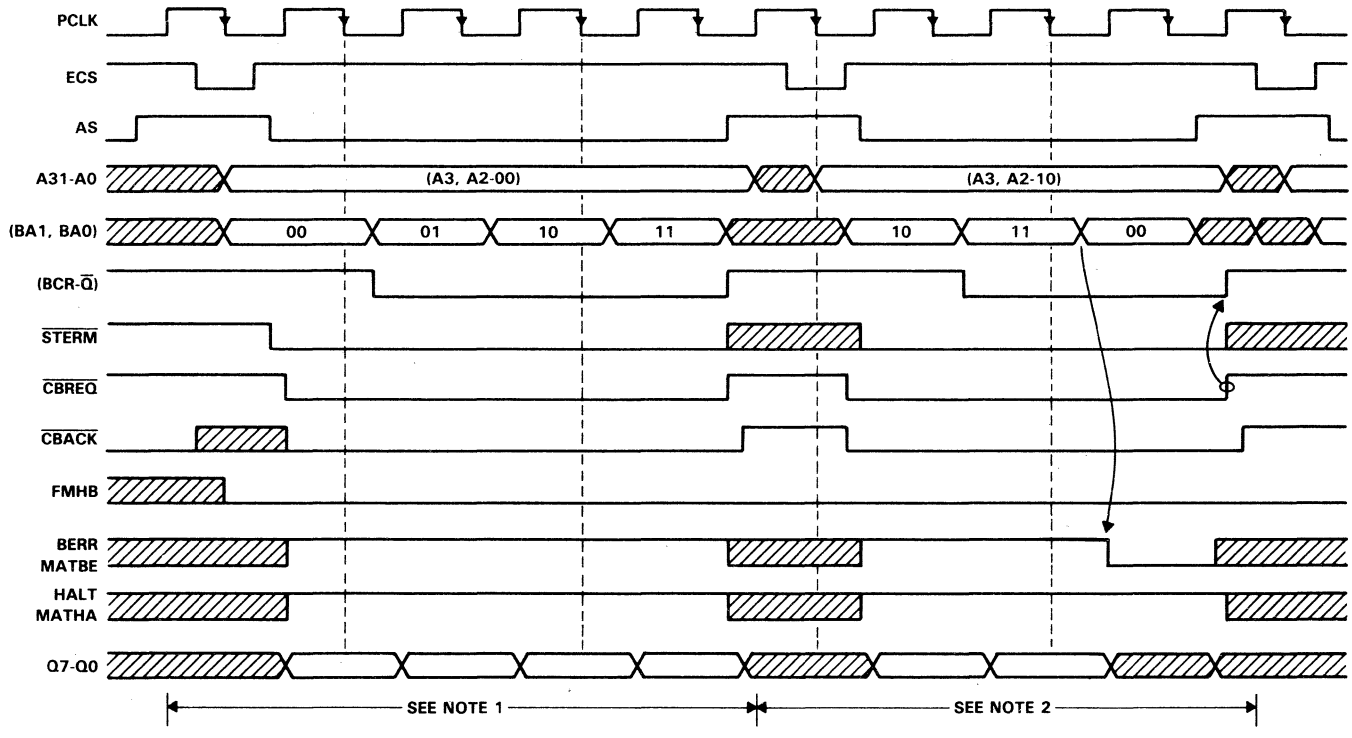
Cascading the SN74ACT2155

As mentioned previously, the SN74ACT2155 is easily cascaded in width and depth (see Figure 13). Wider addresses can be compared by driving the A0 through A10 inputs of each device with the same index and by applying the additional address bits to the D0 through D7 inputs. The select input allows the SN74ACT2155 to be cascaded in depth. When a device is deselected, the MATHA and MATBE outputs are driven high. A decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATHA and MATBE are open-drain outputs for easy wire tying.

Copy-Back Caches Using the SN74ACT2155

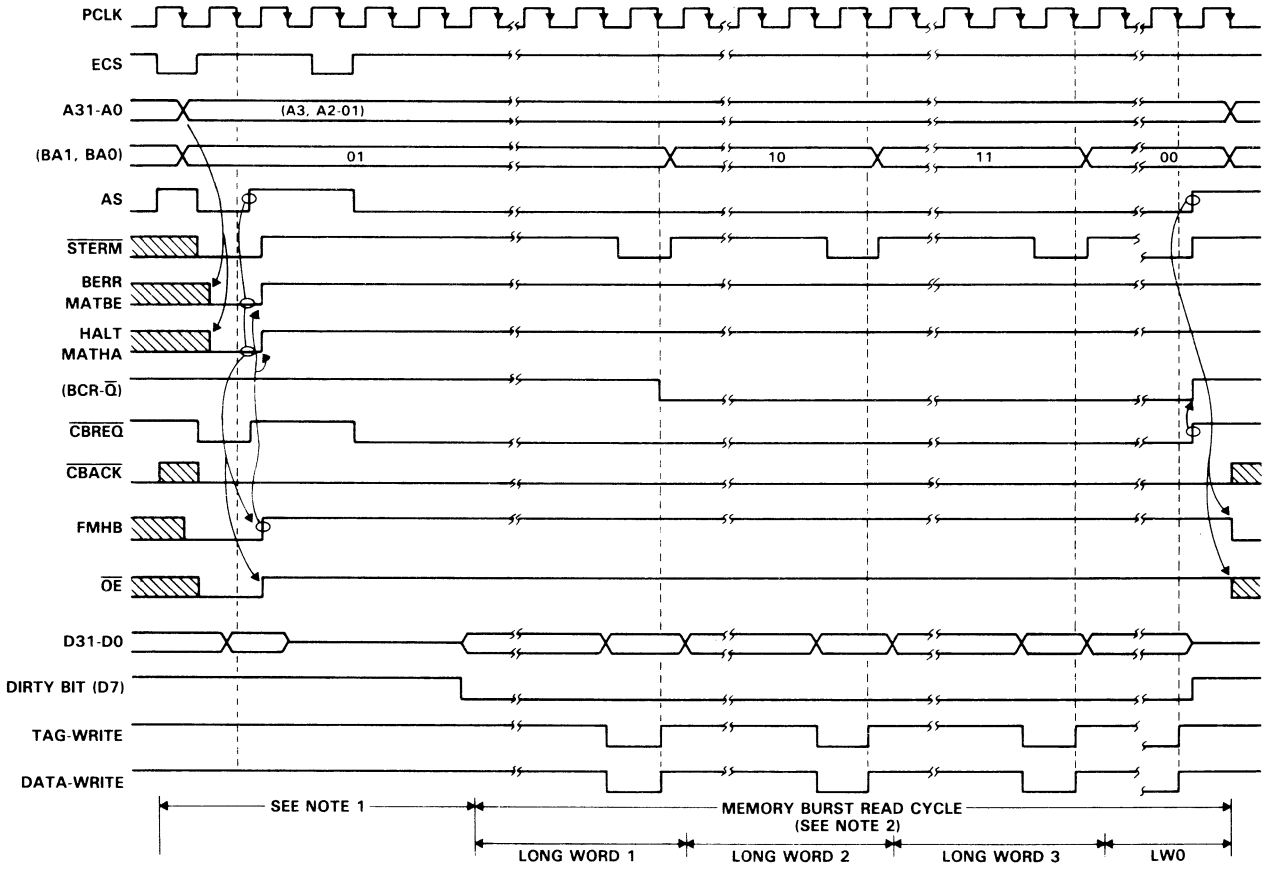
The SN74ACT2155 can be used in write-through cache designs where writes to cache are immediately sent to main memory, or in copy-back cache designs where a cache write initially only modifies the cache and can later be copied back to main memory. Copy-back caches have an advantage in that the number of writes to main memory is reduced usually by a factor of at least two, thereby reducing main memory traffic. Copy-back caches also improve processor performance since write cycles that only involve the cache memory can be performed with zero wait states. To implement a copy-back cache, a dirty bit is needed for each long word in the cache that indicates whether the data is modified from that which is in main memory. When the cache data is modified, the dirty bit is set high. When a miss occurs, data is only copied back to main memory if the dirty bit is set, otherwise it is simply overwritten.

The COMP7 input of the SN74ACT2155 allows bit D7 to be used as a dirty bit. By tying COMP7 low, bits D7 and Q7 are gated out of the comparator and the comparison is only made on D0 through D6. With outputs Q0 through Q7 enabled ($\overline{\text{OE}}$ low), the dirty bit (Q7) can be monitored at the same time as the match signals. If the dirty bit is set during a read or write miss, the tag and data can be stored in latches before writing the new tag and data into cache. The latched data and address can then be copied back to main memory. To implement a copy-back cache with other cache tags, an additional RAM is required to save the dirty bits that signify if the data in the cache is different from that



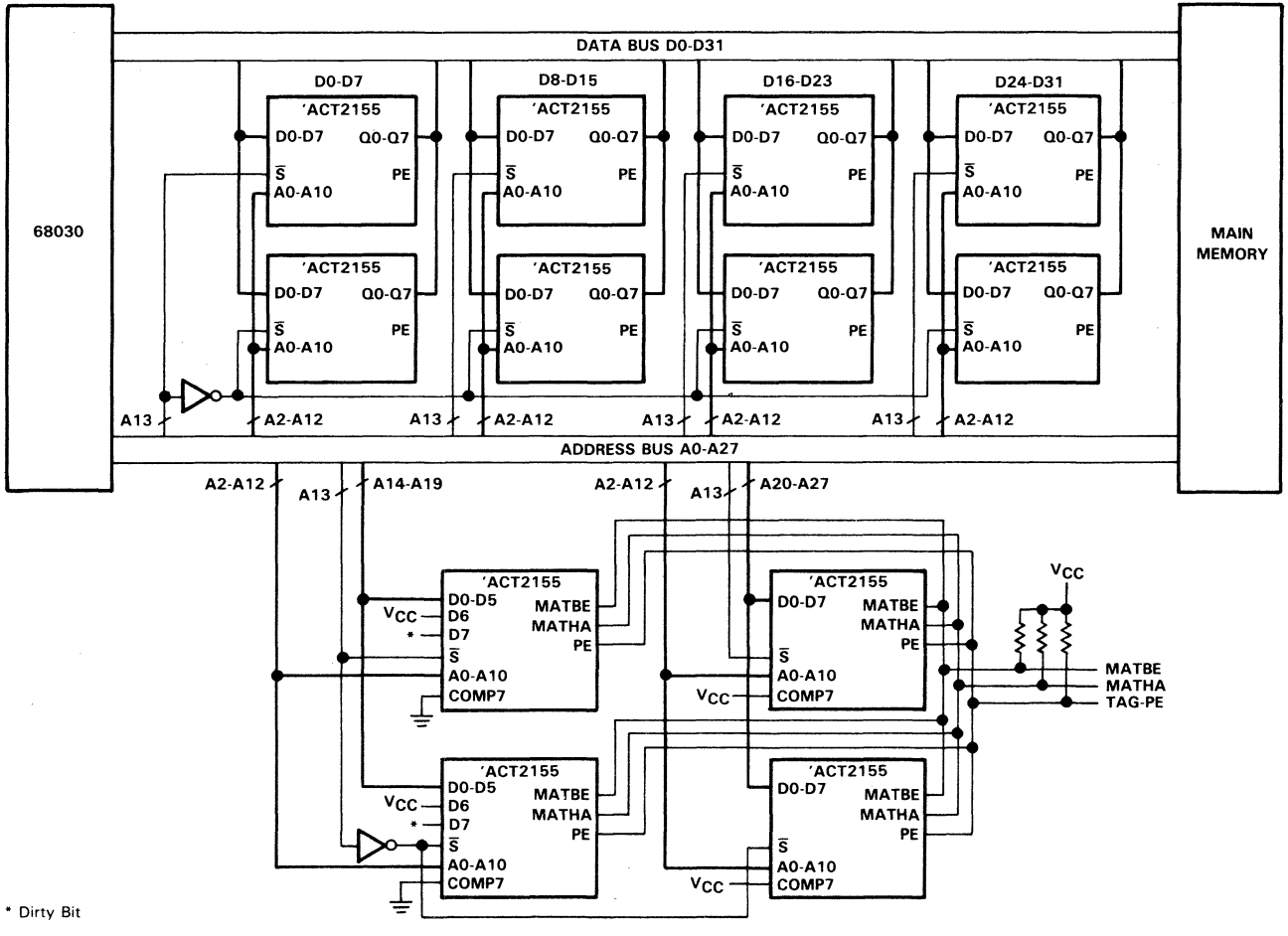
NOTES:
1. MC68030 requests a cache burst fill starting at long word 0. External cache acknowledges and provides a full burst fill. In this case all 4 long words needed to fill MC68030 cache were in the external cache. 4 long words were loaded into the MC68030 in 5 clock cycles.
2. MC68030 requests a cache burst fill starting at long word 2. External cache acknowledges and provides long word 2 and 3, but long word 0 is not in the external cache. The burst fill is terminated with MATBE (BERR). LWO is not cached in the MC68030.

Figure 11. MC68030 Burst Request with Data in External Cache



NOTES: 1. MC68030 requests burst fill of internal cache. A miss occurs in external cache. FMHB is taken high to prevent continuous rerun.
2. Four long words are loaded into a MC68030 cache and into the external cache.

Figure 12. MC68030 Burst Request with Data in Main Memory



* Dirty Bit

Figure 13. Cascading the SN74ACT2155

in main memory. Since the SN74ACT2155 incorporates these status bits internally, the need for extra RAM and additional logic is eliminated. When cascading the SN74ACT2155 for wider tags, the COMP7 input on the additional SN74ACT2155 devices can be tied high. This allows bits D7 and Q7 to be used in the tag comparison.

In Figure 14, the SN74ACT2155 is used to implement a copy-back cache for the MC68030 microprocessor. When the MC68030 requests data that is not in cache during either a regular or a burst mode access, the requested data is fetched from main memory and loaded into the MC68030. Simultaneously with the data being loaded into the microprocessor, it is written into the external cache and the corresponding dirty bits are set low. When the processor modifies and writes this data to memory, it is only written into the external cache and the corresponding dirty bit is set high. As long as the dirty bit remains high, additional writes to the same cache memory location can be accomplished without copying back the old data. When a cache miss occurs, the dirty bit output (Q7) is monitored. If the dirty bit is high, the addressed data and tag are latched before the new tag and data are written into cache.

The latching can be done while data is fetched from main memory. When the new data and tag are written into the cache, the dirty bit is again set low. The latched address and data are then sent to main memory to store the modified word. Bit D6 is used as a valid bit. Figure 15 shows an 8K-byte copy-back cache using the SN74ACT2155. When a copy-back cache system is designed, the question of data coherency must be addressed. The following paragraphs provide several solutions to the coherency problem.

Data Coherency

When a system is designed so that data can be stored in more than one memory, special consideration must be given to data coherency. The problem is that the data does not remain coherent or consistent in all memories. For example, in the copy-back cache system previously described, data can be written to cache without being written to main memory. When this occurs, the corresponding data in main memory becomes invalid and another device requesting data from main memory could receive invalid data.

There are several methods of solving the cache coherency problem. In a multiprocessor system, each microprocessor could have a private cache. Data stored in the cache would be used exclusively by its microprocessor. This allows a copy-back cache to be designed to reduce main-memory bus traffic and avoid data incoherency. When a processor requests data that is shared with other microprocessors, it must be fetched from main memory. If a large portion of data is shared between microprocessors, it is beneficial to put a shared cache in front of the main memory to improve system performance. This is shown in Figure 16.

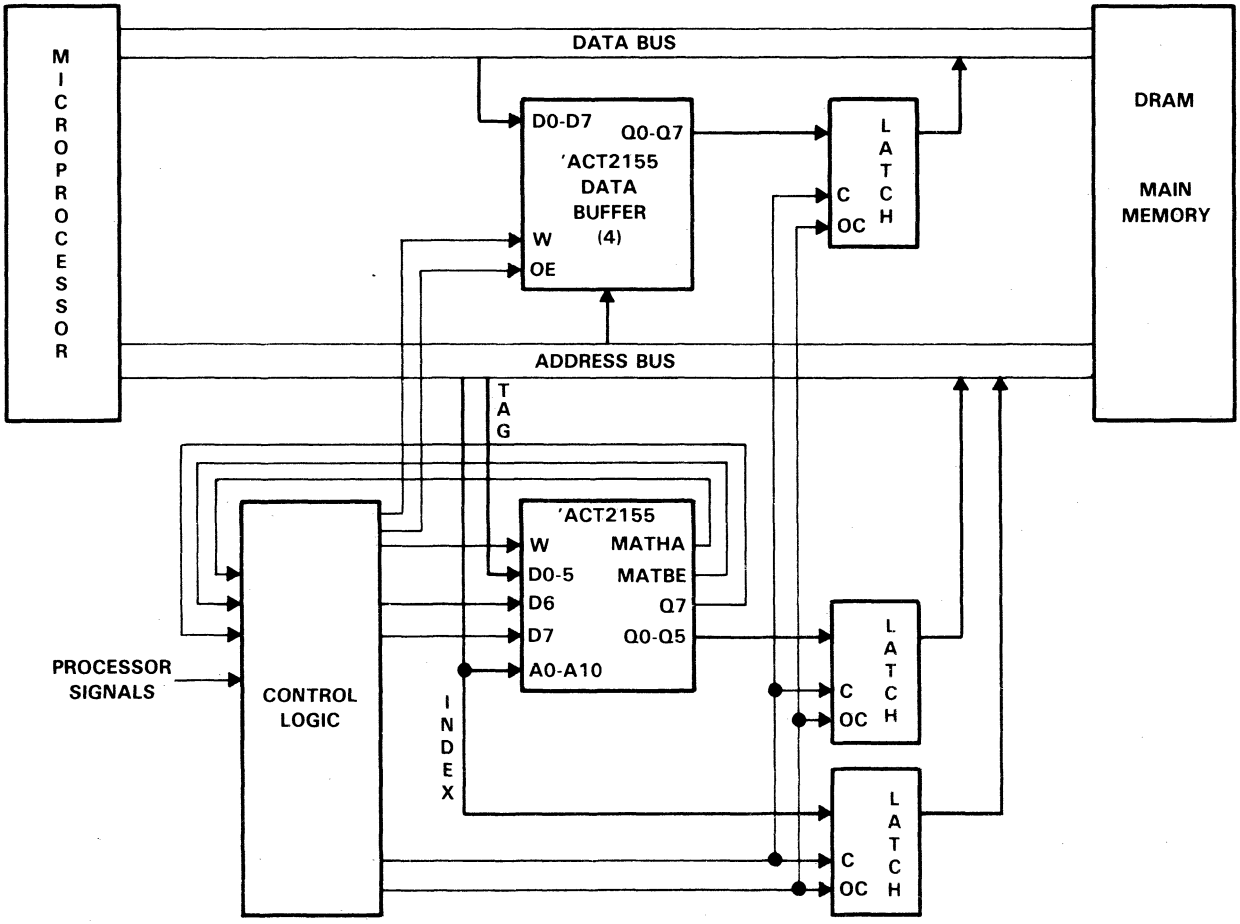


Figure 14. Copy-Back Cache Using the SN74ACT2155

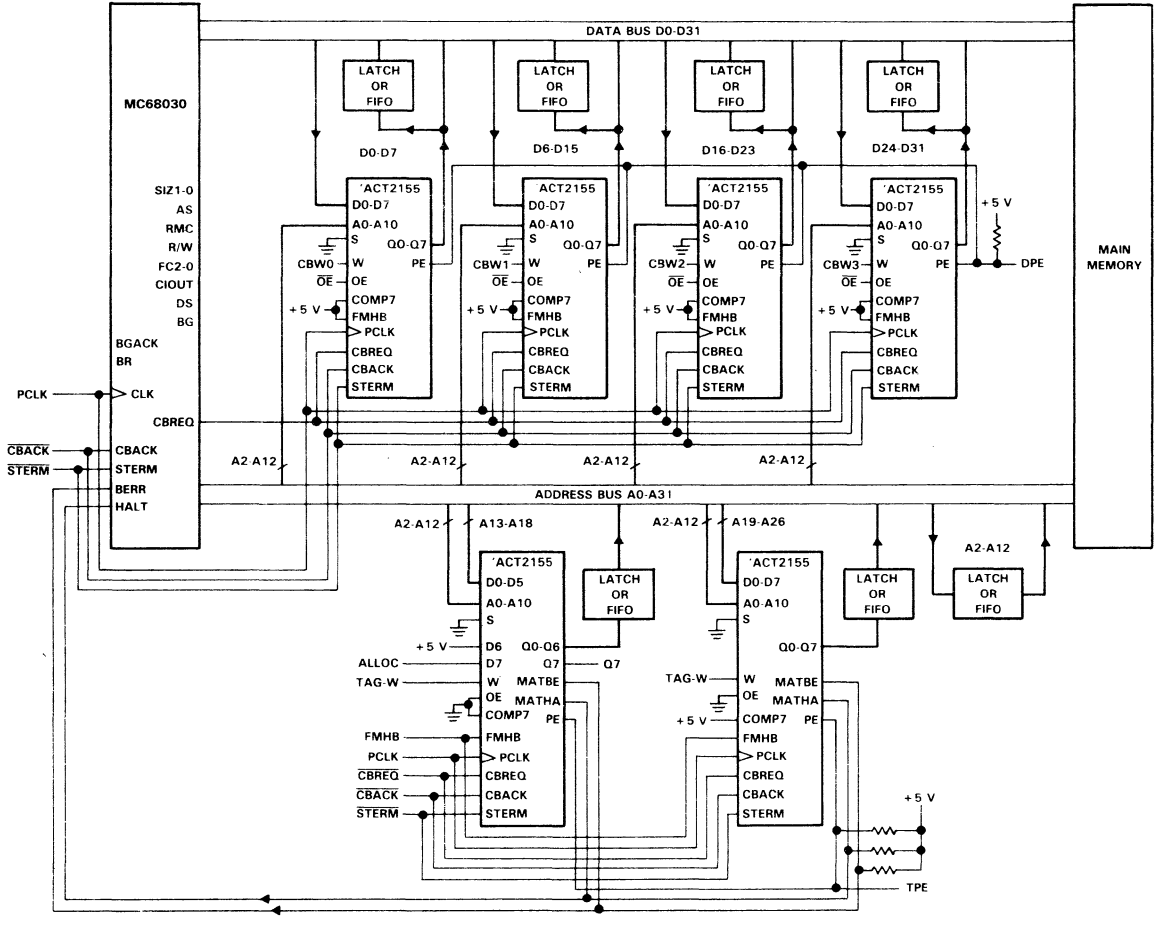


Figure 15. 8K-Byte Copy-Back Cache Configuration

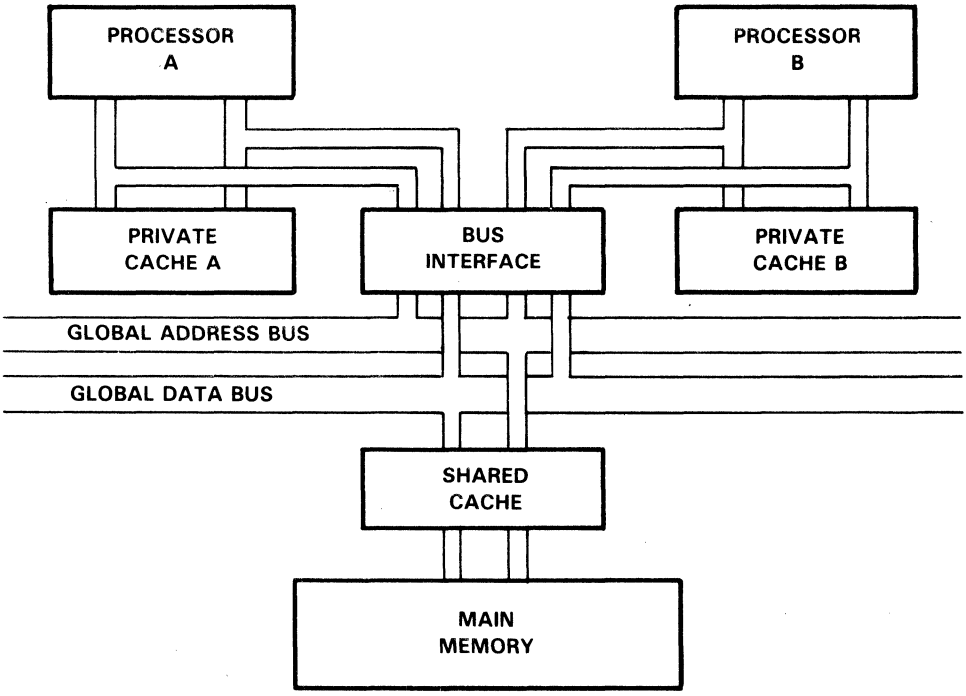


Figure 16. Private Caches as Coherency Solution. Shared Cache Used to Maintain Speed

Another method of solving the coherency problem is through the use of bus watching. With the SN74ACT2155, bus watching is performed by duplicating the tag portion of the cache and using the duplicate tag to monitor the main memory address bus rather than the microprocessor address bus. The bus watcher indicates a hit each time a cached address passes down the main-address bus. If data is being modified in main memory and a bus-watcher hit occurs, the index can be passed to the cache tag RAM for invalidation. When using a write-through cache, only main-memory writes would have to be monitored by the bus watcher to determine if invalidation is necessary. When using a copy-back cache, both main memory writes and reads would have to be monitored by the bus-watcher. By storing the dirty bits in the bus watcher tag RAM (in addition to the cache tag RAM), the dirty bit can be monitored at the same time as the match output. If a bus-watcher hit occurs during a main memory read and the corresponding dirty bit is high, the data must be fetched from the processor cache and not from main memory. Figure 17 shows a possible bus-watcher implementation.

When using the MC68030, the designer should not forget about data coherency with respect to the internal data and instruction caches. The standard method of handling MC68030 cache coherency is to load only nonshared data into the internal caches. The external cache can contain shared and/or unshared data depending on the coherency solution used.

Cache Control Logic for the SN74ACT2155

The control logic required for an SN74ACT2155 based cache can vary greatly depending upon how the cache is designed. Fast-programmable logic such as the TI 5-ns, 7-ns, or 10-ns programmable-array logic can be used for most of the cache control. In general, the cache control logic provides for writing the tag, writing data with byte control, decode for noncacheable addresses, rerun control to force MATBE and MATHA high and disable data outputs when a miss occurs, parity error detection, copy-back control (if used), bus watcher control (if used), resetting of tag RAMs to generate MC68030 input signals such as $\overline{\text{STERM}}$, $\overline{\text{CBACK}}$, BGACK, and BR and cache diagnostics as desired.

As discussed earlier in this report, the SN74ACT2155 has built-in circuits that provide for burst filling of the MC68030 internal caches and easy cache loading when data is retrieved from main memory. Recent Dhrystone benchmark studies have shown that a slight performance improvement may be achievable by disabling the burst operation when a cache hit occurs. System level simulation will provide the best data for deciding whether or not to burst out of cache. Regardless of the burst method used, the burst circuits of the SN74ACT2155 remain beneficial when loading blocks of four long words from main memory into cache. When bursting out of cache, it may be necessary to latch the cache data to ensure the MC68030 specification number 30, CLK low to Data-In Invalid (Synchronous Hold), is met. This specification should be compared to the SN74ACT2155 specification tv(8), Q0-Q7 valid time after PCLKv. The need for latching depends on which versions of the SN74ACT2155 and MC68030 are used. If necessary, the latches can be placed in parallel so that the MC68030 setup time, Data-In Valid to CLK low, is not violated.

The SN74ACT2155 uses the MC68030 retry mechanism to save 10 ns in the critical cache response path. This interface allows the MC68030 to perform two cycle reads out of cache. When a cache miss occurs, two clock cycles are added by utilizing the retry mechanism. Since a cache miss requires a main memory access, the control logic should be designed so that bus interface (bus arbitration) is performed during these two cycles. This will reduce or eliminate the two cycle penalty incurred through use of the retry mechanism.

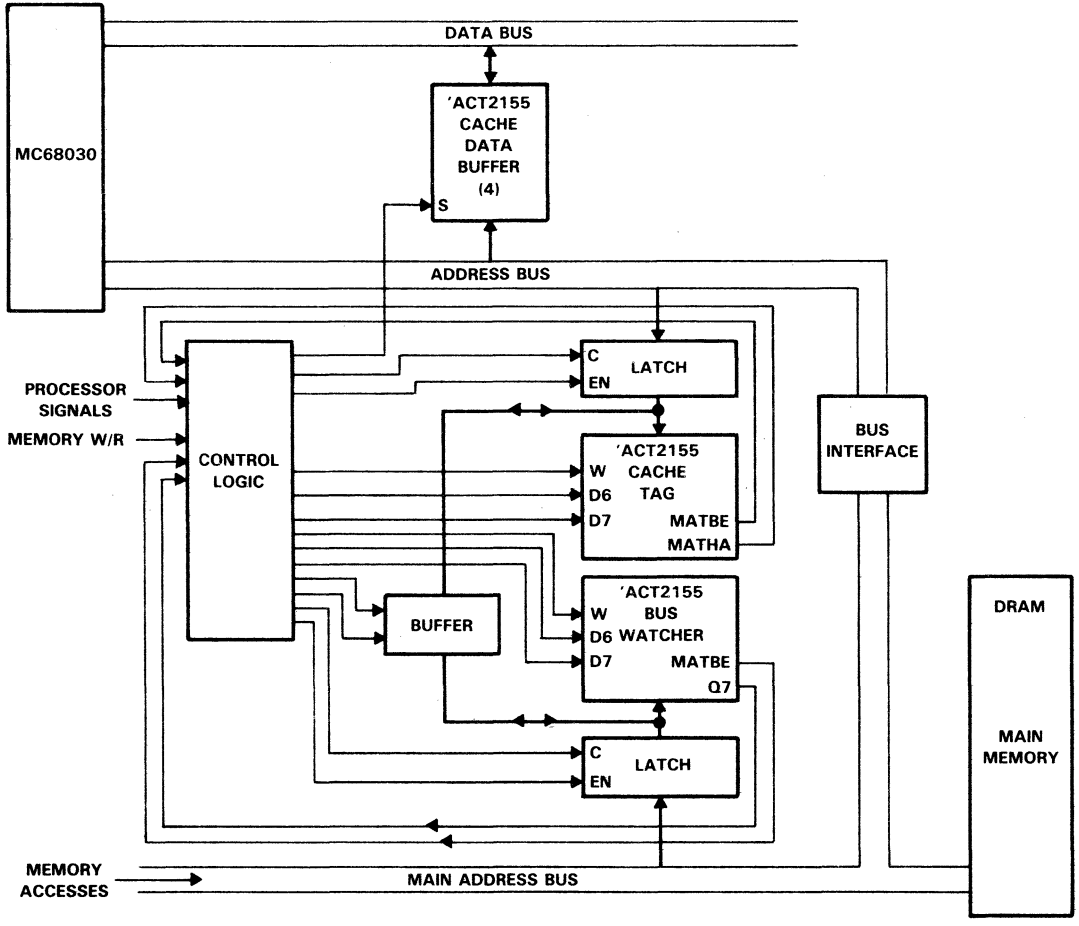


Figure 17. Bus Watching with the SN74ACT2155

Summary

This application report addressed the benefits associated with designing the SN74ACT2155 in a MC68030 based system.

The SN74ACT2155 is the first cache tag device that enables the MC68030 to run at maximum speed. By interfacing directly to the MC68030, it efficiently addresses the microprocessor cache burst-fill requirement and eliminates the unnecessary inclusion of wait states in a system design. Separate I/O ports allow the designer to configure the SN74ACT2155 as both the tag comparator and the SRAM data buffer in a total cache scheme that optimizes the MC68030 internal cache burst-fill requirement. In addition, this architecture serves as the basis for an efficient implementation of copy-back schemes. The performance improvement associated with copy-back schemes results from a considerable reduction in main memory traffic. The added benefit of incorporating dirty-bit storage capability in one chip further eliminates the need for extra RAM and additional control logic. Since the introduction of the SN74ACT2155, a denser version of this device has been introduced, the SN74ACT2156. The SN74ACT2155 and SN74ACT2156 provide the flexibility, density, and speed that is needed to configure a high-performance second level cache for MC68030 based systems.

Contents

Memory Timing Controllers

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Contents

Appendices

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List of Illustrations

Introduction

As processor and memory speeds increase, so do dynamic memory controller requirements. Typical processor speeds today range from 8 to 10 MHz. This increase in processor speed has created a need for faster memories, as well as faster memory timing controllers. The SN74ALS6301 and SN74ALS6302 are Memory Timing Controllers that are designed to meet the need of high performance memory systems.

In addition to offering better system performance, a faster memory controller typically allows the designer to use slower-rated dynamic random access memories (DRAMs). This results in significant cost savings because of the large number of DRAMs required. In other words, a faster dynamic memory controller can reduce overall dynamic memory costs.

The 'ALS6301 and 'ALS6302 feature address multiplexing, memory bank selection, and an address latch for systems which multiplex both data and address on the same bus. A row counter is provided for normal refresh operations. Column and bank counters are available for systems which use memory scrubbing.

This application note describes the functional operation of the 'ALS6301 and 'ALS6302 and shows how they can be interfaced to a typical processor. For illustration purposes, a simple timing controller generated from programmable logic is used to interface the 'ALS6301 to the microprocessor. The 'ALS6301 is interfaced with a Motorola 68000.

Memory Timing Controllers Using the SN54/74ALS6301, SN54/74ALS6302

Functional Description

The 'ALS6301 and 'ALS6302 are capable of controlling any DRAM up to 1M. The two devices typically operate in a read/write or a refresh mode. During normal read/write operations, the row and column addresses are multiplexed to the DRAM, and the corresponding $\overline{RAS}$ and $\overline{CAS}$ signals are activated to strobe the addresses into memory. In the refresh mode, the two counters cycle through the refresh addresses. If memory scrubbing is not being implemented, only the row counter is used. When memory scrubbing is being performed, both the row and column counters are used to perform read-modify-write cycles using an error detection and correction circuit such as the 'ALS632A. In this mode, all $\overline{RAS}$ outputs will be active (low) while only one $\overline{CAS}$ output is active at a time.

Two device types are offered to help simplify interfacing with the system dynamic timing controller. The 'ALS6301 offers active-low row address strobe input ($\overline{\text{RASI}}$) and column address strobe input ($\overline{\text{CASI}}$) signals, while the 'ALS6302 offers active-high RASI and CASI inputs. Figure 1 is a functional block diagram of the two devices.

Table 1 describes the four operating modes of the 'ALS6301 and 'ALS6302 as controlled by inputs MC0 and MC1. During normal read/write operations, the row and column addresses are multiplexed to the DRAM. When MSEL is high, the column address is selected; when MSEL is low, the row address is selected. The corresponding $\overline{\text{RAS}}$n and $\overline{\text{CAS}}$n output signals strobe the addresses into the selected memory bank or banks. A single 'ALS6301 or 'ALS6302 can control as many as four banks of 1M memory. Additional banks of memory can be controlled by using additional 'ALS6301 or 'ALS6302 devices and decoding each chip select ($\overline{\text{CS}}$) input.

Table 1. 'ALS6301, 'ALS6302 Mode-Control Function Table

SIGNAL		MODE SELECTED
MC1	MC0	
L	L	Refresh without Scrubbing. Refresh cycles are performed using the row counter to generate the addresses. In this mode, all four $\overline{\text{RAS}}$ outputs are active while the four $\overline{\text{CAS}}$ outputs remain high.
L	H	Refresh with Scrubbing/Initialize. Refresh cycles are performed using both the row and column counters to generate the addresses. MSEL selects the row or the column counter. All four $\overline{\text{RAS}}$ outputs go low in response to $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302), while only one $\overline{\text{CAS}}$n output goes low in response to $\overline{\text{CASI}}$ ('ALS6301) or CASI ('ALS6302). The bank counter keeps track of which $\overline{\text{CAS}}$ output goes active. This mode can also be used during system power-up so that the memory can be written with a known data pattern.
H	L	Read/Write. This mode is used to perform read/write cycles. Both the row and column addresses are multiplexed to the address output lines using MSEL. SEL0 and SEL1 are decoded to determine which $\overline{\text{RAS}}$n and $\overline{\text{CAS}}$n outputs will be active.
H	H	Clear Refresh Counters. This mode clears the three refresh counters (row, column, and bank) on the inactive transition of $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302), putting them at the beginning of the refresh sequence. In this mode, all four $\overline{\text{RAS}}$ outputs are driven low after the active edge of $\overline{\text{RASI}}$ ('ALS6301) or RASI ('ALS6302) so that DRAM wake-up cycles can also be performed.

In systems where addresses and data are both multiplexed onto a single bus, the 'ALS6301 and 'ALS6302 use latches (row, column, and bank) to hold the address information. The 22 input latches are transparent when the latch enable input (LE) is high; the input data is latched whenever LE goes low. For systems in which the processor has separate address and data buses, LE may be tied high.

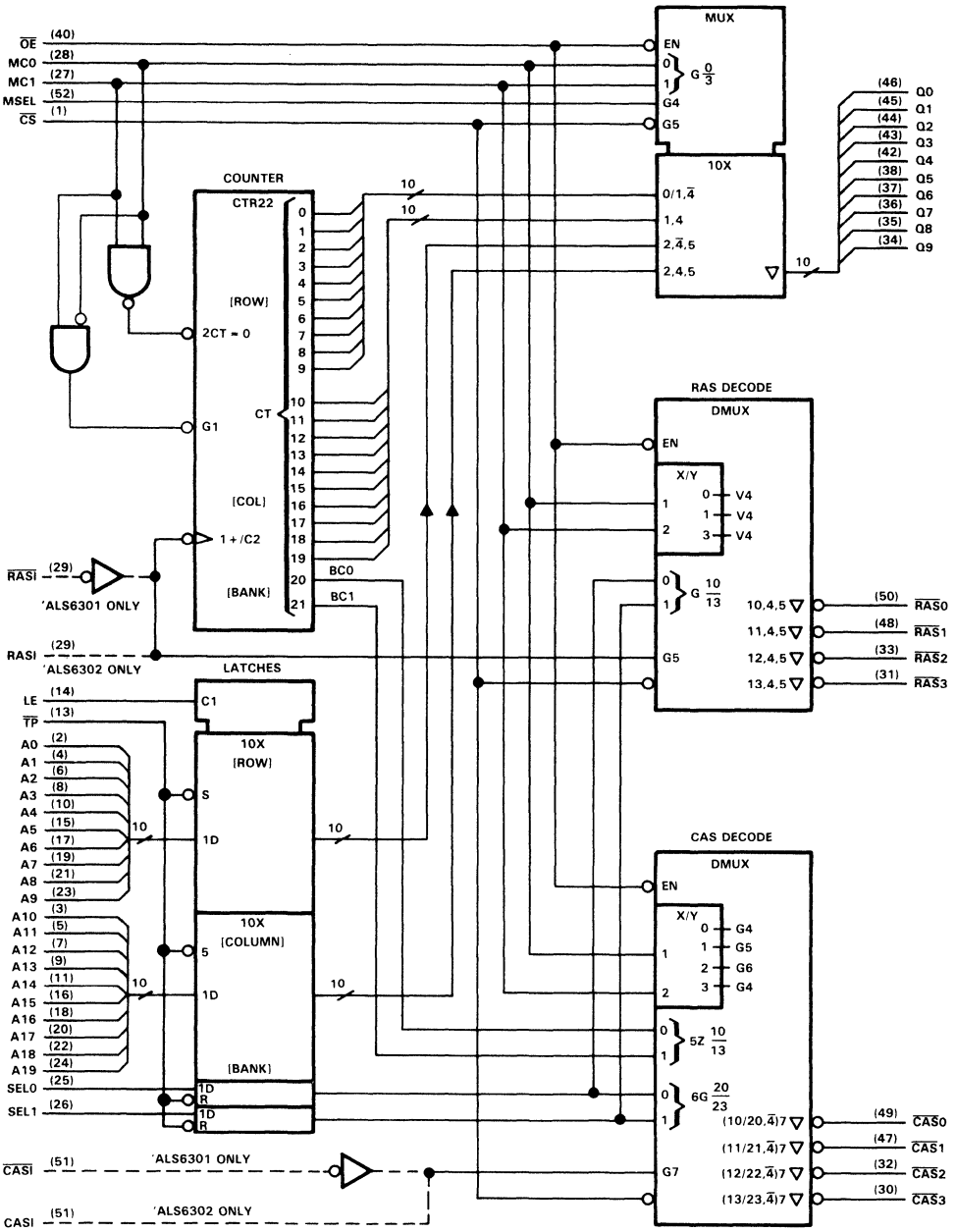


Figure 1. 'ALS6301, 'ALS6302 Functional Block Diagram

The two 10-bit counters in the 'ALS6301 and 'ALS6302 support 128, 256, and 512 line refresh operations. Transparent, burst, synchronous, or asynchronous refresh modes are all possible as determined by the memory timing controller. The refresh counters are advanced on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301, and on the high-to-low transition of RASI on the 'ALS6302. This is true in either refresh mode. In the clear refresh counter mode, the refresh counters (row, column, and bank) can be reset to zero on the low-to-high transition of $\overline{\text{RASI}}$ on the 'ALS6301 or on the high-to-low transition of RASI on the 'ALS6302.

Typical Implementation

Figure 2 shows a system interface using the 'ALS6301 between a Motorola 68000L10 and four banks of 1M DRAMs. Addresses A21 and A22 are used to select one of the four memory banks. Since members of the 68000 processor family have separate address and data busses, the input latches on the 'ALS6301 are left transparent by tying the latch

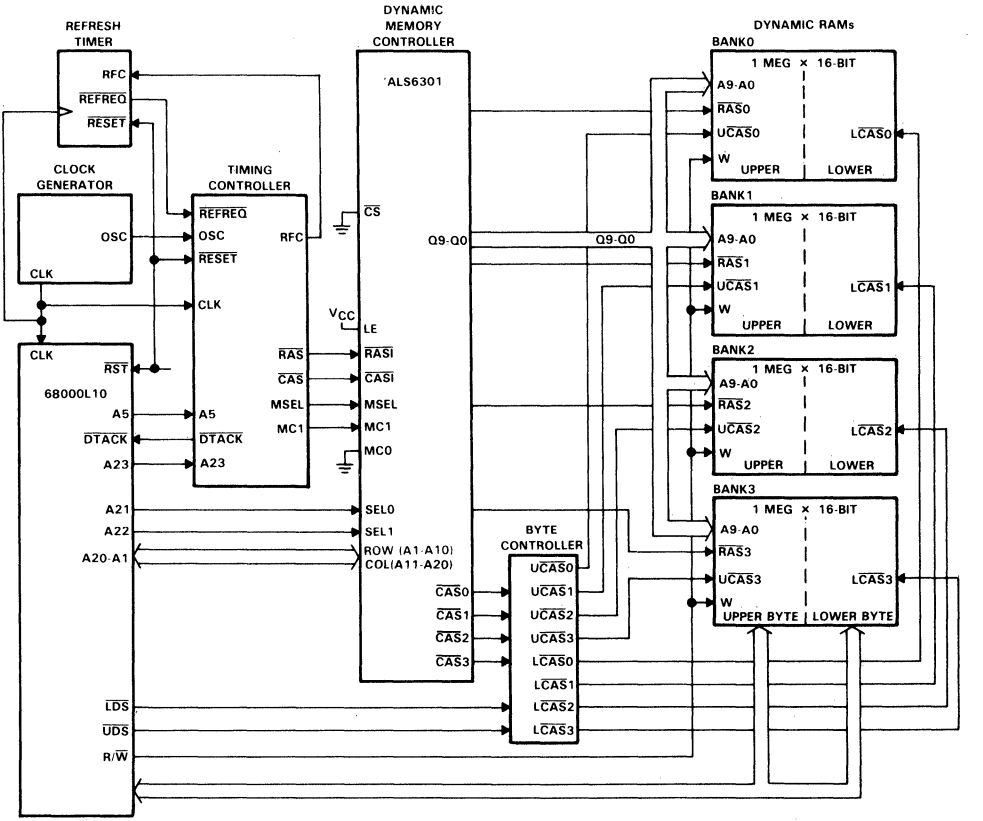


Figure 2. 'ALS6301, 'ALS6302 Timing Controller Interface

enable (LE) input high. The $\overline{CAS0}$ thru $\overline{CAS3}$ outputs of the 'ALS6301 are fed into the byte controller along with processor signals $\overline{LDS}$ and $\overline{UDS}$. The byte controller made from programmable logic allows the processor to determine whether upper, lower, or both bytes are accessed.

The $\overline{RASI}$, $\overline{CASI}$, MSEL and mode control (MC0, MC1) inputs on the 'ALS6301 must be generated by the memory timing controller. The memory timing controller functions as an arbitrator between refresh cycles and 68000L10 access cycles. It also guarantees that timing requirements of the DRAM will be met.

Timing Controller Details

Figure 3 is a timing diagram for a typical 68000L10 access cycle. The 'ALS6301 control signals required to execute the access cycle are also shown. Control signals for the 'ALS6301 are referenced from the OSC output of the 8284A clock generator. OSC runs at 2 times the speed of the system clock, that is CLK = 10 MHz and OSC = 20 MHz. By running the timing controller at a higher speed than the system clock, the system performance is improved. A programmable logic sequencer, the TIB82S167B, is programmed for use as the timing controller.

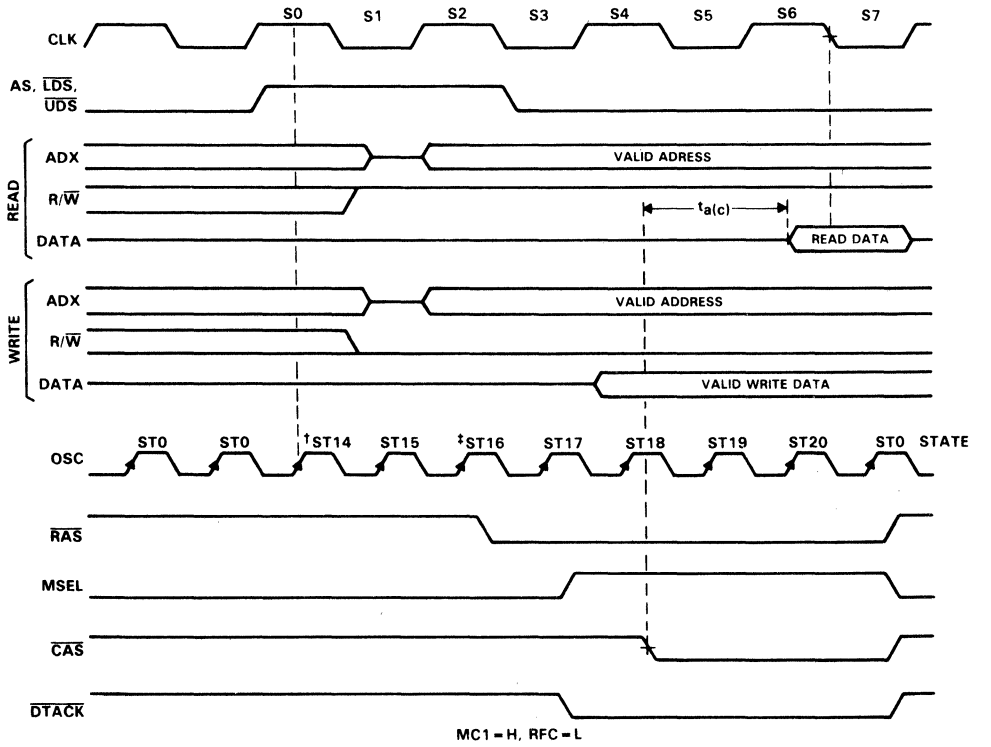
In this example, refresh requests ($\overline{REFREQ}$) are generated every 155 clock cycles. The timing controller will perform the refresh cycle ($\overline{RAS}$ only) immediately if the processor is not in the middle of an access cycle. If the controller is in the middle of an access cycle, the refresh cycle will be delayed until the access cycle is complete. If the controller is asked to perform an access cycle during a refresh, the access cycle will begin immediately after the refresh cycle is completed. Address bit A23 indicates whether the access requested is a memory access (A23 = L) or an I/O access (A23 = H). The timing controller will perform an access cycle only if Address bit A23 is low. Figure 4 is a timing diagram of the refresh/access cycle as explained above. To implement memory scrubbing, the controller must execute a read/write cycle during the refresh cycle and then place the 'ALS6301 in the memory scrubbing mode. (This example executes a $\overline{RAS}$ only refresh.) The flowchart in Figure 5 outlines the required functionality of the timing controller. This flowchart was used along with the timing diagrams in Figures 3 and 4 to design the timing controller.

Refresh Timer Details

Figure 6 shows the actual circuit implementation of the refresh and memory timing controller. The refresh timer signals the controller whenever it is time to execute a refresh cycle. As required by memory, every row (512 on the TMS4C1025 DRAM) must be addressed every 8 ms. This implies that one row should be refreshed at least once every 15.6 ms. With a 10-MHz system clock, the refresh timer should use approximately a division factor of 155. This results in a refresh request every 15.3 ms. The refresh complete

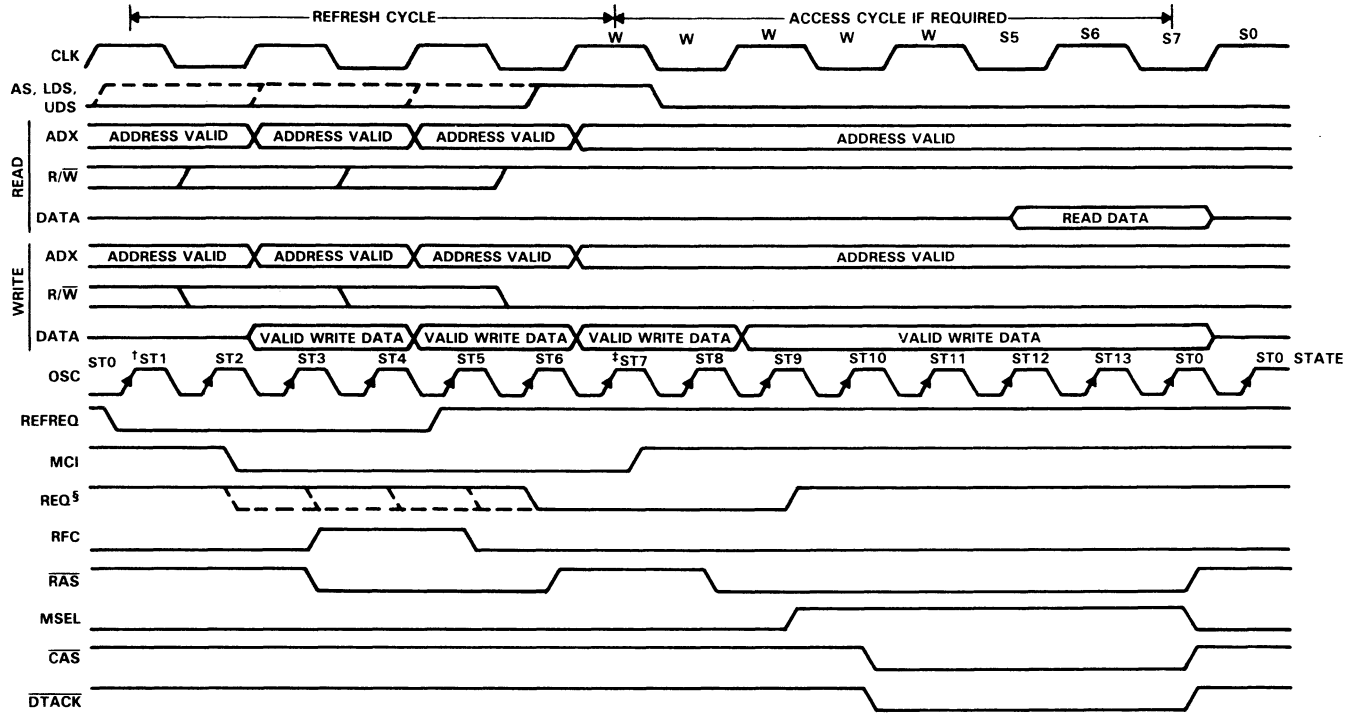
input (RFC) is used to signal the refresh timer that the refresh has been completed. It is important that the timer not stop so that the 8 ms memory requirement is maintained.

The TIBPAL22V10 circuit shown in Figure 6 is used to generate the refresh request signal every 155 clock cycles. The refresh request signal (active low) will remain active (low) until a refresh complete (RFC) signal is received from the timing controller. During a system reset, the refresh request output is set to a high logic level. When using different clock rates or memory sizes, the division circuit in the refresh timer should be adjusted accordingly.



†Start sequence when AS = H, CLK = H, $\overline{\text{REFREQ}}$ = H, STATE = 0
‡Return to ST0 if A23 is high

Figure 3. MC68000 Access Cycle



† Start sequence when $\overline{\text{REFREQ}}$ = L, STATE = 0

‡ Return to STATE 0 if REQ = H or A23 = H

§ REQ is internal status register used to store an access request during a refresh cycle. (If AS = H during refresh cycle ST1-ST5)

Figure 4. Refresh/Access Cycle

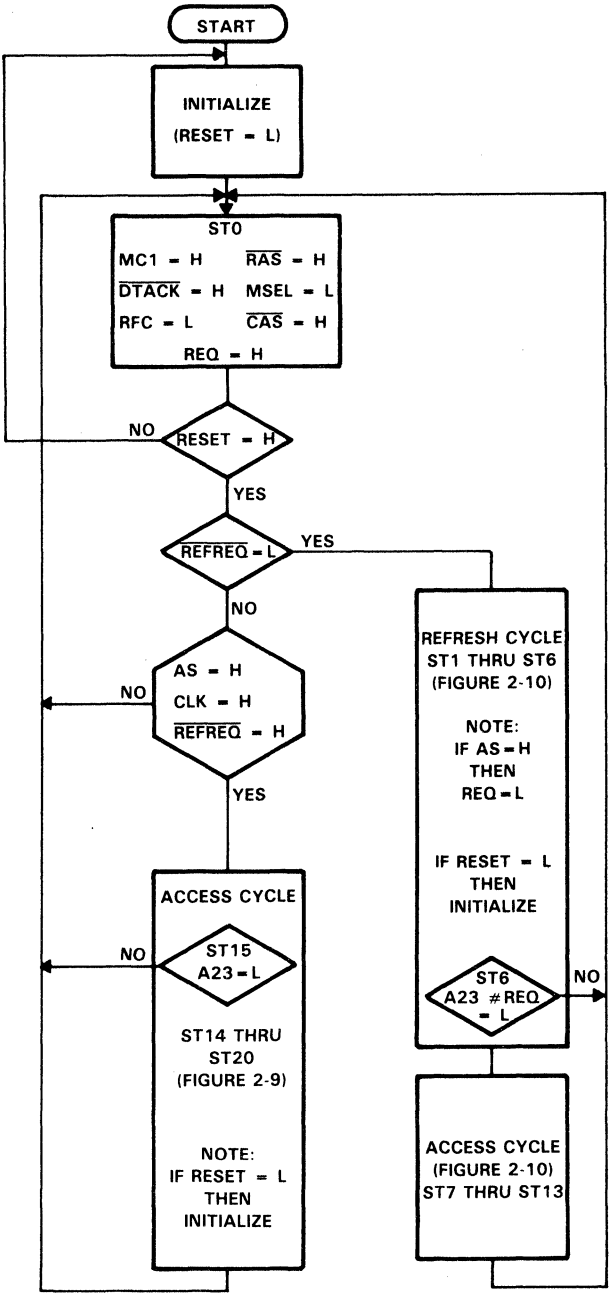


Figure 5. 'ALS6301, 'ALS6302 Memory Timing Controller Flowchart

Programmable Logic Designs

As mentioned previously, the timing controller, byte controller, and the refresh timer used in this example are created using programmable logic. ABEL™ and CUPL™ software packages have been used to reduce equations and generate the fuse maps needed to program these devices. The files used to generate the fuse maps have been included for reference at the end of this application report. Test vectors are included with the device files so software simulation can be performed on the computer. If the proper instruction is provided, the software will attach the test vectors to the end of the fuse map. This allows programming equipment to run a functional test on each device immediately after programming. To help familiarize the reader with these software tools, the timing controller design is done in both ABEL™ and CUPL™.

The TIB82S167B field programmable sequencer shown in Figure 6 is configured as a state machine to execute the flow chart shown in Figure 5. As shown in the flowchart, the timing controller is initialized by taking the reset input low. From the initialization state, state 0, the timing controller can perform either an access or a refresh cycle depending on the signals AS, CLK, and $\overline{\text{REFREQ}}$. If an access is requested (AS = H) during a refresh cycle, an internal status register, REQ, will flag the request and as soon as the refresh cycle is completed, an access cycle will be started. At the start of an access cycle, the timing controller checks the state of the A23 address bit. If A23 is high, indicating an I/O access, the timing controller terminates the access cycle and returns to state 0.

As seen in Figures 3, 4, and 5, a state, ST0-ST30, has been assigned to each clock cycle. The appended ABEL™ and CUPL™ files can be easily understood by comparing the state equations to the states shown in these figures. Since the only difference between the 'ALS6301 and the 'ALS6302 is that the $\overline{\text{RASI}}$ and the $\overline{\text{CASI}}$ inputs are active-high instead of active-low, a slight modification to the timing controller software file will allow an 'ALS6302 to be used instead of an 'ALS6301. The TIBPAL22V10 refresh timer and the TIBPAL16L8 byte controller designs are straight forward and easily achieved as can be seen in the appended files.

In applications with different systems timings, the ABEL™ and CUPL™ files can be modified to fit the processor requirements. For additional information concerning timing controller, refresh timer, and byte controller, contact the Datapath VLSI Products (DVP) Applications group at (214) 997-5762. If a basic understanding of programmable logic is needed, see the Texas Instruments Programmable Logic Data Book.

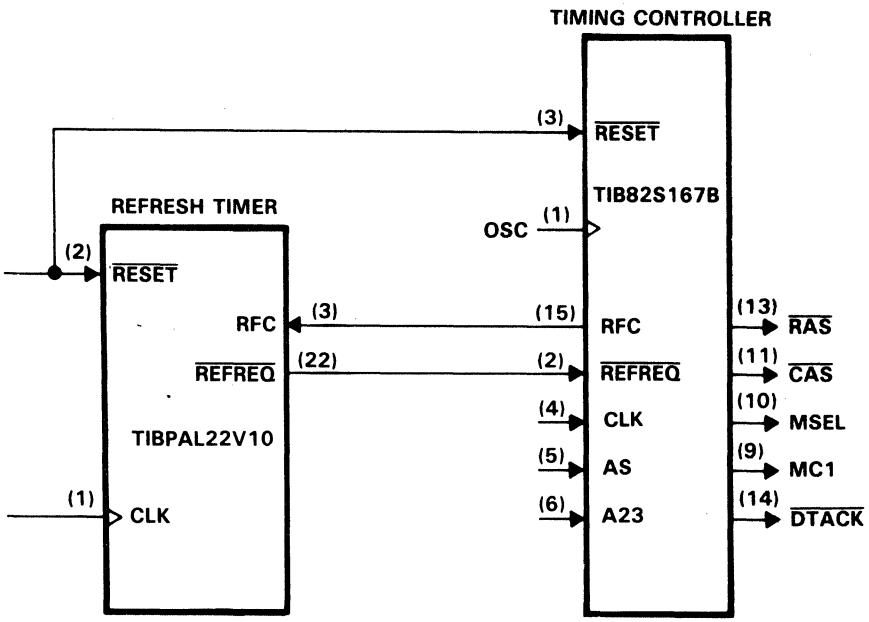


Figure 6. Refresh/Memory Timing Controller

Summary

The 'ALS6301 and 'ALS6302, coupled with programmable logic, offer the system designer a solution to high-speed dynamic memory requirements. Programmable logic allows the designer to tailor the timing controller to a selected processor and memory. In many cases, the generation of a high-speed timing controller from programmable logic will allow the designer to use slower DRAMs without affecting system speed. This results in lower total system cost because of the large number of memory devices used.

Appendix A

ABEL™ Files

module DMC S167

```
module DMC_S167 flag '-KY','-R2' "leave unused OR terms connected
title 'DYNAMIC MEMORY CONTROLLER FOR THE ALS6301 APPLICATION
Loren Schiele   Texas Instruments,  August 15, 1986'

        DMC  device 'F82S167';

" Input pin assignments

OSC     pin   1;                        " OSCILLATOR
REFREQ  pin   2;                        " REFRESH REQUEST
RESET   pin   3;                        " RESET - INITIALIZES WHEN LOW
CLK     pin   4;                        " OSC DIVIDED BY 2
AS      pin   5;                        " ADDRESS STROBE
A23     pin   6;                        " MOST SIGNIFICANT ADDRESS BIT
GND     pin  16;                        " PIN 16 MUST BE TIED LOW

" Output pin and node assignments

MC1     pin   9;  MC1_R    node 25;     " MODE CONTROL
MSEL    pin  10;  MSEL_R   node 26;     " MULTIPLEXER SELECT
CAS     pin  11;  CAS_R    node 27;     " COLUMN ADDRESS STROBE
RAS     pin  13;  RAS_R    node 28;     " ROW ADDRESS STROBE
DTACK   pin  14;  DTACK_R  node 29;     " DATA ACKNOWLEDGE
RFC     pin  15;  RFC_R    node 30;     " REFRESH COMPLETE

" Internal status and counter nodes

P0      node 36;  P0_R     node 42;     " INTERNAL COUNTER REGISTER
P1      node 35;  P1_R     node 41;     " INTERNAL COUNTER REGISTER
P2      node 34;  P2_R     node 40;     " INTERNAL COUNTER REGISTER
P3      node 33;  P3_R     node 39;     " INTERNAL COUNTER REGISTER
P4      node 32;  P4_R     node 38;     " INTERNAL COUNTER REGISTER
REQ     node 31;  REQ_R    node 37;     " REFRESH REQUEST STATUS REGISTER

" Define Set and Reset inputs to output and status flip-flops
MC1_    = [MC1,MC1_R];
MSEL_   = [MSEL,MSEL_R];
CAS_    = [CAS,CAS_R];
RAS_    = [RAS,RAS_R];
DTACK_  = [DTACK,DTACK_R];
RFC_    = [RFC,RFC_R];
REQ_    = [REQ,REQ_R];

" 'high' and 'low' are used to set or reset the output and status
"  registers.  Example: MC1_ := high & RESET; will cause pin 9 to
"  go high on the next clock edge if input pin 3 is high.

high    = [ 1,  0];
low     = [ 0,  1];
Count   = [P4,P3,P2,P1,P0];             " STATE REGISTER SET DEFINED
Cnt     = [P4,P3,P2,P1,P0];             " STATE REGISTER SET DEFINED
H,L,clk,X = 1, 0, .C., .X.;
```

```
state_diagram Count                                    " NEXT
        State 0:        case                           " STATE
                         !REFREQ   & RESET              : 1;
                          REFREQ   & AS & CLK & RESET   :14;
                          REFREQ   & (!AS # !CLK)       : 0;
                        endcase;

" REFRESH TIMING CYCLE
        State 1:        MC1_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1              : 2; endcase;
        State 2:        RFC_  := high & RESET;
                        RAS_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1              : 3; endcase;
        State 3:        REQ_  := low  & (AS & RESET);
                        case     RESET==1              : 4; endcase;
        State 4:        RFC_  := low  & RESET;
                        REQ_  := low  & (AS & RESET);
                        case     RESET==1              : 5; endcase;
        State 5:        RAS_  := high;
                        REQ_  := low  & (AS & RESET);
                        case     RESET == 1            : 6; endcase;

" DETERMINE IF ACCESS HAS BEEN REQUESTED
        State 6:        REQ_  := high & A23;
                        MC1_  := high & RESET;
                        case     REQ # A23             : 0;
                                !A23  & !REQ & RESET   : 7;
                        endcase;

" ACCESS AFTER REFRESH
        State 7:        RAS_  := low  & RESET;
                        case     RESET==1              : 8; endcase;
        State 8:        REQ_  := high & RESET;
                        MSEL_ := high & RESET;
                        case     RESET==1              : 9; endcase;
        State 9:        CAS_  := low  & RESET;
                        DTACK_:= low  & RESET;
                        case     RESET==1              :10; endcase;
        State 10:       case     RESET==1              :11; endcase;

        State 11:       case     RESET==1              :12; endcase;

        State 12:       case     RESET==1              :13; endcase;

        State 13:       RAS_  := high;
                        MSEL_ := low;
                        CAS_  := high;
                        DTACK_:= high;
                        case     RESET==1              : 0; endcase;
@page
```

```
" ACCESS TIMING CYCLE
        State 14:       case     RESET==1                :15; endcase;
        State 15:       RAS_  := low  & !A23 & RESET;
                        case A23 == 1                    : 0;
                             !A23 & RESET                :16;
                        endcase;
        State 16:       MSEL_ := high & RESET;
                        DTACK_:= low  & RESET;
                        case     RESET==1                :17; endcase;
        State 17:       CAS_  := low  & RESET;
                        case     RESET==1                :18; endcase;
        State 18:       case     RESET==1                :19; endcase;
        State 19:       case     RESET==1                :20; endcase;
        State 20:       RAS_  := high;
                        MSEL_ := low;
                        CAS_  := high;
                        DTACK_:= high;
                        case     RESET==1                : 0; endcase;

equations
        enable MC1 = 1;  "always enabled, pin 19 is preset

" INITIALIZATION WHEN RESET IS LOW
        [ MC1,RAS,DTACK,REQ,CAS]                  :=  !RESET;
        [ P0_R,P1_R,P2_R,P3_R,P4_R,MSEL_R,RFC_R] :=  !RESET;

test_vectors ' REFRESH WITH ACCESS FOLLOWING'

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 1, X ] -> [ L ,  L , H , H ,  H  , L , L , 2 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , H , L , 3 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , H , L , 4 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , L ,  H  , L , L , 5 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , H ,  H  , L , L , 6 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , H ,  H  , L , L , 7 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , L ,  H  , L , L , 8 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  H  , L , H , 9 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,10 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,11 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,12 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,13 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' REFRESH WITHOUT ACCESS FOLLOWING'

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , H ,  H  , L , H , 2 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , H , 3 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , H , 4 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , L , H , 5 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ L ,  L , H , H ,  H  , L , H , 6 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
@page
```

```
test_vectors ' REFRESH WITH ACCESS REQUEST BUT DATA NOT IN DRAM (A23=H) '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   0  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 1 ];
 [ 0 ,clk,  1  ,   X  , X , 1, X ] -> [ L ,  L , H , H ,  H  , L , L , 2 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , L , 3 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , H , L , 4 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , L ,  H  , L , L , 5 ];
 [ 0 ,clk,  1  ,   X  , X , 0, X ] -> [ L ,  L , H , H ,  H  , L , L , 6 ];
 [ 0 ,clk,  1  ,   X  , X , 0, 1 ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' ACCESS TIMING CYCLE '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , L ,  H  , L , H ,16 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  L  , L , H ,17 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,18 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,19 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,20 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' ACCESS TIMING CYCLE BUT DATA NOT IN DRAM (A23=H) '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 1 ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 0 , 0, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

test_vectors ' RESET DURING ACCESS TIMING CYCLE '

([GND,OSC,RESET,REFREQ,CLK,AS,A23] -> [MC1,MSEL,CAS,RAS,DTACK,RFC,REQ,Cnt])
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  1  ,   1  , 1 , 1, X ] -> [ H ,  L , H , H ,  H  , L , H ,14 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H ,15 ];
 [ 0 ,clk,  1  ,   X  , X , X, 0 ] -> [ H ,  L , H , L ,  H  , L , H ,16 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , H , L ,  L  , L , H ,17 ];
 [ 0 ,clk,  1  ,   X  , X , X, X ] -> [ H ,  H , L , L ,  L  , L , H ,18 ];
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];
 [ 0 ,clk,  0  ,   X  , X , X, X ] -> [ H ,  L , H , H ,  H  , L , H , 0 ];

end DMC_S167
```

module TIMER154

```
module  TIMER154 flag '-r2','-f'
title  'REFRESH TIMER
        LOREN SCHIELE  TEXAS INSTRUMENTS, DALLAS, 08/15/86'

        T154  DEVICE   'P22V10';

"input declarations

CLK    .       pin 1;              "  SYSTEM CLOCK
RESET          pin 2;              "  RESETS WHEN LOW
RFC            pin 3;              "  REFRESH COMPLETE

"output declarations

Q0,Q1,Q2,Q3    pin 14,15,16,17;    "  COUNTER STATES
Q4,Q5,Q6,Q7    pin 18,19,20,21;    "  COUNTER STATES
REFREQ_        pin 22;             "  REFRESH REQUEST - ACTIVE LOW

"intermediate variables

CNT_154_   =  !Q0 & Q1 & !Q2 & Q3 & Q4 & !Q5 & !Q6 & Q7;
SCLR       =  !RESET # CNT_154_;
count      = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
C,H,L,X    = .C.,1,0,.X.;

equations

REFREQ_   :=  RFC # !CNT_154_ &  REFREQ_ # !RESET;
Q0        :=  (!Q0 ) & !SCLR;
Q1        :=  ( Q1 $  Q0) & !SCLR;
Q2        :=  ( Q2 $  Q1 &  Q0) & !SCLR;
Q3        :=  ( Q3 $ (Q2 &  Q1 &  Q0)) & !SCLR;
Q4        :=  ( Q4 $ (Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q5        :=  ( Q5 $ (Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q6        :=  ( Q6 $ (Q5 &  Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;
Q7        :=  ( Q7 $ (Q6 &  Q5 &  Q4 &  Q3 &  Q2 &  Q1 &  Q0)) & !SCLR;

test_vectors              ([RESET,CLK,RFC] -> [count,REFREQ_])
                           [  0  , C , 0 ] -> [  0  ,   H   ];
@CONST cnt = 1;
@REPEAT 154 {              [  1  , C , 0 ] -> [ cnt ,   H   ];
@CONST cnt = cnt + 1;}
                           [  1  , C , 0 ] -> [  0  ,   L   ];
@CONST cnt = 1;
@REPEAT 20  {              [  1  , C , 0 ] -> [ cnt ,   L   ];
@CONST cnt = cnt + 1;}
                           [  1  , C , 1 ] -> [ 21   ,   H   ];
                           [  1  , C , 0 ] -> [ 22   ,   H   ];
                           [  1  , C , X ] -> [ 23   ,   H   ];
                           [  0  , C , X ] -> [  0   ,   H   ];
end TIMER154
```

Appendix B

CUPL™ Files

DYNAMIC MEMORY CONTROLLER

```
Partno          DMC-S167;
Name            DMC-S167;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*                  DYNAMIC MEMORY CONTROLLER                    */
/*                        FOR ALS6301                            */
/*****************************************************************/
/* Allowable Target Device Types: TIB82S167B                     */
/*****************************************************************/

/**  Inputs  **/
pin 1 =  OSC;              /*  OSCILLATOR                       */
pin 2 = REFREQ;            /*  REFRESH REQUEST                  */
pin 3 = RESET;             /*  RESET - INITIALIZES WHEN LOW     */
pin 4 = CLK;               /*  OSC DIVIDED BY 2                 */
pin 5 = AS;                /*  ADDRESS STROBE                   */
pin 6 = A23_;              /*  MOST SIGNIFICANT ADDRESS BIT     */
pin 16 = GND;              /*  PIN 16 MUST BE TIED LOW          */

/**  Outputs  **/
pin  9 = MC1_;             /*  MODE CONTROL                     */
pin 10 = MSEL;             /*  MULTIPLEXER SELECT               */
pin 11 = CAS;              /*  COLUMN ADDRESS STROBE            */
pin 13 = RAS;              /*  ROW ADDRESS STOBE                */
pin 14 = DTACK;            /*  DATA ACKNOWLEDGE                 */
pin 15 = RFC;              /*  REFRESH COMPLETE                 */

/** Internal Node Group  -   State bits declared as nodes      **/
node [REQ,P4_,P3_,P2_,P1_,P0_];

/** Declarations and Intermediate Variable Definitions         **/
Field State  = [P4_,P3_,P2_,P1_,P0_];

$define  ST0 'b'00000
$define  ST1 'b'00001
$define  ST2 'b'00010
$define  ST3 'b'00011
$define  ST4 'b'00100
$define  ST5 'b'00101
$define  ST6 'b'00110
$define  ST7 'b'00111
$define  ST8 'b'01000
$define  ST9 'b'01001
$define ST10 'b'01010
$define ST11 'b'01011
$define ST12 'b'01100
$define ST13 'b'01101
$define ST14 'b'01110
$define ST15 'b'01111
$define ST16 'b'10000
$define ST17 'b'10001
$define ST18 'b'10010
$define ST19 'b'10011
$define ST20 'b'10100
```

```
/** Logic Equations **/

Sequence State
(Present ST0 IF  RESET & !REFREQ             NEXT ST1;
             IF  RESET &  REFREQ & AS & CLK NEXT ST14;
             DEFAULT                         NEXT ST0;

/*  REFRESH TIMING CYCLE */
Present ST1 IF  AS & RESET  NEXT ST2  OUT [!MC1_,!REQ];
            IF  RESET       NEXT ST2  OUT [!MC1_];
Present ST2 IF  AS & RESET  NEXT ST3  OUT [ RFC,!RAS,!REQ];
            IF  RESET       NEXT ST3  OUT [ RFC,!RAS];
Present ST3 IF  AS & RESET  NEXT ST4  OUT [!REQ];
            IF  RESET       NEXT ST4;
Present ST4 IF  AS & RESET  NEXT ST5  OUT [!RFC,!REQ];
            IF  RESET       NEXT ST5  OUT [!RFC];
Present ST5 IF  AS & RESET  NEXT ST6  OUT [ RAS,!REQ];
            IF  RESET       NEXT ST6  OUT [ RAS];
/** DETERMINE IF ACCESS HAS BEEN REQUESTED **/
Present ST6 IF  A23_ # REQ  NEXT ST0  OUT [ MC1_,REQ];
            IF !A23_ & RESET & !REQ NEXT ST7 OUT [ MC1_];

/** ACCESS AFTER REFRESH **/
Present ST7  IF  RESET       NEXT ST8  OUT [!RAS];
Present ST8  IF  RESET       NEXT ST9  OUT [ REQ, MSEL];
Present ST9  IF  RESET       NEXT ST10 OUT [!CAS,!DTACK];
Present ST10 IF  RESET       NEXT ST11;
Present ST11 IF  RESET       NEXT ST12;
Present ST12 IF  RESET       NEXT ST13;
Present ST13                 NEXT ST0  OUT [ RAS,!MSEL, CAS, DTACK];

/** ACCESS TIMING CYCLE **/
Present ST14 IF  RESET       NEXT ST15;
Present ST15 IF  A23_        NEXT ST0;
             IF !A23_ & RESET NEXT ST16 OUT [!RAS];
Present ST16 IF  RESET       NEXT ST17 OUT [ MSEL,!DTACK];
Present ST17 IF  RESET       NEXT ST18 OUT [!CAS];
Present ST18 IF  RESET       NEXT ST19;
Present ST19 IF  RESET       NEXT ST20;
Present ST20                 NEXT ST0  OUT [ RAS,!MSEL, CAS, DTACK];)

APPEND MC1_.s  = !RESET;  APPEND REQ.s  = !RESET;  APPEND RFC.r = !RESET;
APPEND RAS.s   = !RESET;  APPEND MSEL.r = !RESET;  APPEND CAS.s = !RESET;
APPEND DTACK.s = !RESET;  APPEND P0_.r  = !RESET;  APPEND P1_.r = !RESET;
APPEND P2_.r   = !RESET;  APPEND P3_.r  = !RESET;  APPEND P4_.r = !RESET;
```

```
Partno          DMC-S167;
Name            DMC-S167;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*************************************************************/
/*                  DYNAMIC TIMING CONTROLLER                */
/*                       SIMULATION FILE                     */
/*                         FOR ALS6301                       */
/*************************************************************/
/* Allowable Target Device Types: TIB82S167B                 */
/*************************************************************/

ORDER:  GND,%3,OSC,%3,RESET,%6,REFREQ,%4,CLK,%3,AS,%2,A23_,%6,
        MC1_,%4,MSEL,%3,CAS,%3,RAS,%4,DTACK,%4,RFC,%4,REQ;

VECTORS:
$msg" REFRESH WITH ACCESS FOLLOWING";
$msg"     ";
$msg"    ------------ INPUT -------------   -------- OUTPUT ---------- ACCESS";
$msg"    GND OSC RESET REFREQ CLK AS A23    MC1 MSEL CAS RAS DTACK RFC  REQ";
$msg"    ------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X  X  X      H   L   H   H   H    L   H
/* ST0*/  0   C    1      0    X  X  X      H   L   H   H   H    L   H
/* ST1*/  0   C    1      X    X  1  X      L   L   H   H   H    L   L
/* ST2*/  0   C    1      X    X  X  X      L   L   H   L   H    H   L
/* ST3*/  0   C    1      X    X  X  X      L   L   H   L   H    H   L
/* ST4*/  0   C    1      X    X  X  X      L   L   H   L   H    L   L
/* ST5*/  0   C    1      X    X  X  X      L   L   H   H   H    L   L
/* ST6*/  0   C    1      X    X  X  0      H   L   H   H   H    L   L
/* ST7*/  0   C    1      X    X  X  X      H   L   H   L   H    L   L
/* ST8*/  0   C    1      X    X  X  X      H   H   H   L   H    L   H
/* ST9*/  0   C    1      X    X  X  X      H   H   L   L   L    L   H
/*ST10*/  0   C    1      X    X  X  X      H   H   L   L   L    L   H
/*ST11*/  0   C    1      X    X  X  X      H   H   L   L   L    L   H
/*ST12*/  0   C    1      X    X  X  X      H   H   L   L   L    L   H
/*ST13*/  0   C    1      X    X  X  X      H   L   H   H   H    L   H
/*ST0 */  0   C    1      1    0  0  X      H   L   H   H   H    L   H
/*ST0 */  0   C    1      1    0  1  X      H   L   H   H   H    L   H
/*ST0 */  0   C    1      1    1  0  X      H   L   H   H   H    L   H

$msg"     ";
$msg"     ";
$msg"REFRESH WITHOUT ACCESS FOLLOWING";
$msg"     ";
$msg"    ------------ INPUT -------------   -------- OUTPUT ---------- ACCESS";
$msg"    GND OSC RESET REFREQ CLK AS A23    MC1 MSEL CAS RAS DTACK RFC  REQ  ";
$msg"    ------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X  X  X      H   L   H   H   H    L   H
/* ST0*/  0   C    1      0    X  X  X      H   L   H   H   H    L   H
/* ST1*/  0   C    1      X    X  0  X      L   L   H   H   H    L   H
/* ST2*/  0   C    1      X    X  0  X      L   L   H   L   H    H   H
/* ST3*/  0   C    1      X    X  0  X      L   L   H   L   H    H   H
/* ST4*/  0   C    1      X    X  0  X      L   L   H   L   H    L   H
/* ST5*/  0   C    1      X    X  0  X      L   L   H   H   H    L   H
/* ST6*/  0   C    1      X    X  X  0      H   L   H   H   H    L   H
/* ST0*/  0   C    1      X    X  0  X      H   L   H   H   H    L   H
```

```
$msg"      ";
$msg"      ";
$msg"REFRESH WITH ACCESS REQUEST BUT DATA NOT IN DRAM (A23=H)";
$msg"      ";
$msg"      ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"      GND OSC RESET REFREQ CLK AS A23    MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"      ------------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X      H    L    H   H    H     L    H
/* ST0*/  0   C    1      0    X   X  X      H    L    H   H    H     L    H
/* ST1*/  0   C    1      X    X   1  X      L    L    H   H    H     L    L
/* ST2*/  0   C    1      X    X   0  X      L    L    H   L    H     H    L
/* ST3*/  0   C    1      X    X   0  X      L    L    H   L    H     H    L
/* ST4*/  0   C    1      X    X   0  X      L    L    H   L    H     L    L
/* ST5*/  0   C    1      X    X   0  X      L    L    H   H    H     L    L
/* ST6*/  0   C    1      X    X   0  1      H    L    H   H    H     L    H
/* ST0*/  0   C    1      1    0   0  X      H    L    H   H    H     L    H

$msg"      ";
$msg"      ";
$msg"ACCESS TIMING CYCLE ";
$msg"      ";
$msg"      ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"      GND OSC RESET REFREQ CLK AS A23    MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"      ------------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X      H    L    H   H    H     L    H
/*ST0 */  0   C    1      1    1   1  X      H    L    H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X      H    L    H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  0      H    L    H   L    H     L    H
/*ST16*/  0   C    1      X    X   X  X      H    H    H   L    L     L    H
/*ST17*/  0   C    1      X    X   X  X      H    H    L   L    L     L    H
/*ST18*/  0   C    1      X    X   X  X      H    H    L   L    L     L    H
/*ST19*/  0   C    1      X    X   X  X      H    H    L   L    L     L    H
/*ST20*/  0   C    1      X    X   X  X      H    L    H   H    H     L    H
/*ST0 */  0   C    1      1    0   0  X      H    L    H   H    H     L    H

$msg"      ";
$msg"      ";
$msg"ACCESS TIMING CYCLE BUT DATA NOT IN DRAM (A23=H)";
$msg"      ";
$msg"      ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"      GND OSC RESET REFREQ CLK AS A23    MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"      ------------------------------------------------------------------------";
/*ST0 */  0   C    1      1    1   1  X      H    L    H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X      H    L    H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  1      H    L    H   H    H     L    H
/*ST0 */  0   C    1      1    0   0  X      H    L    H   H    H     L    H

$msg"      ";
$msg"      ";
$msg"RESET DURING ACCESS TIMING CYCLE ";
$msg"      ";
$msg"      ------------ INPUT -------------    -------- OUTPUT ---------- ACCESS";
$msg"      GND OSC RESET REFREQ CLK AS A23    MCI MSEL CAS RAS DTACK RFC  REQ  ";
$msg"      ------------------------------------------------------------------------";
/*RESET*/ 0   C    0      X    X   X  X      H    L    H   H    H     L    H
/*ST0 */  0   C    1      1    1   1  X      H    L    H   H    H     L    H
/*ST14*/  0   C    1      X    X   X  X      H    L    H   H    H     L    H
/*ST15*/  0   C    1      X    X   X  0      H    L    H   L    H     L    H
/*ST16*/  0   C    1      X    X   X  X      H    H    H   L    L     L    H
/*ST17*/  0   C    1      X    X   X  X      H    H    L   L    L     L    H
/*ST18*/  0   C    0      X    X   X  X      H    L    H   H    H     L    H
/*ST0 */  0   C    0      X    X   X  X      H    L    H   H    H     L    H
/*ST0 */  0   C    0      X    X   X  X      H    L    H   H    H     L    H
```

BYTE CONTROLLER

```
Partno          BYTE_CON;
Name            BYTE_CON;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*                      BYTE CONTROLLER                          */
/*              FOR ALS6301/MC68000L10 APPLICATION               */
/*****************************************************************/
/* Allowable Target Device Types: TIBPAL16L8                     */
/*****************************************************************/
/**  Inputs  **/
pin 1 = CAS0;             /*  CAS BANK SELECT                    */
pin 2 = CAS1;             /*       "                             */
pin 3 = CAS2;             /*       "                             */
pin 4 = CAS3;             /*       "                             */
pin 5 = LDS;              /*  LOWER DATA STROBE                  */
pin 6 = UDS;              /*  UPPER DATA STROBE                  */

/**  Outputs  **/
pin 12 = UCAS0;           /*  UPPER BYTE SELECT - BANK 0         */
pin 13 = LCAS0;           /*  LOWER BYTE SELECT - BANK 0         */
pin 14 = UCAS1;           /*  UPPER BYTE SELECT - BANK 1         */
pin 15 = LCAS1;           /*  LOWER BYTE SELECT - BANK 1         */
pin 16 = UCAS2;           /*  UPPER BYTE SELECT - BANK 2         */
pin 17 = LCAS2;           /*  LOWER BYTE SELECT - BANK 2         */
pin 18 = UCAS3;           /*  UPPER BYTE SELECT - BANK 3         */
pin 19 = LCAS3;           /*  LOWER BYTE SELECT - BANK 3         */

/*  equations     */
UCAS0  = CAS0 # UDS;
LCAS0  = CAS0 # LDS;
UCAS1  = CAS1 # UDS;
LCAS1  = CAS1 # LDS;
UCAS2  = CAS2 # UDS;
LCAS2  = CAS2 # LDS;
UCAS3  = CAS3 # UDS;
LCAS3  = CAS3 # LDS;
```

BYTE CONTROLLER SIMULATION

```
Partno          BYTE_CON;
Name            BYTE_CON;
Date            08/15/86;
Revision        01;
Designer        SCHIELE;
Company         TEXAS INSTRUMENTS;
Assembly        None;
Location        DALLAS, TEXAS;
/*****************************************************************/
/*              BYTE CONTROLLER SIMULATION FILE                  */
/*            FOR ALS6301/MC68000L10  APPLICATION                */
/*****************************************************************/
/* Allowable Target Device Types: TIBPAL16L8                     */
/*****************************************************************/

ORDER:
CAS0,%2,CAS1,%2,CAS2,%2,CAS3,%3,LDS,%2,UDS,%4,LCAS0,%2,UCAS0,%2,
LCAS1,%2,UCAS1,%2,LCAS2,%2,UCAS2,%2,LCAS3,%2,UCAS3;

VECTORS:

$msg"      ----- INPUT -----     ------- OUTPUT -------   ";
$msg"                                L  U  L  U  L  U  L  U   ";
$msg"      C  C  C  C               C  C  C  C  C  C  C  C   ";
$msg"      A  A  A  A  L  U         A  A  A  A  A  A  A  A   ";
$msg"      S  S  S  S  D  D         S  S  S  S  S  S  S  S   ";
$msg"      0  1  2  3  S  S         0  0  1  1  2  2  3  3   ";
$msg"      ---------------------------------------------   ";
           1  1  1  1  X  X         H  H  H  H  H  H  H  H
           X  X  X  X  1  1         H  H  H  H  H  H  H  H

           0  1  1  1  0  0         L  L  H  H  H  H  H  H
           1  0  1  1  0  0         H  H  L  L  H  H  H  H
           1  1  0  1  0  0         H  H  H  H  L  L  H  H
           1  1  1  0  0  0         H  H  H  H  H  H  L  L

           0  1  1  1  0  1         L  H  H  H  H  H  H  H
           1  0  1  1  0  1         H  H  L  H  H  H  H  H
           1  1  0  1  0  1         H  H  H  H  L  H  H  H
           1  1  1  0  0  1         H  H  H  H  H  H  L  H

           0  1  1  1  1  0         H  L  H  H  H  H  H  H
           1  0  1  1  1  0         H  H  H  L  H  H  H  H
           1  1  0  1  1  0         H  H  H  H  H  L  H  H
           1  1  1  0  1  0         H  H  H  H  H  H  H  L
```

THCT4502B/MC68000L8 Interface

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Contents

List of Illustrations

Introduction

This application report presents a circuit configuration which interfaces the Motorola MC68000L8 (hereinafter MC68000L8) to DRAM memory via the THCT4502B dynamic RAM controller. The memory array is four banks of 256K-byte memory (TMS4256/4257) that provides a 1M byte system architecture.

Figure 1 is a schematic diagram of the circuit and Figure 2 a timing diagram for two consecutive read cycles. Figure 3 shows a write access, followed by a refresh, followed by a read-access grant. The THCT4502B uses the MC68000L8 system clock and requires no wait states on normal access cycles. When incorporating DRAMs and a DRAM controller into a microprocessor-based system, the following timing specifications should be satisfied to guarantee a correct match between processor and memory.

ALE-to-Clock Relationship
DRAM Refresh Time
DRAM Precharge Time
Row Address Setup and Hold Time
Data Valid to Write Enable Time
Read Access Time

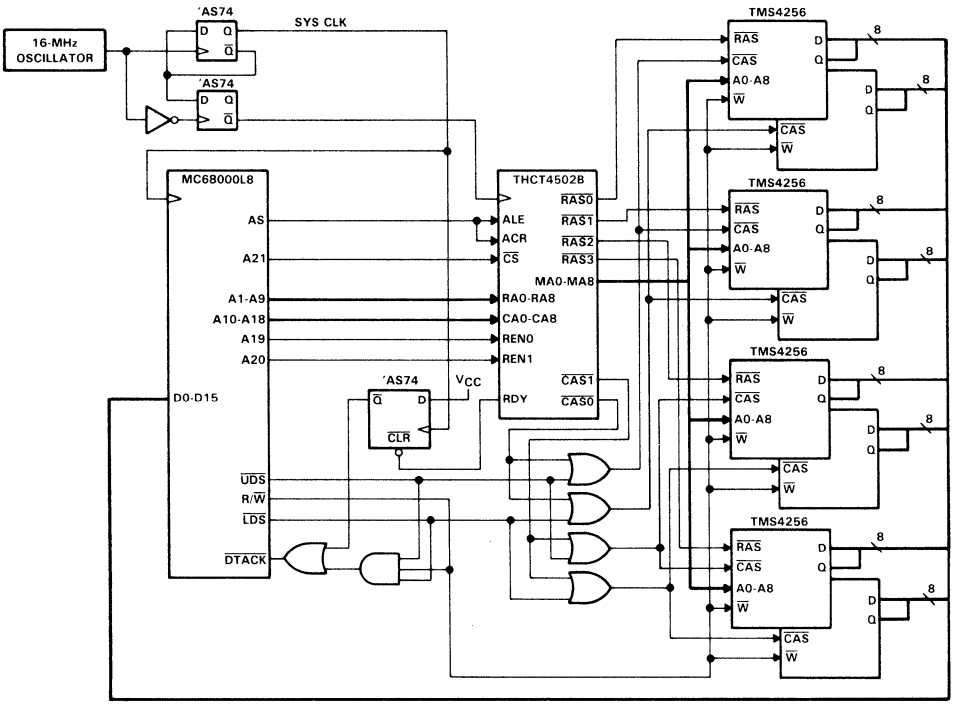

Figure 1. THCT4502B/MC68000L8 Interface Block Diagram

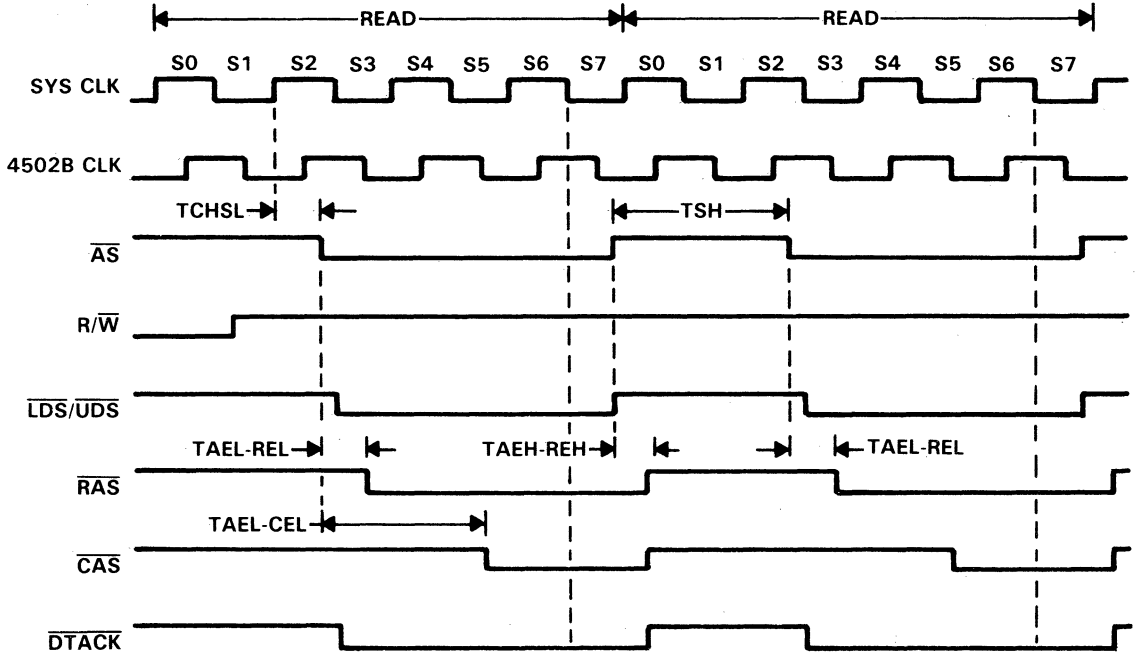

Figure 2. THCT4502B/MC68000L8 Read Cycle Timing Diagram

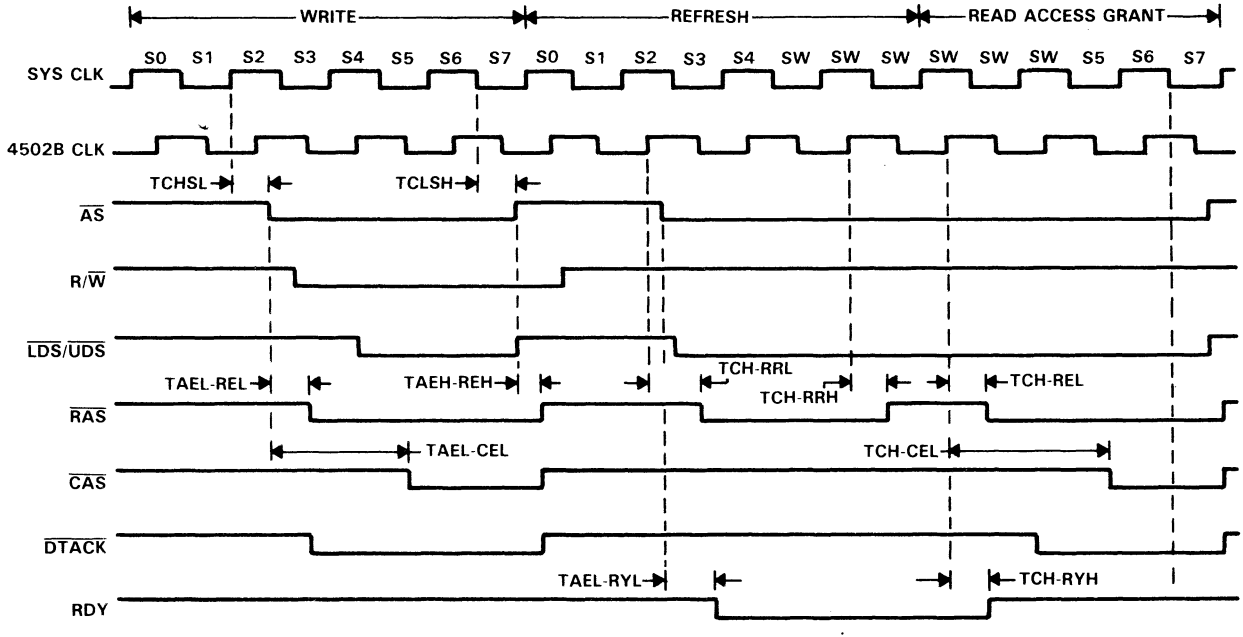

Figure 3. THCT4502B/MC68000L8 Write Access, Refresh, and Read Access Timing Diagram

ALE-to-Clock Relationship

When using the THCT4502B, the high-to-low transition of ALE should not occur between 15 ns before and 15 ns after the falling edge of the clock signal. This condition guarantees the proper selection between refresh and access cycles.

When connecting the Address Strobe (AS) of the MC68000 processor directly to ALE, ensure that the following condition is met:

$$15 < 0.5T - t_{CHSL}$$
$$15 < 0.5(125) - 60$$
$$15 < 2.5$$

At 8 MHz, this condition cannot be guaranteed. Therefore, a circuit is required to shift the input phase of the THCT4502B clock signal by 90 degrees. As shown in Figure 1, this circuit can be built using standard 'AS74 D-type flip-flops. With the THCT4502B CLK shifted by 90 degrees, the new equation becomes:

$$15 < 0.5T + 0.25T - t_{CHSL}$$
$$15 < 0.5(125) + 0.25(125) - 60$$
$$15 < 33.75$$

It should be noted that all of the following equations take into account the 90 degree phase shift. At lower clock frequencies, such as 6-MHz, the AS signal can be directly connected to the THCT4502B and the phase shift circuits are not required.

DRAM Refresh Time

The refresh clock frequency is controlled by the strap input pins (TWST, FS1, and FS0) on the THCT4502B. Table 1 shows the strap configuration for the THCT4502B. At 8 MHz, with no wait states, setting TWST low, FS1 high, and FS0 high yields a refresh rate of 11.375 μs/row. The TMS4256/4257 requires that each of the 256 rows be refreshed at least once every 4 ms. With a refresh rate of 11.375 μs/row, the time required to refresh all 256 rows will be 2.9 ms. This easily satisfies the 4-ms refresh requirement.

Table 1. Refresh Clock Frequency Input Pin Strap Configuration

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	—	REFREQ	4
L	L	H	0	EXTERNAL	—	REFREQ	3
L	H	L	0	CLK ÷ 61	3.904	64-95‡	3
L	H	H	0	CLK ÷ 91	5.824	64-88§	4
H	L	L	1	CLK ÷ 61	3.904	64-95‡	3
H	L	H	1	CLK ÷ 91	5.824	64-75‡	4
H	H	L	1	CLK ÷ 106	6.784	64-73‡	4
H	H	H	1	CLK ÷ 121	7.744	64-83¶	4

†This strap configuration resets the Refresh Timer Circuitry.
‡Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.
§Refresh frequency if clock frequency is 8 MHz.
¶Refresh frequency if clock frequency is 10 MHz.

DRAM Precharge Time

The precharge time is the time required between access cycles to allow internal nodes on the DRAM to charge to their correct reference levels. This is specified on the DRAM data sheet as $t_{w(RH)}$ min. As with most DRAMs, there is a choice of performance ranges. For the TMS4256/4257, $t_{w(RH)}$ ranges from 100 ns on the −12 device to 120 ns on the −20 device.

When using the THCT4502B, there are three precharge conditions which can occur during normal operation. Each condition must be checked to be sure the precharge condition is met. The following equations check these three conditions.

1. Access-to-Access cycle
   $t_{w(RH)} < t_{SH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{AEL\text{-}REL}$
   $t_{w(RH)} < 150 - 35 - 30 + 35$
   $t_{w(RH)} < 120$

2. Access-to-Refresh cycle
   $t_{w(RH)} < 1.5T + 0.25T + t_{CH\text{-}RRL} - t_{CLSH} - t_{AEH\text{-}REH} - t_{t(REH)}$
   $t_{w(RH)} < 1.5(125) + 0.25(125) + 50 - 70 - 35 - 30$
   $t_{w(RH)} < 133.75$

3. Refresh-to-Access cycle

$t_{w(RH)} < T - t_{CH\text{-}RRH} - t_{t(REH)} + t_{CH\text{-}REL}$

$t_{w(RH)} < 125 - 30 - 30 + 45$

$t_{w(RH)} < 110$

When the listed equations are correct, the THCT4502B guarantees the precharge condition for either the −12 or −15 TMS4256/4257 DRAMs.

Row Address Setup and Hold Time

To meet the row address setup-time requirement, the address must be present at the RA0-RA8 and CA0-CA8 inputs to the THCT4502B for at least 10 ns ($t_{AV\text{-}AEL}$) before ALE goes low. The row address setup time from the MC68000L8 is defined by the t_{AVSL} specification. At 8 MHz, t_{AVSL} is 30 ns minimum. This meets the THCT4502B specification. The row address setup time to the DRAM must also be satisfied. For the TMS4256/4257, $t_{su(RA)}$ is specified as 0-ns minimum. The following equation applies:

$0 \text{ ns} < t_{AVSL} + t_{AEL\text{-}REL} - t_{RAV\text{-}MAV}$

$0 \text{ ns} < 30 + 35 - 42$

$0 \text{ ns} < 23$

When the equation is correct, the THCT4502B guarantees the row address setup time to the DRAM. The row address hold time required by the TMS4256/4257 is 15 ns. This specification is guaranteed by the THCT4502B. From the data sheet, $t_{REL\text{-}MAX}$ is specified as 20 ns min.

Data Valid to Write Enable Setup Time

Data can be written into DRAM by two different methods. Depending upon the mode of operation, the falling edge of $\overline{CAS}$ or the the falling edge of $\overline{W}$ will strobe the data into memory. When $\overline{W}$ goes low prior to $\overline{CAS}$ going low, data out will remain in the high-impedance state for the entire cycle. This permits common input/output operation. This type of cycle is referred to as an early write cycle. When $\overline{W}$ goes low after $\overline{CAS}$ goes low, the type of cycle is referred to as delayed-write or read-modify-write cycle. To avoid bus contention, this operation requires a buffer between the Q outputs and the microprocessor.

The circuit shown in Figure 1 generates an early write cycle. Therefore, data valid to write enable needs to be referenced to the falling edge of $\overline{CAS}$. The TMS4256/4257 requirement for an early write cycle is $t_{su(WCL)}$, which is 0 ns minimum. The following equation applies:

$$0 \text{ ns} < t_{CHSL} + t_{AEL\text{-}CEL} - 0.5T - t_{CLDO}$$
$$0 \text{ ns} < 60 + 115 - 0.5(125) - 70$$
$$0 \text{ ns} < 42.5$$

When the equation is correct, the MC68000/THCT4502B combination guarantees that data will be valid before CAS goes low.

Read Access Time from $\overline{CAS}$

When the microprocessor tries to read data from memory, the Read-Access-Time guarantees that data is available. When using the THCT4502B, there are two possible access situations. The most common is the normal access cycle. Another possible access situation is the access-grant cycle. The access-grant cycle occurs when an access cycle immediately follows a refresh cycle.

For the TMS4256/4257, access from $\overline{CAS}$ is specified as $t_{a(C)}$. When using the TMS4256/4257, three speed types are available for selection. The three speed types are as follows:

Speed type -12 $t_{a(CA)} = 60$ ns
Speed type -15 $t_{a(CA)} = 75$ ns
Speed type -20 $t_{a(CA)} = 100$ ns

The following equations apply to the circuit shown in Figure 2.

1. Normal Access Cycles
   $$t_{a(C)} < 2.5T - t_{CHSL} - t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{p(OR)} - t_{DICL}$$
   $$t_{a(C)} < 2.5(125) - 60 - 115 - 20 - 15 - 15$$
   $$t_{a(C)} < 87.5$$
2. Access Grant Cycles
   $$t_{a(C)} < 2.5T - 0.25T - t_{CH\text{-}CEL} - t_{t(CEL)} - t_{p(OR)} - t_{DICL}$$
   $$t_{a(C)} < 2.5(125) - 0.25(125) - 140 - 20 - 15 - 15$$
   $$t_{a(C)} < 91.25$$

As shown by the equations, the only speed type that does not meet the access time requirement is the -20 device. The -12 and -15 devices both meet $t_{a(C)}$.

Other Considerations

The $\overline{\text{DTACK}}$ input on the MC68000L8 informs the microprocessor that data is available. Wait states are inserted by holding $\overline{\text{DTACK}}$ high. This process for the access-grant cycle is illustrated in Figure 3. If an access request occurs during a refresh cycle, the THCT4502B completes the refresh cycle, then finishes the access request. In this situation, the $\overline{\text{DTACK}}$ signal is held high until data is available. The AS74 flip-flop shown in Figure 1 is used to time the $\overline{\text{DTACK}}$ signal in relationship to the falling edge of S6.

On normal accesses, the RDY signal is high allowing either $\overline{\text{UDS}}$, $\overline{\text{LDS}}$ or R/$\overline{\text{W}}$ to force $\overline{\text{DTACK}}$ low. During write cycles, R/$\overline{\text{W}}$ will force $\overline{\text{DTACK}}$ low. During read cycles, $\overline{\text{UDS}}$ and/or $\overline{\text{LDS}}$ will force $\overline{\text{DTACK}}$ low. During access-grant cycles, the low RDY signal holds $\overline{\text{DTACK}}$ high until it is released.

Summary

This application report provides an example of how to interface the THCT4502B with the MC68000L8. The major design criteria has been calculated and checked against typical DRAM specifications. When using processor speeds lower than 8 MHz, the interface is simplified further because it is not necessary to shift the THCT4502B input clock frequencies. Additional design ideas can be obtained from an Applications Brief *TMS4500B/MC68000 INTERFACE*, Texas Instruments publication SMCA008.

SN74ACT4503/MC6800L10 Interface Using TMS4C1024 and TICPAL18V8

TEXAS INSTRUMENTS

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Contents

Appendix

List of Illustrations

Introduction

The SN74ACT4503 Dynamic RAM Controller is the 1M-bit counterpart of the THCT4502 Dynamic RAM Controller. This application report presents the system interface from four banks of TMS4C1024 1M DRAMs, via the 'ACT4503, to the MC68000L10 microprocessor with TICPAL18V8 acting as the decoder logic.

Figure 1 is a schematic diagram of the interface circuit and Figure 2 shows the discrete logic implementation of TICPAL18V8 shown in Figure 1. Figure 3, along with Tables 1 and 2, depicts the conditions for the FS0 and FS1 signals during the initial reset sequence. Access cycle and refresh cycle timings are shown in Figures 4 and 5. When incorporating DRAMs and a DRAM controller into a microprocessor based system, the following timing specifications should be satisfied to ensure a correct match between processor and memory.

ALE-to-Clock Relatlionship
DRAM Refresh Time
DRAM Precharge Time
Row Address Setup and Hold Times
Data Valid to Write Enable Time
Read Access Time

ALE-to-Clock Relationship

When using the 'ACT4503, the high-to-low transition of ALE should not occur earlier than 20 ns before the access/refresh arbitration edge of the clock. This condition ensures the arbitration between refresh and access cycle.

By using Table 2 to choose the proper access or refresh arbitration clock edge, a designer can ensure that the ALE-to-Clock relation is met when connecting the Address Strobe (AS) of the MC68000 processor directly to ALE.

At 10-MHz clock and low-to-high clock edge as access or refresh arbitration clock edge, equation 1 is satisfied.

$$20 < T - t_{CHSL} \quad (1)$$
$$20 < 100 - 55$$
$$20 < 45$$

This choice of access or refresh arbitration clock edge ensures the ALE-to-Clock relationship at a 10-MHz clock frequency.

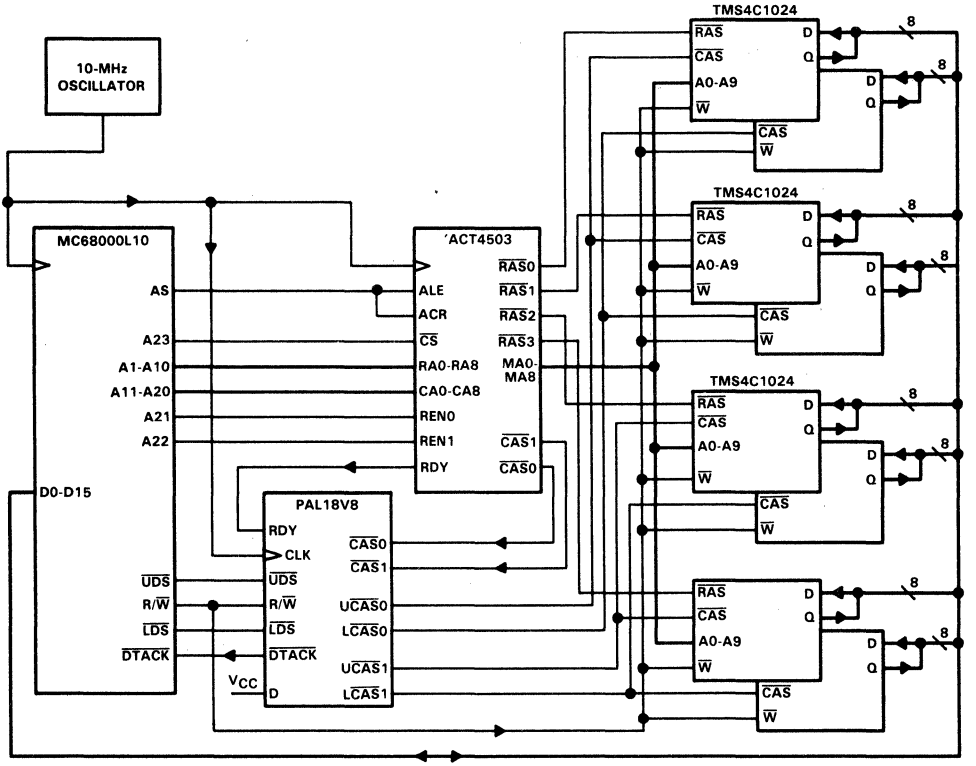


Figure 1. SN74ACT4503 to MC68000L10 Interface

DRAM Times

Refresh Time

The refresh clock frequency is controlled by the strap input pins (FS0 and FS1) on the 'ACT4503. Table 1 lists the strap configuration for the 'ACT4503. FS0 = H and FS1 = L setting at 10 MHz yields a refresh rate of 13.6 μs/row. The refresh requirement for 1M DRAM is to complete 512 rows of refresh in 8 ms. With a 13.6-μs refresh rate, the time to refresh 512 rows is 6.96 ms. This refresh time easily satisfies the 8-ms requirement.

Precharge Time

The precharge time is the time required between access cycles to allow internal nodes on the DRAM to charge to their correct reference levels. This is specified on the DRAM data sheet as $t_{w(RH)}$min. The TMS4C1024 1M DRAM can select three different speeds regarding the $t_{w(RH)}$:

Speed Selection	$t_{w(RH)}$
– 15	100 ns
– 12	90 ns
– 10	80 ns

Table 1. Strap Configuration

Strap Input Modes		Refresh Rate	Minimum Clock Frequency (MHz)	Maximum Clock Frequency (MHz)	Refresh Frequency (kHz)	Clock Cycles For Each Refresh
FS1	FS0					
L	L	CLK/61	3.904	5.824	64-95	3
H	H	CLK/91	5.824	7.744	64-85	4
H	L	CLK/121	7.744	8.704	64-72	4
L	H	CLK/136	8.704	10.50	64-77	4

Table 2. Operation Mode Selection

Selection	Operation Modes
FS0 = L	Access/refresh arbitration on high-to-low clock edge
FS0 = H	Access/refresh arbitration on low-to-high clock edge
FS1 = L	Refresh cycles initiated internally
FS1 = H	Refresh cycles initiated externally. Internal refresh timer disabled.

There are three conditions in which precharge time is relevant for normal operation of the 'ACT4503. Each of the conditions must be checked to ensure that the precharge time is met. The following equations check these three conditions.

1. Access-to-Access cycle

$$t_{w(RH)} < t_{SH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{AEL\text{-}REL} \quad (2)$$
$$t_{w(RH)} < 105 - 20 - 10 + 20$$
$$t_{w(RH)} < 95$$

2. Access-to-Refresh cycle

$$t_{w(RH)} < 2.5T - t_{CLSH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{C\text{-}RRL} \quad (3)$$
$$t_{w(RH)} < 250 - 55 - 10 + 40$$
$$t_{w(RH)} < 205$$

3. Refresh-to-Access cycle

$$t_{w(RH)} < 1.5T - t_{C\text{-}RRH} - t_{t(REH)} + t_{C\text{-}REL} \quad (4)$$
$$t_{w(RH)} < 150 - 25 - 10 + 30$$
$$t_{w(RH)} < 145$$

When the conditions of equations 2, 3, and 4 are met, the 'ACT4503 ensures the precharge time of the –10 and –12 TMS4C1024 DRAMs at 10-MHz clock frequency.

Setup and Hold Times

Row-Address Setup and Hold Times

To meet the row-address setup time requirement, the address must be present at the RA0 through RA9 and CA0 through CA9 inputs of the 'ACT4503 for at least 5 ns $t_{AV\text{-}AEL}$ before ALE goes low. The row and column addresses from the MC68000L10 appear on the address bus 20 ns (t_{AVSL}) before the falling edge of AS signal. This row-address setup time defined by t_{AVSL} of the processosr easily meets the 'ACT4503 row-address setup time requirements.

To meet the 0-ns row-address setup time, $t_{su(RA)}$, of the TMS4C1024, the following equation must hold true.

$$0 < t_{AVSL} + t_{AEL\text{-}REL} - t_{RAV-MAV} \quad (5)$$
$$0 < 20 + 20 - 30$$
$$0 < 10$$

When equation 5 is satisfied, the 'ACT4503 will ensure the row-address setup time to the DRAM. $t_{REL\text{-}MAX}$ of the 'ACT4503 is timed from the input clock so that the row-address hold time to the TMS4C1024 is a minimum of 20 ns.

Data Valid to Write-Enable Setup Time

Data can be written into the DRAM using two different methods. Depending upon the mode of operation, the falling edge of $\overline{CAS}$ or the falling edge of $\overline{W}$ will strobe the data into memory. When $\overline{W}$ goes low prior to $\overline{CAS}$ going low, the data out will remain in the high-impedance state for the entire cycle. This permits common input/output operation. This type of cycle is referred to as an early write cycle. When $\overline{W}$ goes low after $\overline{CAS}$ goes low, the type of cycle is referred to as delayed-write or read-modify-write cycle. To avoid bus contention, this operation requires a buffer between the Q output and the microprocessor.

The circuit shown in Figure 1 generates an early write cycle. Therefore, data valid to write enable needs to be referenced to the falling edge of $\overline{CAS}$. The write-enable signal must meet the $t_{su(WCL)}$ requirement (0 ns) of the TMS4C1024 and the valid data must meet the setup time, $t_{su(D)}$ (30 ns), before $\overline{CAS}$. Equations 6 and 7 describe the write-enable setup time before $\overline{CAS}$ and the valid-data setup time before $\overline{CAS}$, respectively.

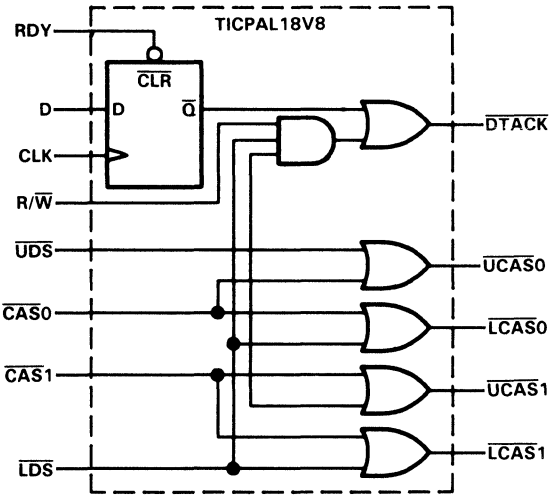


Figure 2. Discrete Logic Implementation of TICPAL18V8

$$t_{su(WCL)} < t_{CHSL} + t_{AEL\text{-}CEL} - t_{CHRL} \quad (6)$$
$$t_{su(WCL)} < 55 + 90 - 60$$
$$t_{su(WCL)} < 85$$

$$t_{su(D)} < t_{CHSL} + t_{AEL\text{-}CEL} - 0.5T - t_{CLDO} \quad (7)$$
$$t_{su(D)} < 55 + 100 - 50 - 55$$
$$t_{su(D)} < 50$$

Satisfying equations 6 and 7 ensures the early write cycle with the data input being valid before $\overline{CAS}$ goes low.

Read-Access Time from CAS

When the microprocessor tries to read data from memory, the read-access time ensures that data is available. There are two possible access situations: normal access cycle and access grant cycle. Normal access cycle is a more common access cycle than the access grant cycle, which occurs immediately following a refresh cycle.

Three speed sorts are available for the TMS4C1024 access time $t_{a(C)}$.

Speed Selection	$t_{a(C)}$	$t_{a(CA)}$
– 15	40 ns	70 ns
– 12	30 ns	55 ns
– 10	25 ns	45 ns

Equations 8 and 9 apply for the two access cycles.

1. Normal Access Cycles

$$t_{a(C)} < 2.5T - t_{CHSL}\ t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{pd(PAL)} - t_{DICL} \quad (8)$$
$$t_{a(C)} < 250 - 55 - 100 - 10 - 25 - 15$$
$$t_{a(C)} < 45$$

2. Access Grant Cycles

$$t_{a(C)} < 2.5T - t_{C\text{-}CEL} - t_{t(CEL)} - t_{pd(PAL)} - t_{DICL} \quad (9)$$
$$t_{a(C)} < 250 - 105 - 10 - 25 - 15$$
$$t_{a(C)} < 95$$

In addition to meeting these access times from $\overline{CAS}$, the maximum access time from column address must also be met. Equations 10 and 11 apply after equations 8 and 9 are satisfied.

1. Normal Access Cycle

$$t_{a(CA)} < t_{a(C)1} + t_{MAV\text{-}CEL} + t_{t(CEL)} + t_{pd(PAL)} \quad (10)$$
$$t_{a(CA)} < 45 + 5 + 10 + 25$$
$$t_{a(CA)} < 85$$

2. Access Grant Cycles

$$t_{a(CA)} < t_{a(C)2} + t_{t(CEL)} + t_{pd(PAL)} \quad (11)$$
$$t_{a(CA)} < 95 + 10 + 25$$
$$t_{a(CA)} < 130$$

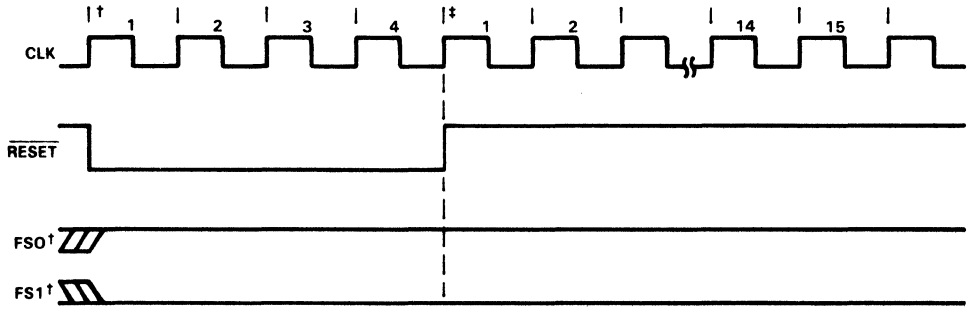
Where $t_{a(C)1}$ and $t_{a(C)2}$ are the times resulted from equations 8 and 9.

Other Considerations

The $\overline{DTACK}$ input on the MC68000L10 informs the microprocessor that data is available. Wait states are inserted by holding $\overline{DTACK}$ high. This process for the access grant cycle is illustrated in Figure 4. If an access request occurs during a refresh cycle, the 'ACT4503 completes the refresh cycle, then finishes the access request. In this situation, the $\overline{DTACK}$ signal is held high until data is available. The internal register of TICPAL18V8, shown in Figure 2, is used to time the $\overline{DTACK}$ signal in relation to the falling edge of S6.

On normal accesses, a high RDY signal allows either UDS, LDS or R/$\overline{W}$ to force $\overline{DTACK}$ low. During write cycle, R/$\overline{W}$ will force $\overline{DTACK}$ low. During read cycles, UDS and/or LDS will force $\overline{DTACK}$ low. During access grant cycles, the low RDY signal holds $\overline{DTACK}$ high. The RDY signal returns to the high state immediately after the refresh sequence is completed.

For proper operation of the 'ACT4503, the reset sequence must be executed with the correct FS0 and FS1 strap inputs. Figure 3 shows that for the last four clock cycles of the RESET low, FS0 and FS1 have to be at the logic levels which select the desired operation mode. After the low-to-high transition of the RESET signal, initial 15 clock cycles are needed to calibrate the row address hold time. Any access request during this calibration time is treated like an access cycle occuring during a refresh cycle.



† FS0 and FS1 signals are based on Table 2 for these initial four clock periods during reset low.
† FS0 and FS1 signals are set to the corresponding refresh frequency as shown in Table 1. 15 clock periods of initialization after $\overline{\text{RESET}}$ is required by the 'ACT4503 for row address hold time calibration.

Figure 3. Reset Sequence

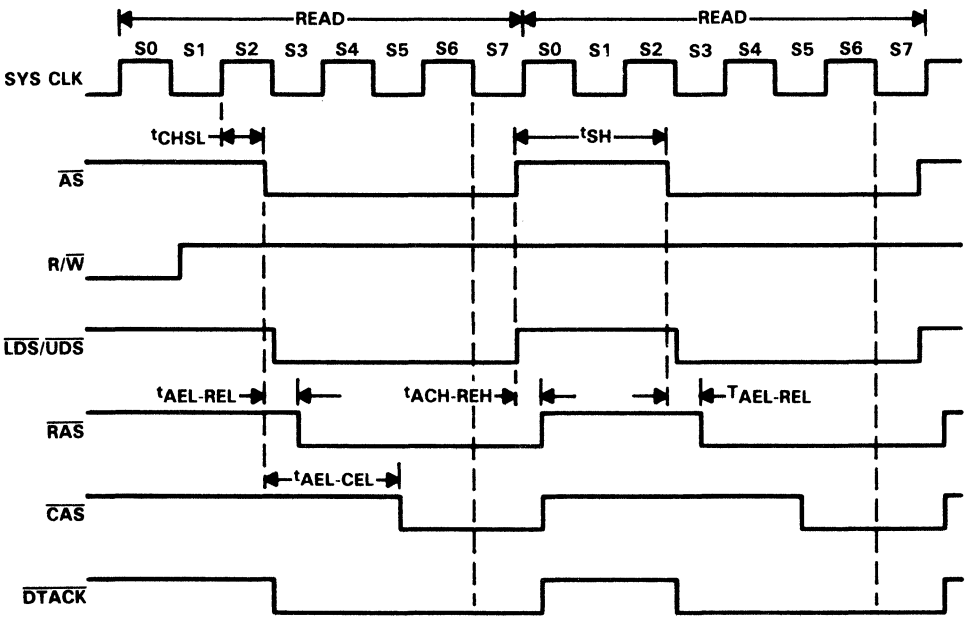


Figure 4. 'ACT4503 to MC68000L10 Timing

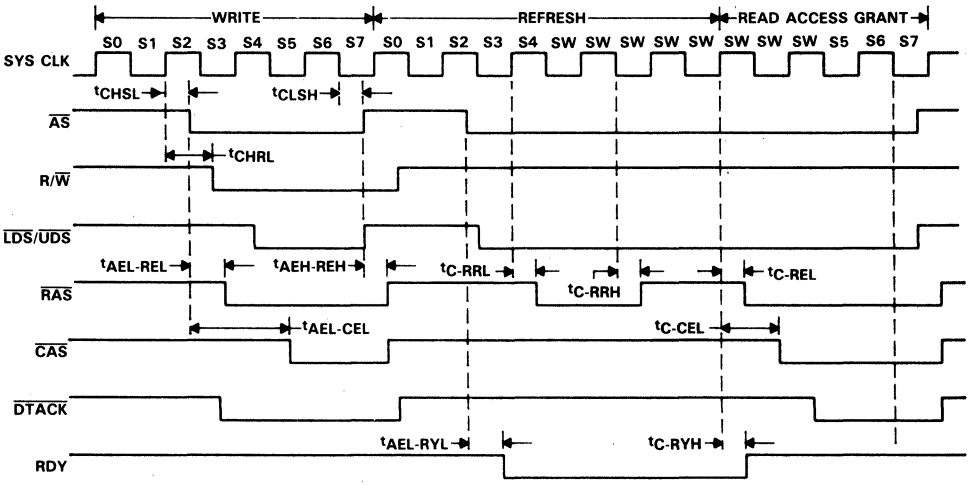


Figure 5. 'ACT4503 to MC68000L10 Timing

Decoder Implementation

TICPAL18V8 with flexible output macro cell allows the designer to implement the decoder logic in a single chip which would otherwise be implemented with several discrete logic devices as shown in Figure 2. Refer to 1988 *Programmable Logic Data Book* for more information on TICPAL18V8.

TICPAL18V8 is supported by ABEL development software. The ABEL source file, which is used to develop the fusemap of the decoder logic and to test the functionality of the logic, is appended to this application brief.

Summary

This application report provides an example of how to interface the 'ACT4503 with the MC68000L10. The design ideas in this application report are based on the THCT4502BV/MC68000L8 Interface application note in *Memory Management Applications Handbook* and the *TMS4500B/MC68000 Interface* application report, Texas Instruments publication SMCA008.

APPENDIX A
CONTROL LOGIC FOR 'ACT4503

```
module _CNTR4503 FLAG '-R3','-F0'
title 'CONTROL LOGIC FOR ACT4503
       BERTRAND LEIGH, TEXAS INSTRUMENTS, MAY 16, 1988'

         CNTR4503 device 'P18V8';

"*************************************************************************
" This control logic converts the RDY signal form ACT4503 through a
" D-type flip-flop so that it will conform to the requirements of the
" DTACK input of the MC68000. It also decodes CAS0 and CAS1 form the
" ACT4503 and UDS and LDS from the processor to drive the appropriate
" CAS signal of the DRAM.
"*************************************************************************

"Input pin assignments
  SYS_CLK      PIN 1;      "SYSTEM CLOCK
  D            PIN 2;      "D INPUT OF THE D-TYPE FLIP-FLOP
  RDY          PIN 3;      "ACT4503 RDY SIGNAL
  UDS_         PIN 4;      "UPPER DATA STROBE FROM THE PROCESSOR
  LDS_         PIN 5;      "LOWER DATA STROBE FROM THE PROCESSOR
  RW_          PIN 6;      "R/W SIGNAL FROM THE PROCESSOR
  CAS0_        PIN 7;      "CAS0 FROM ACT4503
  CAS1_        PIN 8;      "CAS1 FROM ACT4503

"Output pin assignments
  UCAS0_       PIN 12;     "UPPER DATA BYTE CAS0 OUTPUT
  LCAS0_       PIN 13;     "LOWER DATA BYTE CAS0 OUTPUT
  UCAS1_       PIN 14;     "UPPER DATA BYTE CAS1 OUTPUT
  LCAS1_       PIN 15;     "LOWER DATA BYTE CAS1 OUTPUT
  Q_           PIN 16;     "!Q OUTPUT OF THE D FLIP-FLOP
  DTACK_       PIN 17;     "DTACK SIGNAL DRIVING PROCESSORS INPUT

"I/O pin definition
  UCAS0_,LCAS0_,UCAS1_,LCAS1_,DTACK_  ISTYPE  'COM,NEG,FEED_PIN';
  Q_                                  ISTYPE  'NEG,FEED_REG';

"Intermediate declaration
  H,L,C,X  = 1,0,.C.,.X.;

equations

UCAS0_ = UDS_ # CAS0_ ;
LCAS0_ = LDS_ # CAS0_ ;
UCAS1_ = UDS_ # CAS1_ ;
LCAS1_ = LDS_ # CAS1_ ;
DTACK_ = (UDS_ & RW_ & LDS_) # Q_ ;
Q_     := !D ;
Q_.AR  = !RDY ;
```

```
test_vectors

([SYS_CLK,D,RDY,UDS_,LDS_,RW_,CAS0_,CAS1_]->[UCAS0_,LCAS0_,UCAS1_,LCAS1_,Q_,DTACK_])
 [   C   ,H, H , H  , H  , H , H  ,  H  ]->[  H   ,  H   ,  H   ,  H   , L,  H   ] ;
 [   C   ,H, H , L  , H  , H , L  ,  H  ]->[  L   ,  H   ,  H   ,  H   , L,  L   ] ;
 [   C   ,H, H , H  , L  , H , L  ,  H  ]->[  H   ,  L   ,  H   ,  H   , L,  L   ] ;
 [   C   ,H, H , L  , L  , H , L  ,  H  ]->[  L   ,  L   ,  H   ,  H   , L,  L   ] ;
 [   C   ,H, H , L  , H  , L , H  ,  L  ]->[  H   ,  H   ,  L   ,  H   , L,  L   ] ;
 [   C   ,H, H , H  , L  , L , H  ,  L  ]->[  H   ,  H   ,  H   ,  L   , L,  L   ] ;
 [   C   ,H, H , L  , L  , L , H  ,  L  ]->[  H   ,  H   ,  L   ,  L   , L,  L   ] ;
 [   C   ,H, L , L  , L  , L , L  ,  H  ]->[  L   ,  L   ,  H   ,  H   , H,  H   ] ;
 [   C   ,H, H , H  , H  , H , H  ,  H  ]->[  H   ,  H   ,  H   ,  H   , L,  H   ] ;

END
```

System Solutions for Static Column Decode

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Contents

Appendixes

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List of Illustrations

Introduction

The new 32-bit microprocessors are capable of addressing 4G bytes of physical memory and typically feature clock frequencies greater than 16 MHz. However, clock speed alone does not guarantee increased system performance; if the processor must wait for data, then memory bandwidth will be the limiting factor.

This situation exists between today's microprocessors and the access times of affordable DRAMs. One solution to optimizing system performance is to mix and match memory, using lower-cost dynamic RAM in conjunction with fast, more expensive static RAM caches. However, this approach is only attractive to high-end systems where cost and board space is a less significant factor.

Another approach to improving system performance is to utilize the new accessing modes available on certain 1M-bit DRAMs, such as static column decode. This method does not improve system performance as much as caches, but it does involve less hardware, resulting in lower system cost. This approach can also be used in systems already using caches, further improving system performance.

This application note describes the theory of using static column decode and also describes how it might be implemented in a typical system. In addition, it highlights three new products from Texas Instruments; the SN74ALS6300 Selectable Refresh Timer, the SN74ALS6310 Static Column Access Detector, and the TIBPSG507 Programmable Sequence Generator.

Static Column Decode

The TMS4C1027 is a 1,048,576-bit × 1 dynamic RAM featuring static column decode. Static column decode allows high-speed read and write operations by reducing the number of required signal setup, hold, and transition timings. This is achieved by first strobing the row and column addresses in the normal manner by taking $\overline{RAS}$ and $\overline{CAS}$ low. If $\overline{RAS}$ and $\overline{CAS}$ are kept low, new data can be accessed by simply changing the column addresses, assuming the new address is in the same row. If the new address is not in the same row, then a normal access cycle must be performed.

Figure 1 is a timing diagram taken from the TMS4C1027 data sheet showing static column-decode-mode read cycle timing.

If the assumption is made that the majority of memory references tend to be sequential, which is a similar assumption made when using caches, then it is logical to assume that a large percentage of memory accesses will be within the same row. The trick is how to implement a timing controller that will take full advantage of the static column mode of operation.

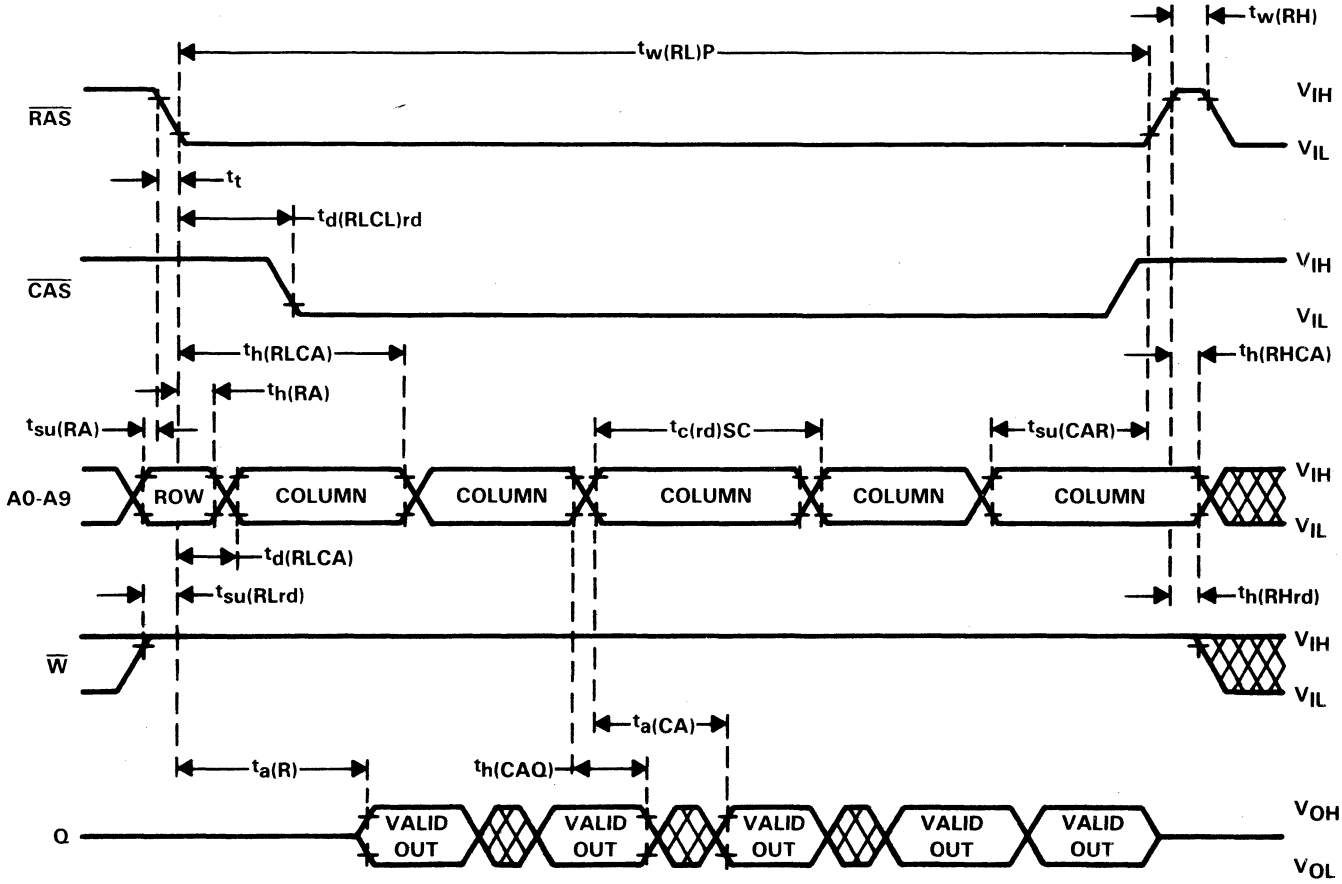

Figure 1. Static Column-Decode-Mode Read Cycle Timing

Typical Memory Controller

Figure 2 shows a block diagram of a memory system utilizing static column decode. The 'ALS6310 is a new circuit offered by Texas Instruments that detects if the present row being accessed is the same as last row accessed. This is the fundamental requirement for implementing static column decode. Note that the row addresses from the Motorola MC68020 (hereinafter MC68020) are used as the most significant bits (A10-A19), and the column addresses are used as the least significant bits (A0-A9). Figure 3 shows a block diagram of the 'ALS6310.

In circuit operation, when address strobe (AS) from the MC68020 is taken low, the present row (A10-A19) and bank address (B0, B1) is clocked into the first register of the 'ALS6310. The previous bank and row address, stored in the first register, is clocked into the second register at the same time. The two addresses are then compared to see if they are equal. If they are equal, the high-speed access output ($\overline{HSA}$) will be logically low. If not, $\overline{HSA}$ will be high.

The function of the PSG507 is to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the 'ALS6301 dynamic memory controller. The 'ALS6301 is responsible for multiplexing row and column addresses into DRAM. The 'ALS6301 is also capable of driving four banks of 1M-byte memory.

Supporting the TIBPSG507 is the 'ALS6300 refresh timer. This device is responsible for generating a refresh request signal ($\overline{REFREQ}$) every 15.5 μs. The input select lines are hardwired to match the microprocessor clock frequency. The refresh complete input ($\overline{RFC}$) resets the $\overline{REFREQ}$ signal after the timing controller completes the refresh cycle.

Timing Controller Details

Figure 4 shows a typical flow chart for implementing static column decode. As stated before, the TIBPSG507 is responsible for implementing the flow chart shown in Figure 4. A breakdown of this flow chart reveals 9 states (ST0-ST8) associated with 5 different sequences. States ST0, ST1, ST3, and ST4 are holding and transition states leading into the various sequences. The five possible sequences are listed below.

ST2 Normal Access Sequence
ST5 Extended Access Sequence
ST6 High-Speed Access Sequence
ST7 Normal Refresh Sequence
ST8 Extended Refresh Sequence

Notice that the $\overline{HSA}$ signal from the 'ALS6310 decides if the timing controller will execute ST5, the Extended Access Sequence, or ST6, the High-Speed Access Sequence. A brief description of each sequence follows.

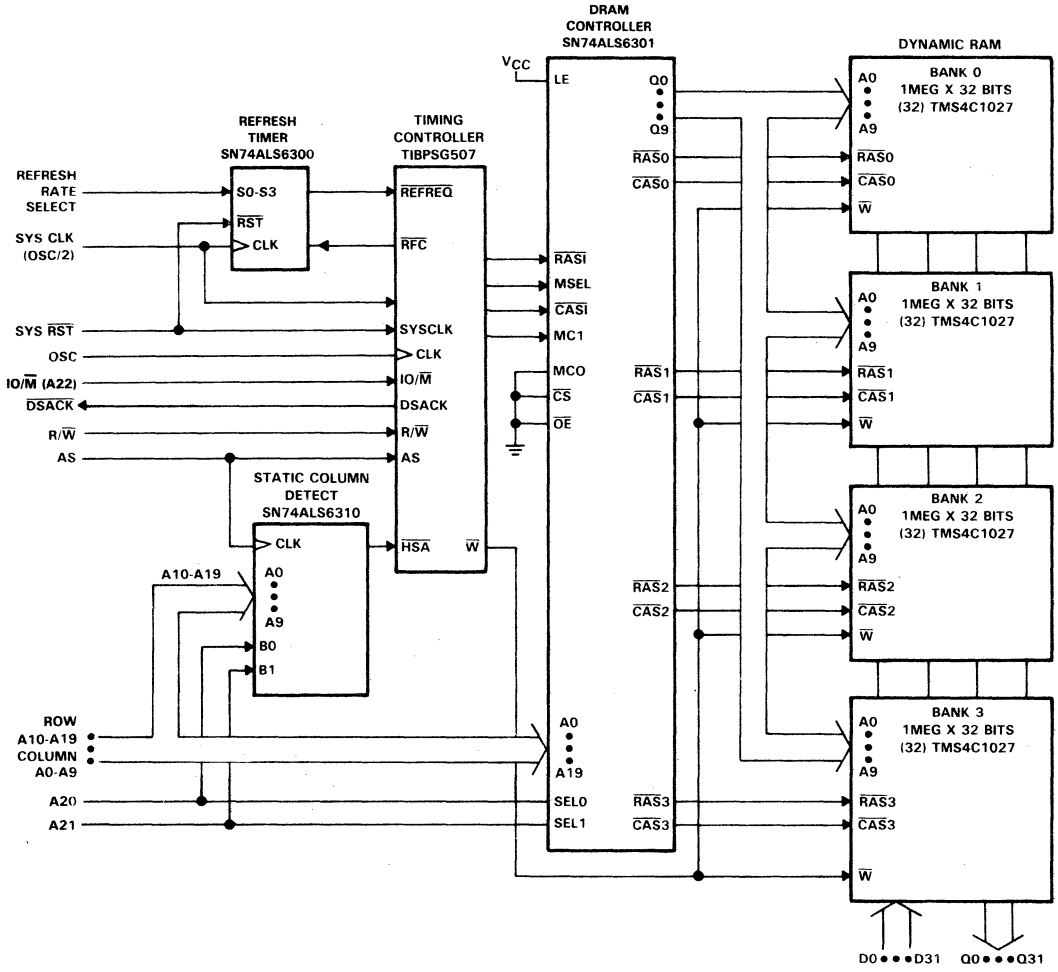

Figure 2. MC68020 Static Column Memory Controller

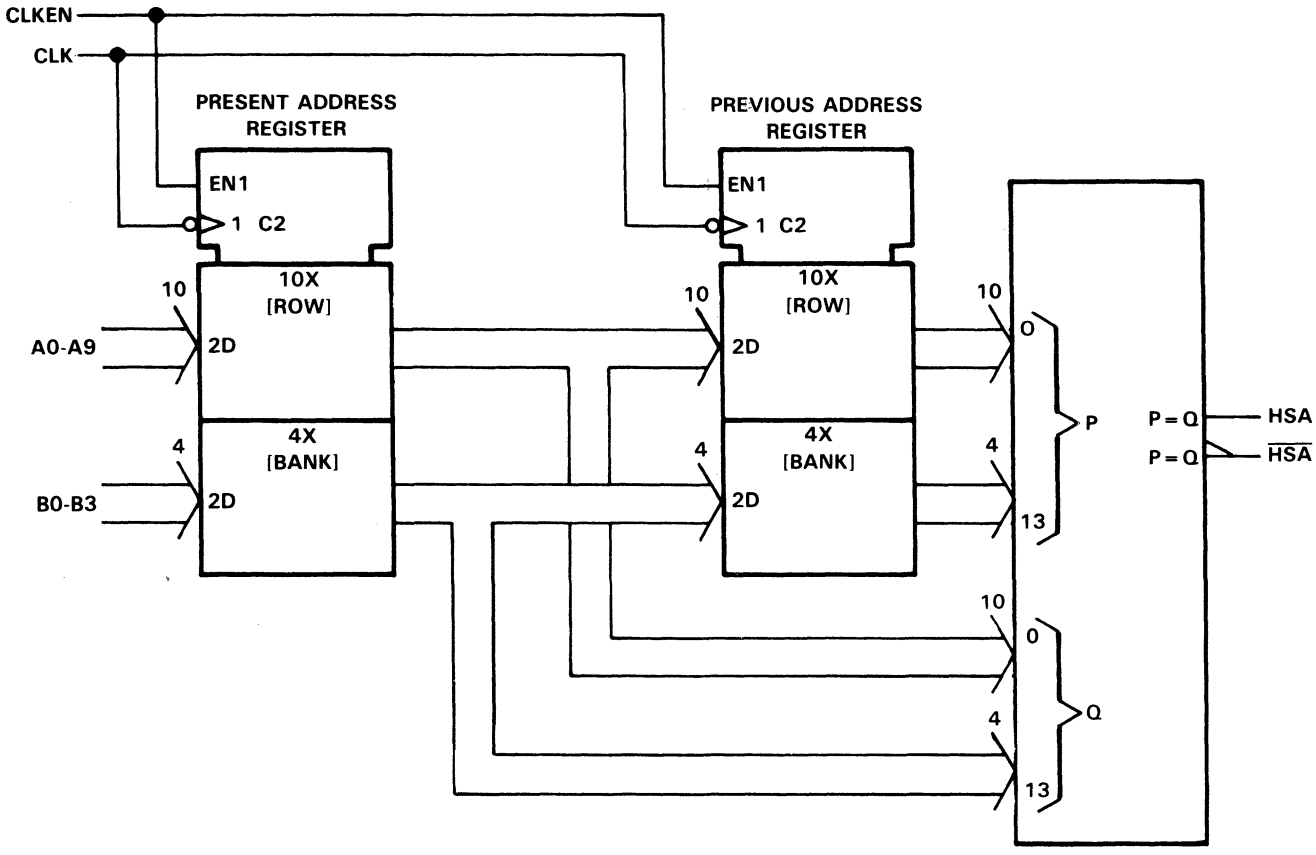

Figure 3. 'ALS6310 Static Column Page Mode Access Detector

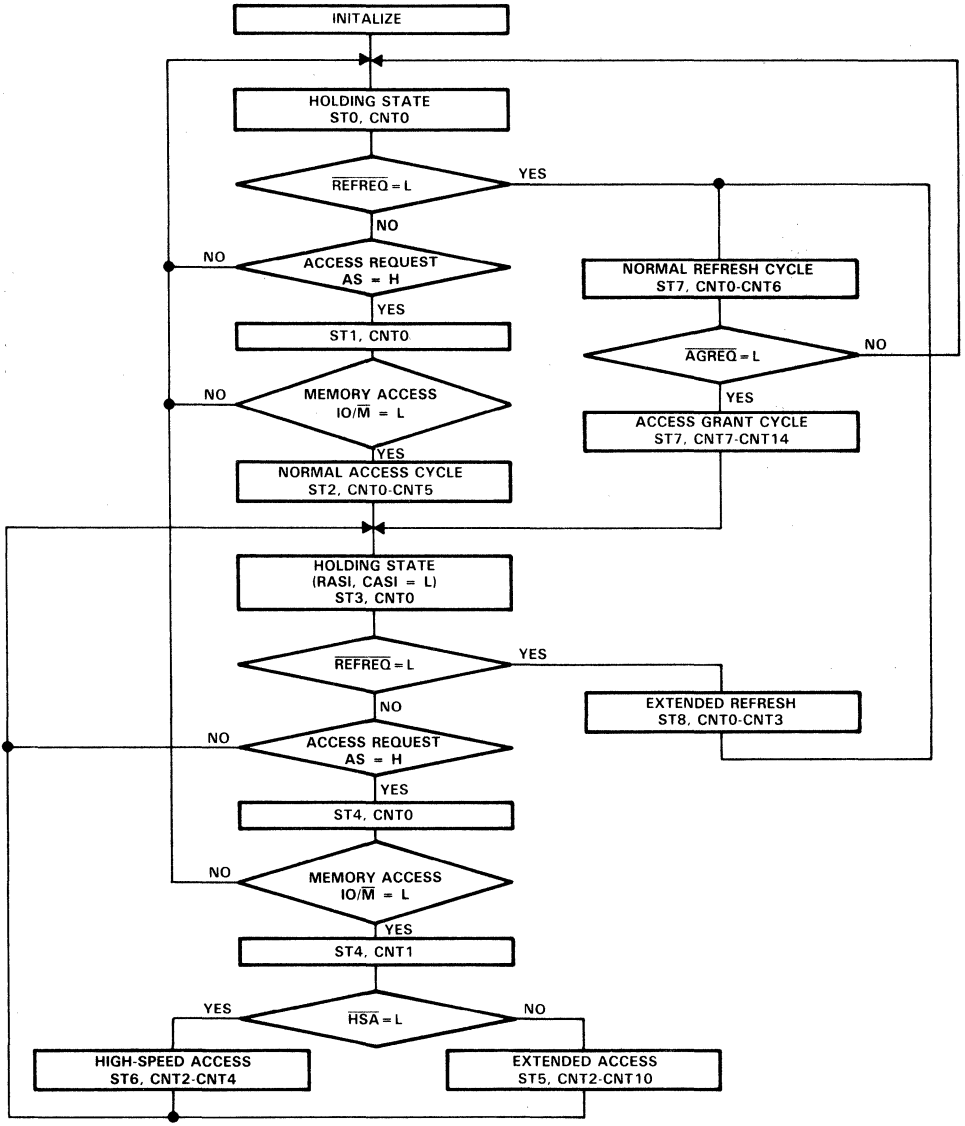

Figure 4. Timing Controller Flowchart

Normal Access Sequence

The normal access sequence is shown in Figure 5. This sequence begins by executing a normal $\overline{RAS}/\overline{CAS}$ cycle. Notice that a wait state of one clock cycle is needed to guarantee that data is valid for the MC68020. This is the problem mentioned in the introduction; if all access cycles had to be performed in this manner, then the processor would face a wait state every access cycle. As will be shown later, this wait state can be eliminated if the next address is from the same row.

Notice also, at the end of this sequence, the $\overline{RAS}$ and $\overline{CAS}$ output signals are left active (low). Here we are making the assumption that the next access cycle will be a high-speed access. We will not know if this assumption is true until the next address is presented by the MC68020. At that time, the 'ALS6310 will signal the timing controller if it can execute a high-speed access.

High-Speed Access Sequence

For a high-speed access sequence to be executed, two conditions must be met. The $\overline{RAS}$ and $\overline{CAS}$ inputs must already be low, and secondly, the static column access detector must be indicating the present row is the same as the last row ($\overline{HSA}$ = L). The bank addresses must also be unchanged as detected by the 'ALS6310.

Figure 6 shows the timing diagram for the high-speed access sequence. Notice that no wait states are required. If the assumption is made that the majority of memory references are sequential, then this sequence will be the one typically used. In other words, this sequence is similar to accessing data from a static RAM or just like taking data from cache.

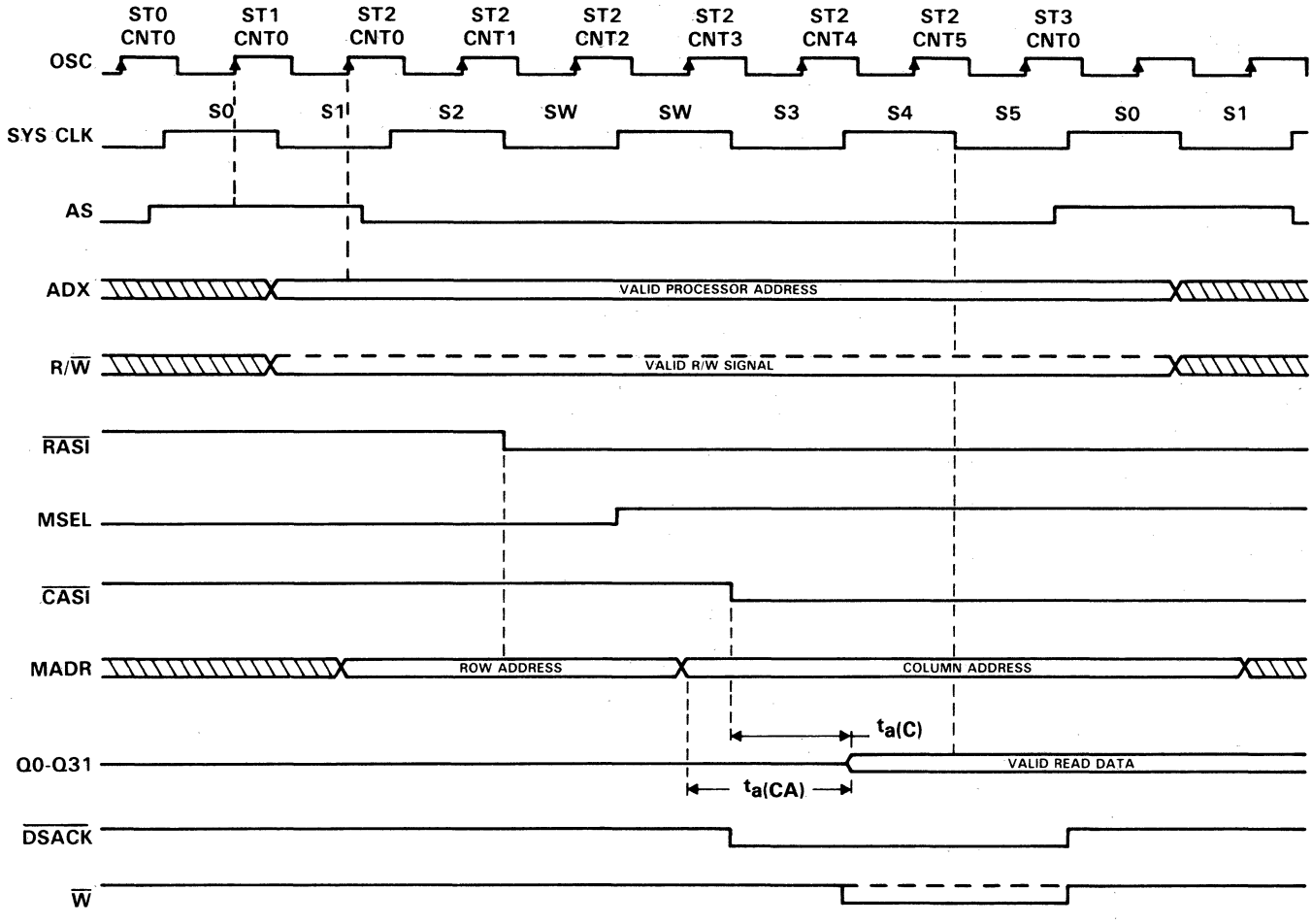

Figure 5. Normal Access Cycle

Extended Access Sequence

The extended access sequence is executed if the 'ALS6310 detects a difference between the present and last row addresses. This cycle is called extended because $\overline{RAS}$ and $\overline{CAS}$ are presently low and both must be brought high to strobe inthe new row and column addresses. The precharge time of the DRAM has to be met before taking $\overline{RAS}$ and $\overline{CAS}$ low. From the timing diagram in Figure 7, it can be seen that wait states of three clock cycles are generated when executing this timing sequence.

In systems where sequential data is not the general rule, it would be more efficient to execute only normal access sequences, since this generates fewer wait states. The system designer must understand what type of memory accesses will be used. For example, the designer may want only to enter the high-speed access portion of the flow chart when the system is performing DMA access cycles.

Normal/Extended Refresh Sequences

Figures 8 and 9 show the timing diagrams for the normal and extended refresh sequences. The refresh sequence selected is a function of the present condition of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ and $\overline{CAS}$ are presently low, an extended refresh cycle is performed. If $\overline{RAS}$ and $\overline{CAS}$ are presently high, a normal refresh cycle is executed. At the end of each refresh sequence, the controller checks to see if an access request has been generated. If there has been a access request, the controller will perform an access grant sequence at the end of the refresh cycle before returning to normal process flow.

Referring back to Figure 1, there is a maximum time that $\overline{RAS}$ and $\overline{CAS}$ can be held low, $t_{W(RL)P}$. For the TMS4C1027, $t_{W(RL)P}$ must not exceed 100 μs. Since our refresh timer forces a refresh cycle every 15.5 μs, $t_{W(RL)P}$ cannot be violated. If the designer chooses to use a different refresh scheme, then $t_{W(RL)P}$ must be considered.

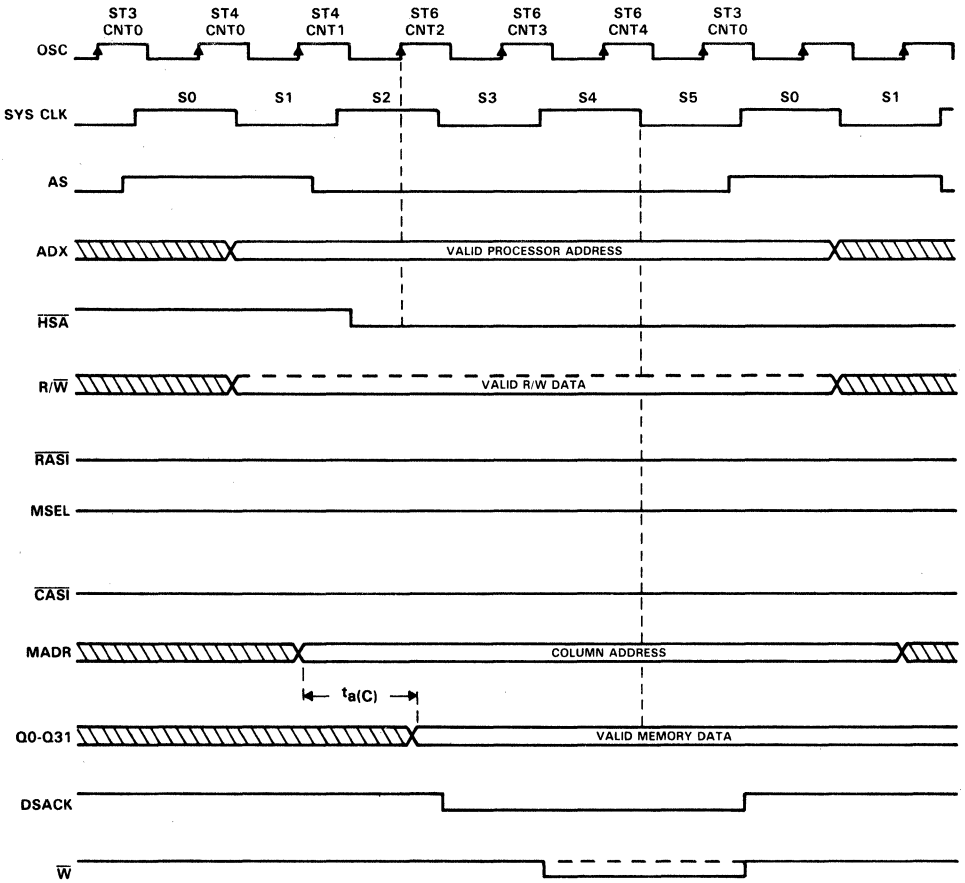

Figure 6. High-Speed Access Cycle

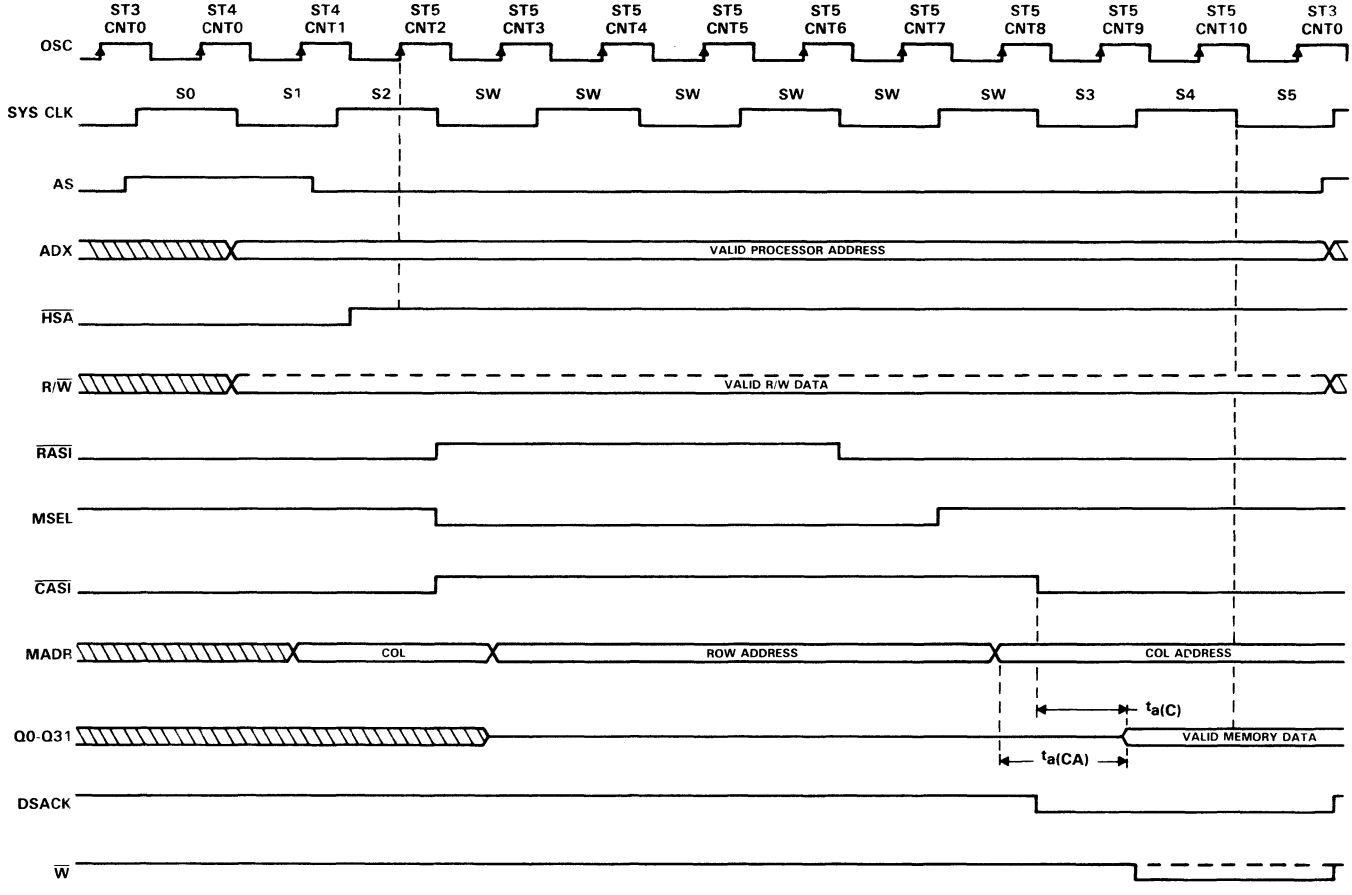

Figure 7. Extended Access Cycle

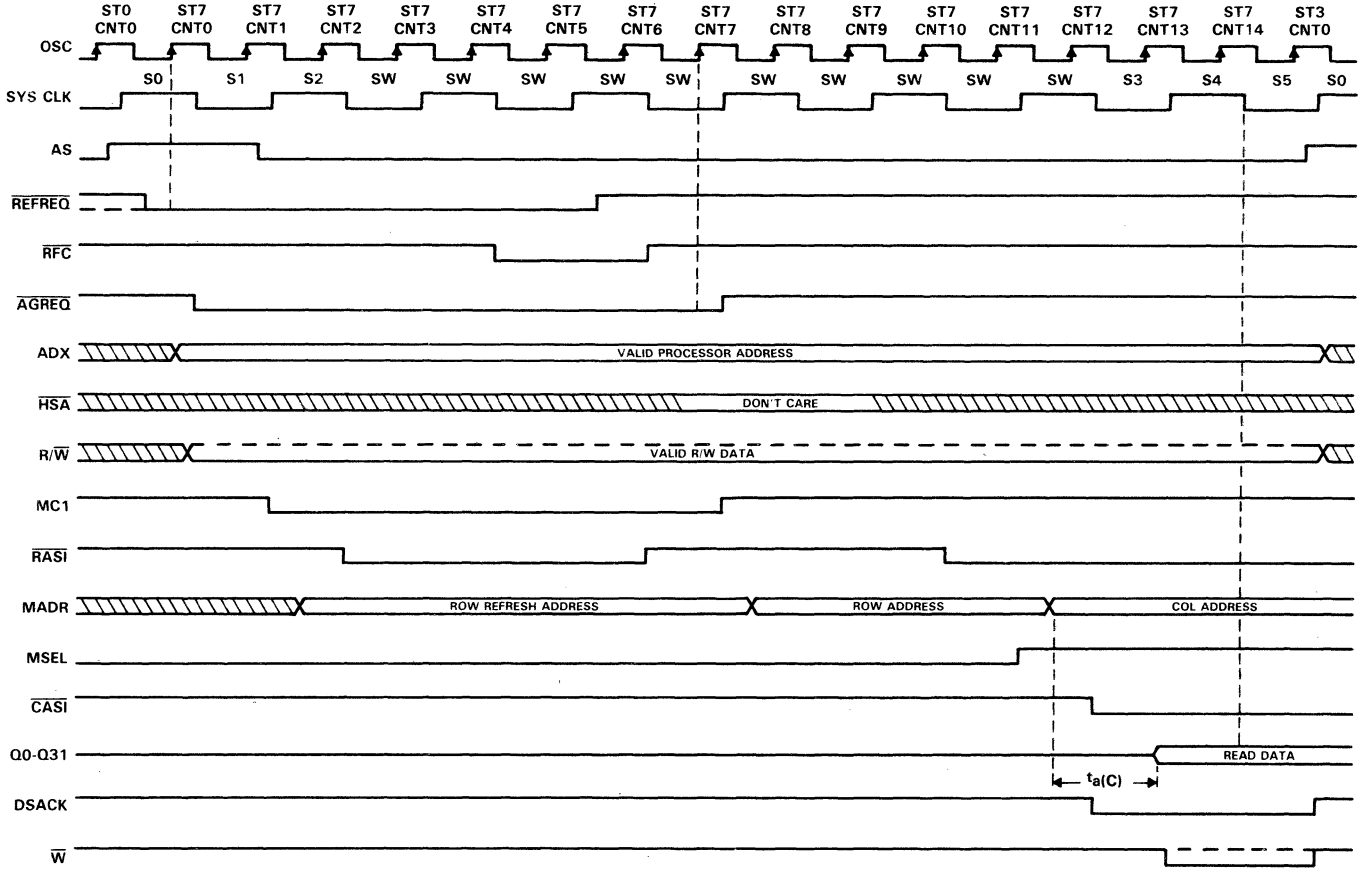

Figure 8. Normal Refresh/Access Grant Cycle

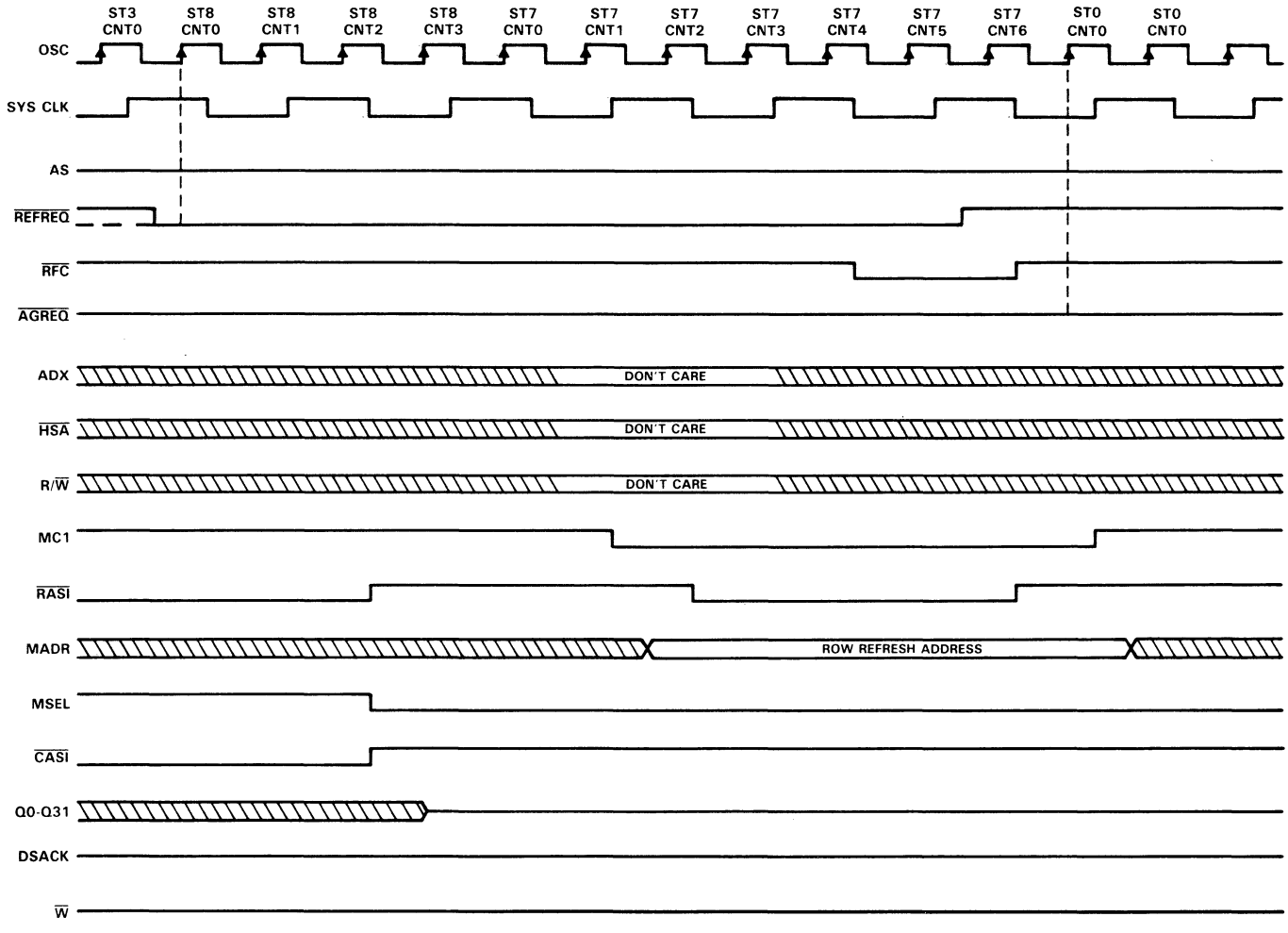

Figure 9. Extended Refresh Cycle

Software Support

The TIBPSG507 is supported by two software packages. CUPL which was created by, and is supported by, Logical Devices Inc. and ABEL, which was created by, and is supported by, FutureNet, a division of Data I/O Corp. Both of these software packages have been used to reduce equations and to generate the fusemap necessary to program the TIBPSG507. Appendices A and B show the ABEL™ and CUPL™ source files for the described static column memory timing controller are attached to assist the designer in programming the TIBPSG507.

Since only 54% (43 out of 80) of the TIBPSG507's product terms were used in this design, it will be easy to modify or add to the sequences used to meet specific system requirements. For detailed information on designing with the TIBPSG507 see *A Designer's Guide to the TIBPSG507* application report.

Summary

Static column decode offers the system designer a method for improving system performance in applications where the microprocessor can outperform conventional DRAM access times. By utilizing the 'ALS6310 Static Column Access Detector, the 'ALS6300 Refresh Timer, and the TIBPSG507 Programmable Sequence Generator, a high-performance memory timing controller can be easily developed to take full advantage of static column decode.

APPENDIX A

```
module SCDECODE
title  'ABEL EXAMPLE FOR THE STATIC COLUMN DECODER
              JOSH PEPRAH, TEXAS INSTRUMENTS, OCT 29, 1987'

      DECODE device 'F507';

" Input pin assignments
OSC           pin   1;                        " OSCILLATOR
RESET         pin   2;                        " SYSTEM RESET - WHEN LOW
A22           pin   3;                        " IO/MEMORY - MEMORY ACCESS
RW            pin   4;                        " READ / WRITE ENABLE
REFREQ        pin   5;                        " REFRESH REQUEST
AS            pin   6;                        " ADDR STROBE - ACCESS REQ
HSA           pin   7;                        " HIGH SPEED ACCESS
SYSCLK        pin  17;                        " SYSTEM CLOCK - (OSC/2)

" Output pin and node assignments
RFC           pin   8;  RFC_r    node 47;   " REFRESH COMPLETE
RASI          pin   9;  RASI_r   node 48;   " ROW ADDRESS STROBE
MSEL          pin  10;  MSEL_r   node 49;   " MULTIPLEXER SELECT
CASI          pin  11;  CASI_r   node 50;   " COLUMN ADDRESS STROBE
MC1           pin  13;  MC1_r    node 51;   " MODE CONTROL
W             pin  14;  W_r                  node 52;   " WRITE
DSACK         pin  15;  DSACK_r  node 53;   " DATA STROBE ACKNOWLEDGE


" Internal counter bits & control, and state reg - node declarations
C0,C1,C2,C3,C4,C5  node 55,56,57,58,59,60;
SCLR0         node 25;
CNTHOLD0 node 28;
CNTHOLD1 node 29;  CNTHOLD1_r node 30; " COUNT/HOLD CONTROL REGISTER

" Buried state registers - node declarations

P0     node 31;  P0_r       node 39;       " STATE REGISTER
P1     node 32;  P1_r       node 40;       " STATE REGISTER
P2     node 33;  P2_r       node 41;       " STATE REGISTER
P3     node 34;  P3_r       node 42;       " STATE REGISTER
AGREQ  node 35; AGREQ_r node 43;       " ACCESS GRANT REQUEST STATUS REGISTER

" Set notation is used to represent control, buried state, and output
" registers. This is done to simplify the equations.  The following
" sets are in the form;  register name_ = [set input, reset input]. Note
" that the ouput register pin name specifies the set input.

RFC_              = [RFC, RFC_r];
RASI_             = [RASI, RASI_r];
MSEL_             = [MSEL, MSEL_r];
CASI_             = [CASI, CASI_r];
MC1_              = [MC1, MC1_r];
W_                = [W, W_r];
DSACK_            = [DSACK, DSACK_r];
AGREQ_            = [AGREQ, AGREQ_r];
```

```
" Intermediate declarations for simplification.
" The sets 'high' and 'low' are used to set or reset the S/R
" registers.  Example: RAS1_ := high & RESET; will cause pin 9
" to go high on the next clock edge if input pin 6 is high.

high        = [ 1,  0];
low         = [ 0,  1];
COUNT       = [C3,C2,C1,C0];
STATE_      = [P3,P2,P1,P0];          " STATE REGISTER SET DEFINED
H,L,clk,X   = 1, 0, .C., .X.;

equations

enable RFC  = 1;  "outputs always enabled, pin 17 is only an input

" Initialization when RESET is low
    [RAS1,CAS1,RFC,W,AGREQ,DSACK,MC1,SCLR0] := !RESET;
    [MSEL_r,P0_r,P1_r,P2_r,P3_r]            := !RESET;

" Counter controls defined

SCLR0       =  !RESET
               # STATE_==2 & COUNT==5
               # STATE_==4 & COUNT==0
               # STATE_==5 & COUNT==10
               # STATE_==6 & COUNT==4
               # STATE_==7 & COUNT==6 & (A22 # AGREQ)
               # STATE_==7 & COUNT==14
               # STATE_==8 & COUNT==3;

CNTHOLD1    :=  !RESET
               # STATE_==2 & COUNT==5
               # STATE_==4 & COUNT==0
               # STATE_==5 & COUNT==10
               # STATE_==6 & COUNT==4
               # STATE_==7 & COUNT==6 & (A22 # AGREQ)
               # STATE_==7 & COUNT==14
               # STATE_==8 & COUNT==3;

CNTHOLD1_r :=   STATE_==0 & !REFREQ & RESET
               # STATE_==1 & !A22 & RESET
               # STATE_==3 & !REFREQ & RESET
               # STATE_==3 &  REFREQ &  AS & SYSCLK & RESET;

" Execution of access and refresh sequences
state_diagram STATE_
   State 0:                                          " NEXT
                    case                             " STATE
                     !RESET                             : 0;
                      REFREQ & (!AS  # !SYSCLK)         : 0;
                      REFREQ &  AS & SYSCLK & RESET     : 1;
                     !REFREQ &  RESET                   : 7;
                    endcase;
```

```
" NORMAL ACCESS CYCLE

   State 1:                                              " NEXT
                    case                                 " STATE
                      COUNT==0 & !A22                       : 2;
                      COUNT==0 &  A22                       : 0;
                    endcase;

   State 2:
                    RASI_ := COUNT==0  & low  & RESET;
                    MSEL_ := COUNT==1  & high;
                    CASI_ := COUNT==2  & low  & RESET;
                   DSACK_ := COUNT==2  & low  & RESET;
                      W_  := COUNT==3  & low  & RESET;
                      W_  := COUNT==5  & high;
                   DSACK_ := COUNT==5  & high;
                  if COUNT==5 then 3 else 2;

"HOLDING STATE
   State 3:                                              " NEXT
                    case                                 " STATE
                  (!AS # !SYSCLK) & REFREQ & RESET          : 3;
                   REFREQ &  AS & SYSCLK & RESET            : 4;
                  !REFREQ & RESET                           : 8;
                   endcase;

   State 4:
                  CASI_  := COUNT==0  &  high &  A22;
                  RASI_  := COUNT==0  &  high &  A22;
                  MSEL_  := COUNT==0  &  low  &  A22;
                  RASI_  := COUNT==1  &  high &  HSA;
                  DSACK_ := COUNT==1  &  low  & !HSA;
                  MSEL_  := COUNT==1  &  low  &  HSA;
                  CASI_  := COUNT==1  &  high &  HSA;

                                                       " NEXT
                    case                               " STATE
                      COUNT==0 &  A22  & RESET             : 0;
                      COUNT==0 & !A22  & RESET             : 4;
                      COUNT==1 &  HSA  & RESET             : 5;
                      COUNT==1 & !HSA  & RESET             : 6;
                    endcase;

"EXTENDED ACCESS CYCLE
   State 5:
                    RASI_ := COUNT==5  & low & RESET;
                    MSEL_ := COUNT==6  & high & RESET;
                    CASI_ := COUNT==7  & low & RESET;
                   DSACK_ := COUNT==7  & low & RESET;
                       W_ := COUNT==8  & low & RESET;
                       W_ := COUNT==10 & high;
                   DSACK_ := COUNT==10 & high;
                      if COUNT==10 & RESET then 3 else 5;
```

```
"HIGH SPEED ACCESS
   State 6:
                        W_ := COUNT==2  & low & RESET;
                        W_ := COUNT==4  & high;
                    DSACK_ := COUNT==4  & high;
                       if COUNT==4 then 3 else 6;

"NORMAL REFRESH CYCLE
   State 7:
                    AGREQ_ :=   AS      & low  & RESET;
                      MC1_ := COUNT==0  & low  & RESET;
                     RAS1_ := COUNT==1  & low  & RESET;
                      RFC_ := COUNT==3  & low  & RESET;
                      RFC_ := COUNT==5  & high;
                     RAS1_ := COUNT==5  & high;
                      MC1_ := COUNT==6  & high;
                     RAS1_ := COUNT==9  & low  & RESET;
                     MSEL_ := COUNT==10 & high & RESET;
                     CAS1_ := COUNT==11 & low  & RESET;
                    DSACK_ := COUNT==11 & low  & RESET;
                        W_ := COUNT==12 & low  & RESET;
                        W_ := COUNT==14 & high;
                    DSACK_ := COUNT==14 & high;
                    if COUNT==6 & (A22 # AGREQ) then 0 else 7;
                    if COUNT==14 then 3 else 7;

"EXTENDED REFRESH CYCLE
   State 8:
                     RAS1_ := COUNT==1  & high;
                     MSEL_ := COUNT==1  & low ;
                     CAS1_ := COUNT==1  & high;
                     if COUNT==3 then 7 else 8;


test_vectors  'NORMAL ACCESS CYCLE'

([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE_])
 [clk,  L  , X , X,  X   , X, X ,   X  ,  X  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
 [clk,  H  , X , X,  H   , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
 [clk,  H  , X , X,  H   , H, X ,   H  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  1   ];
 [clk,  H  , L , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  1  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  2   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  5  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];

test_vectors  'HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE_])
 [clk,  H  , H , X,  H   , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4   ];
 [clk,  H  , L , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4   ];
 [clk,  H  , X , X,  X   , X, H ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5   ];
```

```
test_vectors  'EXTENDED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , X , X,  X   , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  4  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  5  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  6  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  7  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  8  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  9  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  5   ];
 [clk,  H  , X , X,  X   , X, X ,   X  , 10  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];

test_vectors  'HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , H , X,  H   , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4   ];
 [clk,  H  , L , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4   ];
 [clk,  H  , L , X,  X   , X, L ,   X  ,  1  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  6   ];

test_vectors  'HIGH SPEED ACCESS'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , X , X,  X   , X, X ,   X  ,  2  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  3  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  6   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  4  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];

test_vectors  'NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , H , X,  H   , H, X ,   H  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  4   ];
 [clk,  H  , H , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
 [clk,  H  , X , X,  H   , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
 [clk,  H  , X , X,  H   , X, X ,   L  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
 [clk,  H  , X , X,  L   , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];

test_vectors  'NORMAL REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , X , X,  X   , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  X   , L, X ,   X  ,  1  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  X   , L, X ,   X  ,  2  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  X   , L, X ,   X  ,  3  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  X   , L, X ,   X  ,  4  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  H   , L, X ,   X  ,  5  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7   ];
 [clk,  H  , X , X,  X   , L, X ,   X  ,  6  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  0   ];
```

```
test_vectors  'NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
[clk,  H  , X , X,  L   , X, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];
[clk,  H  , X , X,  X   , L, X ,   X  ,  0  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , X , X,  X   , L, X ,   X  ,  1  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , X , X,  X   , H, X ,   X  ,  2  ] -> [ H ,  L ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , X , X,  X   , H, X ,   X  ,  3  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , X , X,  X   , L, X ,   X  ,  4  ] -> [ L ,  L ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , L , X,  H   , L, X ,   X  ,  5  ] -> [ H ,  H ,  L ,  H , L ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  ,  6  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  ,  7  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  ,  8  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  ,  9  ] -> [ H ,  L ,  L ,  H , H ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  , 10  ] -> [ H ,  L ,  H ,  H , H ,H,  H  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  , 11  ] -> [ H ,  L ,  H ,  L , H ,H,  L  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  , 12  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  , 13  ] -> [ H ,  L ,  H ,  L , H ,L,  L  ,  7   ];
[clk,  H  , L , X,  X   , L, X ,   X  , 14  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];

test_vectors  'HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , X , X,  H   , X, X ,   L  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];
 [clk,  H  , X , X,  H   , L, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  3   ];
 [clk,  H  , X , X,  L   , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8   ];

test_vectors  'EXTENDED REFRESH CYCLE'
([OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT] -> [RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE_])
 [clk,  H  , X , X,  X   , X, X ,   X  ,  0  ] -> [ H ,  L ,  H ,  L , H ,H,  H  ,  8   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  1  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  2  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  8   ];
 [clk,  H  , X , X,  X   , X, X ,   X  ,  3  ] -> [ H ,  H ,  L ,  H , H ,H,  H  ,  7   ];


end SCDECODE
```

APPENDIX B

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*************************************************************************************/
/*   Static Column Decode                                                            */
/*                                                                                   */
/*                                                                                   */
/*        This is an example of how the PSG507 can be used to generate the           */
/*   required memory timing control signals (RAS, CAS, MSEL etc) for static          */
/*   column decode implementation using the ALS6301, ALS6310 and the ALS630          */
/*   ALS6300, in a system environment.                                               */
/*                                                                                   */
/*                                                                                   */
/*************************************************************************************/
/*   Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507                      */
/*************************************************************************************/

/**  Inputs  **/

pin  1          =  OSC      ;          /* Oscillator                          */
pin  2          =  RESET    ;          /* System Reset - when low             */
pin  3          =  A22      ;          /* IO/!M - Memory access               */
pin  4          =  RW       ;          /* Read / Write  Enable                */
pin  5          =  REFREQ   ;          /* Refresh Request                     */
pin  6          =  AS       ;          /* Addr Strobe - access request        */
pin  7          =  HSA      ;          /* High Speed Access                   */
pin 18          =  SYSCLK   ;          /* System Clock - (OSC/2)              */

/**  Outputs  **/

pin  8          =  RFC      ;          /* Refresh Complete                    */
pin  9          =  RAS1     ;          /* Row Address Strobe                  */
pin 10          =  MSEL     ;          /* Multiplexer Select                  */
pin 11          =  CAS1     ;          /* Column Address Strobe               */
pin 13          =  MC1_     ;          /* Mode Control                        */
pin 14          =  W        ;          /* Write                               */
pin 15          =  DSACK    ;          /* Data Strobe Acknowledge             */

/** Node Declarations **/
pinnode [33..38] = [C0..5]  ;          /* Built-in 6-Bit counter              */
pinnode 39       = SCLR0    ;          /* Counter Cclear- non registered      */
pinnode 41       = CNTHOLD0 ;          /* Counter Hold - non registered       */
pinnode 42       = CNTHOLD1 ;          /* Counter Hold - registered           */
node               [P3..0]  ;          /* Buried State Registers              */
node               AGREQ    ;          /* Access Grant Request                */
```

```
/** Declarations and Intermediate Variable Definition **/
field COUNT      = [C5..0]   ;
field STATE      = [P3..0]   ;
$define ST0        'b'0000
$define ST1        'b'0001
$define ST2        'b'0010
$define ST3        'b'0011
$define ST4        'b'0100
$define ST5        'b'0101
$define ST6        'b'0110
$define ST7        'b'0111
$define ST8        'b'1000

/* BUILT-IN COUNTER CONTROL EQUATIONS */

SCLR0        = !RESET                          /* Clear counter when RESET is low        */
             # ST2 & COUNT:'d'5                 /* and during transitions at the end      */
             # ST4 & COUNT:'d'0                 /* the indicated states and counts.       */
             # ST5 & COUNT:'d'10                /*                                        */
             # ST6 & COUNT:'d'4                 /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ) /*                                        */
             # ST7 & COUNT:'d'14                /*                                        */
             # ST8 & COUNT:'d'3;                /*                                        */

CNTHOLD1.s   = !RESET                          /* Set count hold while clearing          */
             # ST2 & COUNT:'d'5                 /* the counters accordingly.              */
             # ST4 & COUNT:'d'0                 /*                                        */
             # ST5 & COUNT:'d'10                /*                                        */
             # ST6 & COUNT:'d'4                 /*                                        */
             # ST7 & COUNT:'d'6 & (A22 & AGREQ) /*                                        */
             # ST7 & COUNT:'d'14                /*                                        */
             # ST8 & COUNT:'d'3;                /*                                        */

 CNTHOLD1.r  = ST0 & !REFREQ & RESET            /* Reset count hold on transition to ST7  */
             # ST1 & !A22 & RESET               /* Reset count hold on transition to ST2  */
             # ST3 & !REFREQ & RESET            /* Reset count hold on transition to ST8  */
             # ST3 &  REFREQ &  AS              /* Reset count hold on transition to ST4  */
                  & SYSCLK & RESET;

/** State Machine Equations **/
sequence STATE {
present ST0:
       if(REFREQ & (!AS  # !SYSCLK))       next ST0;
       if(REFREQ &  AS & SYSCLK & RESET)   next ST1;
       if(!REFREQ &  RESET)                next ST7;
       default                             next ST0;

present ST1:
       if(COUNT:'d'0 & !A22)               next ST2;
       if(COUNT:'d'0 &  A22)               next ST0;
       default                             next ST1;

present ST2:
       /* NORMAL ACCESS CYCLE */
       if(COUNT:'d'0) &  RESET             next ST2 out !RAS1;
       if(COUNT:'d'1)                      next ST2 out  MSEL;
       if(COUNT:'d'2) & RESET              next ST2 out [!CAS1,!DSACK];
       if(COUNT:'d'3) & RESET              next ST2 out !W;
       if(COUNT:'d'5)                      next ST3 out [W,DSACK];
       default                             next ST2;
```

```
present ST3:
        /* HOLDING STATE    */
        if(!AS # !SYSCLK) & REFREQ & RESET   next ST3;
        if(REFREQ &  AS & SYSCLK & RESET)    next ST4;
        if(!REFREQ & RESET)                  next ST8;
        default                              next ST3;

present ST4:
        if(COUNT:'d'0) & A22 & RESET         next ST0 out [RAS!,!MSEL,CAS!];
        if(COUNT:'d'0) & !A22 & RESET        next ST4;
        if(COUNT:'d'1) & HSA & RESET         next ST5 out [RAS!,!MSEL,CAS!];
        if(COUNT:'d'1) & !HSA & RESET        next ST6 out !DSACK;
        default                              next ST4;

present ST5:
        /* EXTENDED ACCESS CYCLE */
        if(COUNT:'d'5) & RESET               next ST5 out !RAS!;
        if(COUNT:'d'6) & RESET               next ST5 out  MSEL;
        if(COUNT:'d'7) & RESET               next ST5 out [!CAS!,!DSACK];
        if(COUNT:'d'8) & RESET               next ST5 out !W;
        if(COUNT:'d'10) & RESET              next ST3 out [W,DSACK];
        default                              next ST5;

present ST6:
         /* HIGH SPEED ACCESS    */
         if(COUNT:'d'2) & RESET              next ST6 out !W;
         if(COUNT:'d'4)                      next ST3 out [W,DSACK];
         default                             next ST6;

present ST7:
         /* NORMAL REFRESH CYCLE */
         if AS                               next ST7 out !AGREQ;
         if(COUNT:'d'0) & RESET              next ST7 out !MC1_;
         if(COUNT:'d'1) & RESET              next ST7 out !RAS!;
         if(COUNT:'d'3) & RESET              next ST7 out !RFC;
         if(COUNT:'d'5)                      next ST7 out [RFC,RAS!];
         if(COUNT:'d'6) & (A22 # AGREQ)      next ST0 out  MC1_;
         if(COUNT:'d'6) & !A22 & !AGREQ      next ST7 out  MC1_;
         if(COUNT:'d'9) & RESET              next ST7 out !RAS!;
         if(COUNT:'d'10) & RESET             next ST7 out  MSEL;
         if(COUNT:'d'11) & RESET             next ST7 out [!CAS!,!DSACK];
         if(COUNT:'d'12) & RESET             next ST7 out !W;
         if(COUNT:'d'14)                     next ST3 out [W,DSACK];
         default                             next ST7;

present ST8:
         /* EXTENDED REFRESH CYCLE   */
         if(COUNT:'d'1)                      next ST8 out [RAS!,!MSEL,CAS!];
         if(COUNT:'d'3)                      next ST7;
         default                             next ST8; }

APPEND RAS!.s = !RESET; APPEND CAS!.s  = !RESET; APPEND RFC.s   = !RESET;
APPEND W.s    = !RESET; APPEND AGREQ.s = !RESET; APPEND DSACK.s = !RESET;
APPEND MC1_.s = !RESET; APPEND SCLR0   = !RESET; APPEND MSEL.r  = !RESET;
APPEND P0_.r  = !RESET; APPEND P1_.r   = !RESET; APPEND P2_.r    = !RESET;
APPEND P3_.r  = !RESET;
```

```
NAME      SCDECODE;
PARTNO    T10004;
DATE      05/07/87 ;
REV       01 ;
DESIGNER  Breuninger/Peprah;
COMPANY   Texas Instruments;
ASSEMBLY  None ;
LOCATION  Dallas;

/*****************************************************************************************/
/* Static Column Decode                                                                  */
/*                                                                                       */
/*      CUPL simulation file for the Static Column Decode Application                    */
/*                                                                                       */
/*****************************************************************************************/
/*  Allowable Target Device Types :  TEXAS INTSRUMENTS  PSG507                           */
/*****************************************************************************************/

ORDER:  OSC,%4,RESET,%4,A22,%3,RW,%3,REFREQ,%5,AS,%2,HSA,%5,SYSCLK,%3,COUNT,
        %2,RFC,%4,RASI,%4,MSEL,%4,CASI,%3,MCI_,%2,W,%3,DSACK,%4,STATE;

BASE: DECIMAL;

VECTORS:

$msg"   ";
$msg"   ";
$msg"NORMAL ACCESS CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C    0    X   X   X     X  X     X    'X'    H    H    L    H    H   H    H    "0"
          C    1    X   X   1     0  X     X    '0'    H    H    L    H    H   H    H    "0"
          C    1    X   X   1     1  X     1    '0'    H    H    L    H    H   H    H    "1"
          C    1    0   X   X     X  X     X    '0'    H    H    L    H    H   H    H    "2"
          C    1    X   X   X     X  X     X    '0'    H    L    L    H    H   H    H    "2"
          C    1    X   X   X     X  X     X    '1'    H    L    H    H    H   H    H    "2"
          C    1    X   X   X     X  X     X    '2'    H    L    H    L    H   H    L    "2"
          C    1    X   X   X     X  X     X    '3'    H    L    H    L    H   L    L    "2"
          C    1    X   X   X     X  X     X    '4'    H    L    H    L    H   L    L    "2"
          C    1    X   X   X     X  X     X    '5'    H    L    H    L    H   H    H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH EXTENDED ACCESS REQUEST";
$msg"   ";
$msg"     ----------------- INPUT -------------------  -------------- OUTPUT ------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C    1    1   X   1     1  X     1    '0'    H    L    H    L    H   H    H    "4"
          C    1    0   X   X     X  X     X    '0'    H    L    H    L    H   H    H    "4"
          C    1    X   X   X     X  1     X    '1'    H    H    L    H    H   H    H    "5"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   X     X  X     X    '2'    H    H    L    H   H  H   H    "5"
          C   1   X   X   X     X  X     X    '3'    H    H    L    H   H  H   H    "5"
          C   1   X   X   X     X  X     X    '4'    H    H    L    H   H  H   H    "5"
          C   1   X   X   X     X  X     X    '5'    H    L    L    H   H  H   H    "5"
          C   1   X   X   X     X  X     X    '6'    H    L    H    H   H  H   H    "5"
          C   1   X   X   X     X  X     X    '7'    H    L    H    L   H  H   L    "5"
          C   1   X   X   X     X  X     X    '8'    H    L    H    L   H  L   L    "5"
          C   1   X   X   X     X  X     X    '9'    H    L    H    L   H  L   L    "5"
          C   1   X   X   X     X  X     X   '10'    H    L    H    L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 4 WITH HIGH SPEED ACCESS REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   1   X   1     1  X     1    '0'    H    L    H    L   H  H   H    "4"
          C   1   0   X   X     X  X     X    '0'    H    L    H    L   H  H   H    "4"
          C   1   0   X   X     X  0     X    '1'    H    L    H    L   H  H   L    "6"

$msg"   ";
$msg"   ";
$msg"HIGH SPEED ACCESS";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   X   X   X     X  X     X    '2'    H    L    H    L   H  L   L    "6"
          C   1   X   X   X     X  X     X    '3'    H    L    H    L   H  L   L    "6"
          C   1   X   X   X     X  X     X    '4'    H    L    H    L   H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"NON-MEMORY ACCESS FOLLOWED BY REFRESH REQUEST";
$msg"   ";
$msg"     ------------------ INPUT ------------------  ------------- OUTPUT ---------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------------ ";
          C   1   1   X   1     1  X     1    '0'    H    L    H    L   H  H   H    "4"
          C   1   1   X   X     X  X     X    '0'    H    H    L    H   H  H   H    "0"
          C   1   X   X   1     0  X     X    '0'    H    H    L    H   H  H   H    "0"
          C   1   X   X   1     X  X     0    '0'    H    H    L    H   H  H   H    "0"
          C   1   X   X   0     X  X     X    '0'    H    H    L    H   H  H   H    "7"
```

```
$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE";
$msg"   ";
$msg"      ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"      OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"      ------------------------------------------------------------------------------- ";
           C    1    X   X   X     0  X     X     '0'   H    H    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '1'   H    L    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '2'   H    L    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '3'   L    L    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '4'   L    L    L    H    L  H   H    "7"
           C    1    X   X   1     0  X     X     '5'   H    H    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '6'   H    H    L    H    H  H   H    "0"

$msg"   ";
$msg"   ";
$msg"NORMAL REFRESH CYCLE FOLLOWED BY ACCESS GRANT REQUEST";
$msg"   ";
$msg"      ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"      OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"      ------------------------------------------------------------------------------- ";
           C    1    X   X   0     X  X     X     '0'   H    H    L    H    H  H   H    "7"
           C    1    X   X   X     0  X     X     '0'   H    H    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '1'   H    L    L    H    L  H   H    "7"
           C    1    X   X   X     1  X     X     '2'   H    L    L    H    L  H   H    "7"
           C    1    X   X   X     1  X     X     '3'   L    L    L    H    L  H   H    "7"
           C    1    X   X   X     0  X     X     '4'   L    L    L    H    L  H   H    "7"
           C    1    0   X   X     0  X     X     '5'   H    H    L    H    L  H   H    "7"
           C    1    0   X   X     0  X     X     '6'   H    H    L    H    H  H   H    "7"
           C    1    0   X   X     0  X     X     '7'   H    H    L    H    H  H   H    "7"
           C    1    0   X   X     0  X     X     '8'   H    H    L    H    H  H   H    "7"
           C    1    0   X   X     0  X     X     '9'   H    L    L    H    H  H   H    "7"
           C    1    0   X   X     0  X     X     '10'  H    L    H    H    H  H   H    "7"
           C    1    0   X   X     0  X     X     '11'  H    L    H    L    H  H   L    "7"
           C    1    0   X   X     0  X     X     '12'  H    L    H    L    H  L   L    "7"
           C    1    0   X   X     0  X     X     '13'  H    L    H    L    H  L   L    "7"
           C    1    0   X   X     0  X     X     '14'  H    L    H    L    H  H   H    "3"

$msg"   ";
$msg"   ";
$msg"HOLDING STATE 3 WITH EXTENDED REFRESH REQUEST";
$msg"   ";
$msg"      ----------------- INPUT -----------------  -------------- OUTPUT --------------- ";
$msg"      OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RAS1,MSEL,CAS1,MC1,W,DSACK,STATE  ";
$msg"      ------------------------------------------------------------------------------- ";
           C    1    X   X   1     X  X     0     '0'   H    L    H    L    H  H   H    "3"
           C    1    X   X   1     0  X     X     '0'   H    L    H    L    H  H   H    "3"
           C    1    X   X   0     X  X     X     '0'   H    L    H    L    H  H   H    "8"
```

```
$msg"   ";
$msg"   ";
$msg"EXTENDED REFRESH CYCLE";
$msg"   ";
$msg"     ----------------- INPUT -----------------  ------------- OUTPUT --------------- ";
$msg"     OSC,RESET,A22,RW,REFREQ,AS,HSA,SYSCLK,COUNT  RFC,RASI,MSEL,CASI,MCI,W,DSACK,STATE  ";
$msg"     ------------------------------------------------------------------------------- ";
          C    I    X   X   X     X  X     X    '0'    H    L    H    L   H  H    H     "8"
          C    I    X   X   X     X  X     X    '1'    H    H    L    H   H  H    H     "8"
          C    I    X   X   X     X  X     X    '2'    H    H    L    H   H  H    H     "8"
          C    I    X   X   X     X  X     X    '3'    H    H    L    H   H  H    H     "7"
```

System Solutions for Hidden Refresh

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Contents

List of Illustrations

Introduction

As part of Texas Instruments Dynamic Memory support chip, Input Selectable Refresh Timer (SN74ALS6300) gives the user a simplified solution of generating refresh frequency and implementing hidden refresh. When combined with Texas Instruments Dynamic Memory Controllers (SN74ALS6301 and SN74ALS6302) and Programmable Sequence Generator (TIBPSG507), DRAM designers have a complete set of memory support chips at their disposal to meet their design needs.

In order to keep up with current processor speeds, it is important to find ways to increase the memory bandwidth. One of the solutions is to implement a hidden refresh scheme. Hidden refresh is implemented under the assumption that there is at least one memory access per refresh period and that access cycles occur in a manner where there is enough time for a refresh cycle between access cycles. Under this assumption, a refresh cycle can be hidden from the processor by refreshing the DRAM immediately after the first memory access of each refresh period.

This application note gives a functional description of the SN74ALS6300 and how it can be used to implement hidden refresh. A detail description of the timing controller for hidden refresh using TIBPSG507 is also provided.

Functional Description

The 'ALS6300 is a modified frequency divider with provisions to meet specific DRAM refresh requirements. It has an internal 10-bit counter that can run at frequencies ranging from 5 MHz to 40 MHz. Table 1 shows the list of different frequencies that can be selected with S3-S0 inputs. In addition to the S3-S0 input signals, RFC and $\overline{\text{RFC}}$, CLK and $\overline{\text{RESET}}$ are the other input signals and MREF, $\overline{\text{MREF}}$, REFREQ, and $\overline{\text{REFREQ}}$ are the output signals provided by 'ALS6300 for system interface.

$\overline{\text{REFREQ}}$ (refresh request) output is activated every refresh period to signal the DRAM controller for a refresh cycle. $\overline{\text{MREF}}$ (mandatory refresh) is provided for hidden refresh implementation. In a normal distributive refresh, $\overline{\text{REFREQ}}$ is the only output signal required for refresh operations where refresh cycle is initiated as soon after the activation of $\overline{\text{REFREQ}}$ as possible. In a hidden refresh operation, $\overline{\text{REFREQ}}$ signals the DRAM controller to initiate a refresh cycle immediately after an access cycle if there is a memory access. $\overline{\text{MREF}}$, on the other hand, signals the timing controller to initiate a refresh cycle as soon as possible. $\overline{\text{MREF}}$ is always activated 20 clock periods before the next activation of $\overline{\text{REFREQ}}$, if $\overline{\text{REFREQ}}$ is still active. $\overline{\text{MREF}}$ indicates to the DRAM controller that a refresh is mandatory and the controller has 20 clock periods to complete a refresh cycle before the next refresh cycle begins.

The selection of S3-S0 sets the internal clock divisor rate so that the selected system clock frequency is divided down to the corresponding refresh rate (see Table 1). The refresh periods in Table 1 are guaranteed to meet the requirements of currently available DRAMs. $\overline{\text{RFC}}$, refresh complete signal, resets the $\overline{\text{REFREQ}}$ and $\overline{\text{MREF}}$ to their inactive states. This input signal is the indication from the DRAM timing controller that a refresh cycle has been

completed. A synchronous reset ($\overline{\text{RESET}}$) is provided for system reset where a low level on this input clears the ALS6300's counter and drives $\overline{\text{REFREQ}}$ and $\overline{\text{MREF}}$ signals to their inactive states.

For design flexibility, both active high and active low options are available for REFREQ, MREF, and RFC signals. The range of frequencies for 'ALS6300 is chosen to support the clock frequencies of the most widely used processors.

Table 1. System Clock Selection

Select Inputs				CPU Clock Frequencies (MHz)	Clock Divisor	Refresh Periods (μs)	% Chance of Hidden Refresh
S3	S2	S1	S0				
L	L	L	L	5	77	15.4	74.0
L	L	L	H	6	93	15.5	78.5
L	L	H	L	7.5	116	15.5	82.8
L	L	H	H	8	124	15.5	83.9
L	H	L	L	10	155	15.5	87.1
L	H	L	H	11	171	15.5	88.3
L	H	H	L	12	186	15.5	89.2
L	H	H	H	12.5	194	15.5	89.7
H	L	L	L	15	233	15.5	91.4
H	L	L	H	16	248	15.5	91.9
H	L	H	L	18	280	15.5	92.9
H	L	H	H	20	310	15.5	93.5
H	H	L	L	24	373	15.5	94.6
H	H	L	H	25	389	15.6	94.9
H	H	H	L	33	511	15.5	96.1
H	H	H	H	40	625	15.6	96.8

Hidden Refresh

TMS4C1024 (1,048,576-bit × 1) DRAM requires that 512 rows of refresh be completed in 8 ms. With access cycles which normally take 500 ns and with the required refresh time of 8 ms, there can be a maximum of 16,000 access cycles without any refresh cycles within each 8 ms of the long refresh period. If an access cycle has to wait for a refresh cycle every time a refresh cycle is taking place, 3.2% of memory availability is lost to refresh. Hidden refresh is one solution to improve the memory performance with minor changes to the DRAM's basic building blocks at little or no cost.

The hidden refresh cycle always follows an access cycle. As the DRAM timing controller makes the transition from the access cycle to the hidden refresh cycle, the column address strobe (CAS) signal is kept active so that the output data of the DRAMs remain valid to the processor while the refresh cycle is taking place. From the processor's point of view, this combination of access cycle and hidden refresh cycle is seen as a long access cycle.

From the DRAM's requirement, there must be one refresh cycle in every refresh period of 15.5 μs. This requirement is satisfied either by a hidden refresh or by a mandatory refresh. A hidden refresh cycle always accompanies the first access cycle of each refresh period, provided the first access cycle occurs within the start of the refresh period and 20 clock periods before the start of the next refresh period. The DRAM timing controller initiates a mandatory refresh cycle if the combination of access cycle and hidden refresh cycle has not been completed at 20 clock periods before the next refresh period.

The only time the hidden refresh scheme will suffer a penalty in access time is when a normal access cycle follows right after the hidden refresh cycle. Due to the delay time to complete the hidden refresh cycle before starting the access cycle, this access cycle requires a longer period of time than a normal access cycle. Under the basic assumption of implementing hidden refresh, the occurrence of hidden refresh followed by normal access cycle is very rare.

Timing Controller Details

The flowchart for the timing controller of Figure 1 is shown in Figure 2. As can be seen from the flowchart, there are five different states. State 0 initializes the outputs of the timing controller during reset and between transitions of states. State 1 and state 3 initiates the mandatory refresh cycle and hidden refresh cycle, respectively. Normal access cycle is initiated during state 2 and access grant cycle is initiated in state 4.

State 0 initializes MC1, $\overline{\text{RAS}}$, $\overline{\text{DSACK}}$, $\overline{\text{CAS}}$, $\overline{\text{RFCAS}}$, MSEL, and RFC outputs to their respective logic levels as shown in the flowchart. In addition to the outputs, internal register for access request, REQ, is also initialized. A system reset in any other state forces the timing controller to state 0. From state 0, the status of the mandatory refresh request (MREF) from 'ALS6300 determines whether the timing controller goes to state 1 for mandatory refresh cycle or to continue with the decision, based on the $\overline{\text{AS}}$ and CLK signals, to go to state 2 for a normal access cycle.

Mandatory refresh cycle gets initiated when active logic level on $\overline{\text{MREF}}$ forces the timing controller to state 1. The timing diagrams in Figure 5 shows the sequence of events during a mandatory refresh cycle. If there is an access request while the refresh sequence is in progress, the internal register signal REQ is activated. At the end of the refresh cycle, REQ signal becomes the determining factor to go to state 4 for an access grant cycle if there was a pending request. Figure 5 also shows the $\overline{\text{RFCAS}}$ signal for the purpose of driving $\overline{\text{CAS}}$0-$\overline{\text{CAS}}$3 low via the CAS decoder as required by the CAS-before-RAS refresh sequence. Refresh complete signal (RFC) in state 1 sets the $\overline{\text{REFREQ}}$ and $\overline{\text{MREF}}$ outputs of the 'ALS6300 to their inactive states.

A normal access cycle in state 2 is initiated based on the $\overline{\text{AS}}$ and CLK signals. Once in state 2, A23 (M/IO) signal is checked to determine whether the access requested is a memory request or an I/O request. Figure 3 shows the timing diagram for a normal access cycle. After completing the access cycle, activation of refresh request ($\overline{\text{REFREQ}}$) signal

from 'ALS6300 forces the timing controller into state 3 for a hidden refresh cycle. This transition sequence from access cycle to hidden refresh cycle is shown in Figure 4.

The sequence of events of the hidden refresh cycle in state 3 is similar to the mandatory refresh cycle. Access request is saved in the internal register and indicated with REQ signal for the access grant sequence in state 4. Figure 4 shows an access cycle accompanied by a hidden refresh cycle. Notice that $\overline{CASI}$ signal is kept low throughout the transition from access cycle to refresh cycle to keep the data output of the DRAM valid for the duration of the refresh cycle. $\overline{RFCAS}$ is also provided as in mandatory refresh cycle so that CAS-before-RAS refresh is performed on the banks of DRAMs that are not being accessed. RFC signal of this refresh cycle has the same effect on the 'ALS6300 as in state 1.

Finally, the timing diagram of the access grant cycle in state 4 is shown in Figure 5 as following the mandatory refresh cycle. After completing either of the refresh cycles, M/IO signal and REQ signal determine the start of the access grant sequence. If there is no pending access request after either of the refresh cycles, the timing controller returns to state 0. The sequence of events for the access grant cycle is identical to the sequence of events in the normal access cycle. After completing the access grant cycle, the timing controller returns to state 0.

The timing controller was developed using the TIBPSG507, a programmable sequence generator. Sample ABEL™ and CUPL™ source files along with the functional test patterns are given in the appendix for reference. These source files can be changed to customize the timing controller to meet the designer's need.

CAS Decoder

CAS decoder takes $\overline{CAS0}$-$\overline{CAS3}$ from the DRAM controller and $\overline{RFCAS}$ from the timing controller as its inputs. For a normal access cycle, output $\overline{CAS}$ ($\overline{OCAS0}$-$\overline{OCAS3}$) are identical to the input $\overline{CAS}$ ($\overline{ICAS0}$-$\overline{ICAS3}$). During a refresh cycle, the refresh $\overline{CAS}$ ($\overline{RCAS}$) takes over to force all output $\overline{CAS}$ to their active levels.

The CAS decoder is implemented with a TIBPAL16L8-10. Also given in the appendix are the ABEL™ and CUPL™ source files for the CAS decoder. An option to this design is to have the RAS-only refresh instead of the CAS-before-RAS refresh. For this option, the CAS decoder can be eliminated. One disadvantage of the RAS-only refresh is that the data output of the DRAM is not available to the processor during the hidden refresh cycle.

Software Support

The TIBPSG507 is supported by two software packages. CUPL™ which is supported by Logical Devices and ABEL™ which was created by and is supported by FutureNet, a division of Data I/O Corp. Both of these software packages have been used to reduce equations and to generate the fusemap necessary to program the TIBPSG507 and

ABEL is a trademark of FutureNet, a division of Data I/O Corporation.
CUPL is a trademark of Logical Devices, Inc.

TIBPAL16L8. For additional information on designing with the TIBPSG507, see *A Designer's Guide to the TIBPSG507* application report (SDPA003A).

Summary

Although hidden refresh implementation increases the memory bandwidth by approximately 3%, it is achieved with very little cost. By generating the refresh request signals with the 'ALS6300, the hidden refresh scheme can be implemented with the same building blocks as the requirement of the minimun DRAM system. While providing a ready made memory refresh timer, SN74ALS6300 is versatile enough to give the system designer the option of hidden refresh.

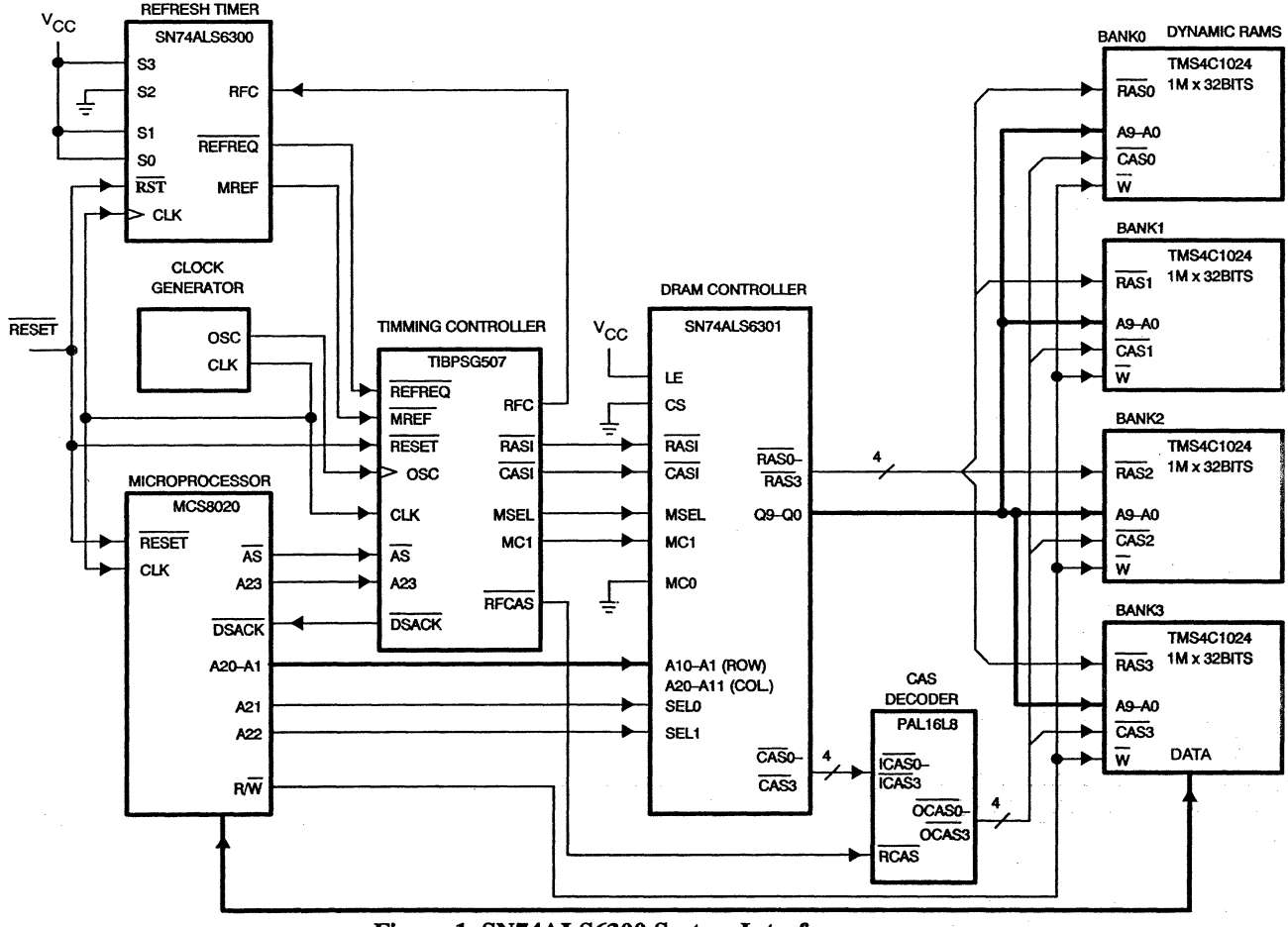

Figure 1. SN74ALS6300 System Interface

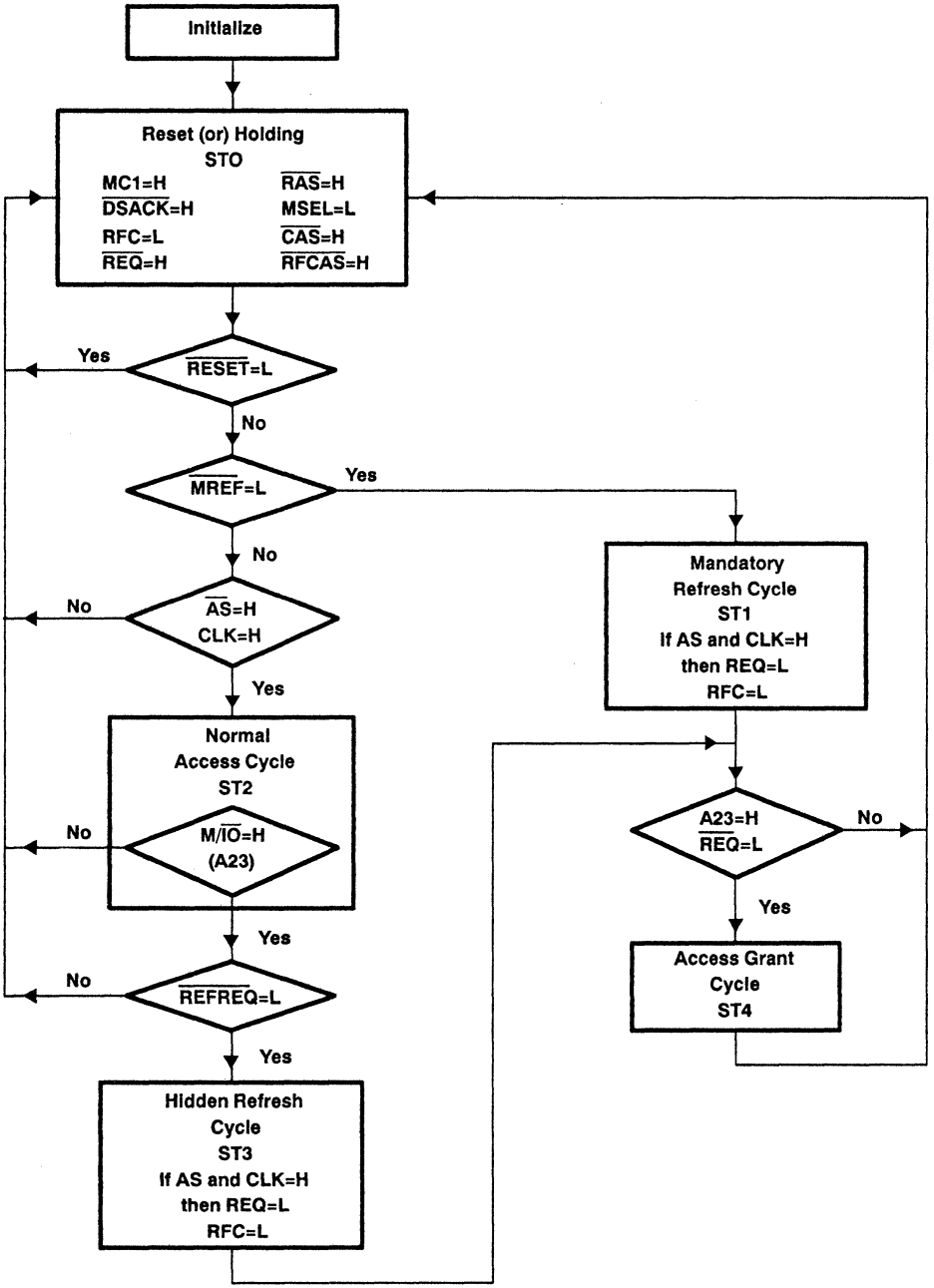

Figure 2. DRAM Timing Controller Flowchart with Hidden Refresh

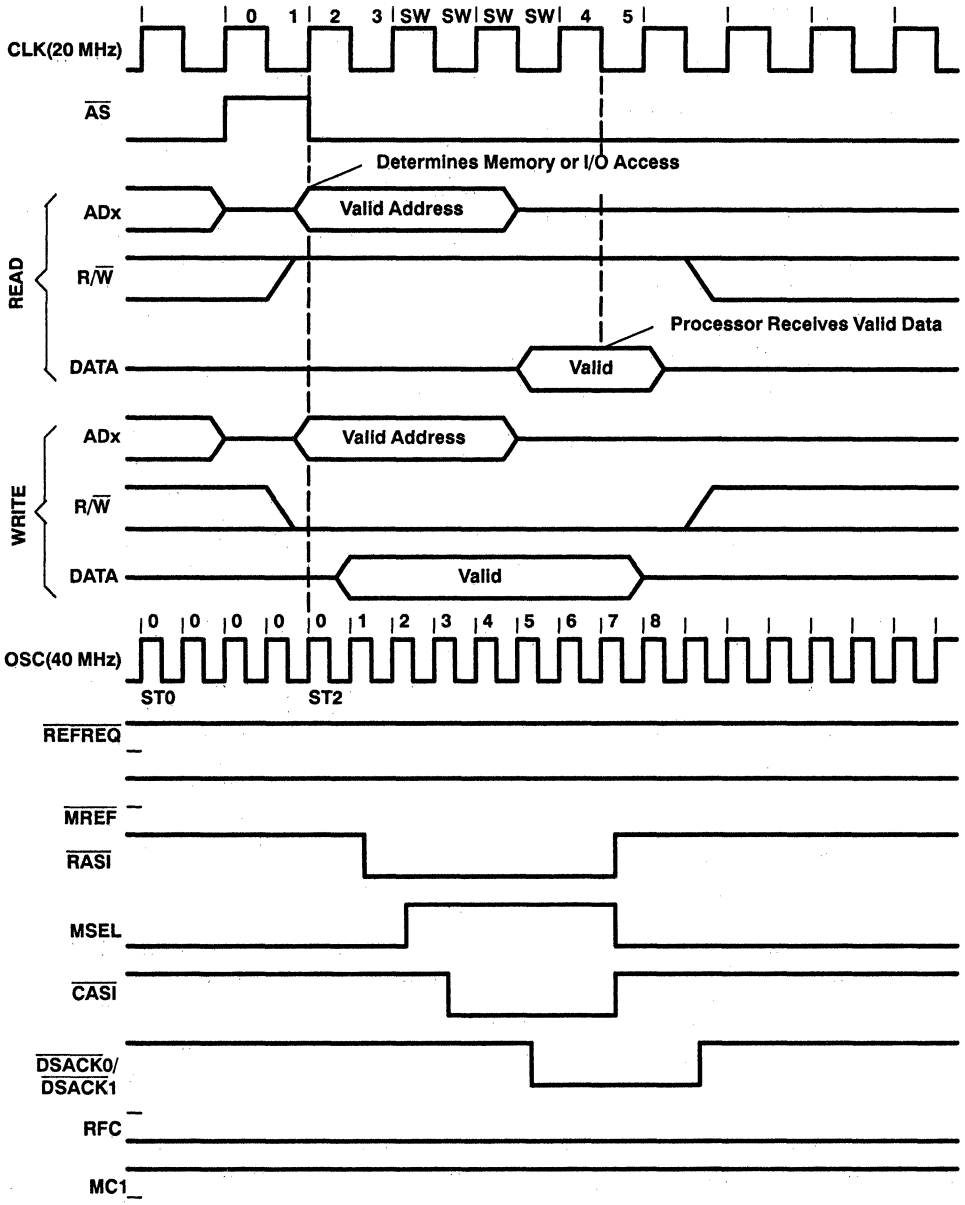

Figure 3. Normal Access Cycle

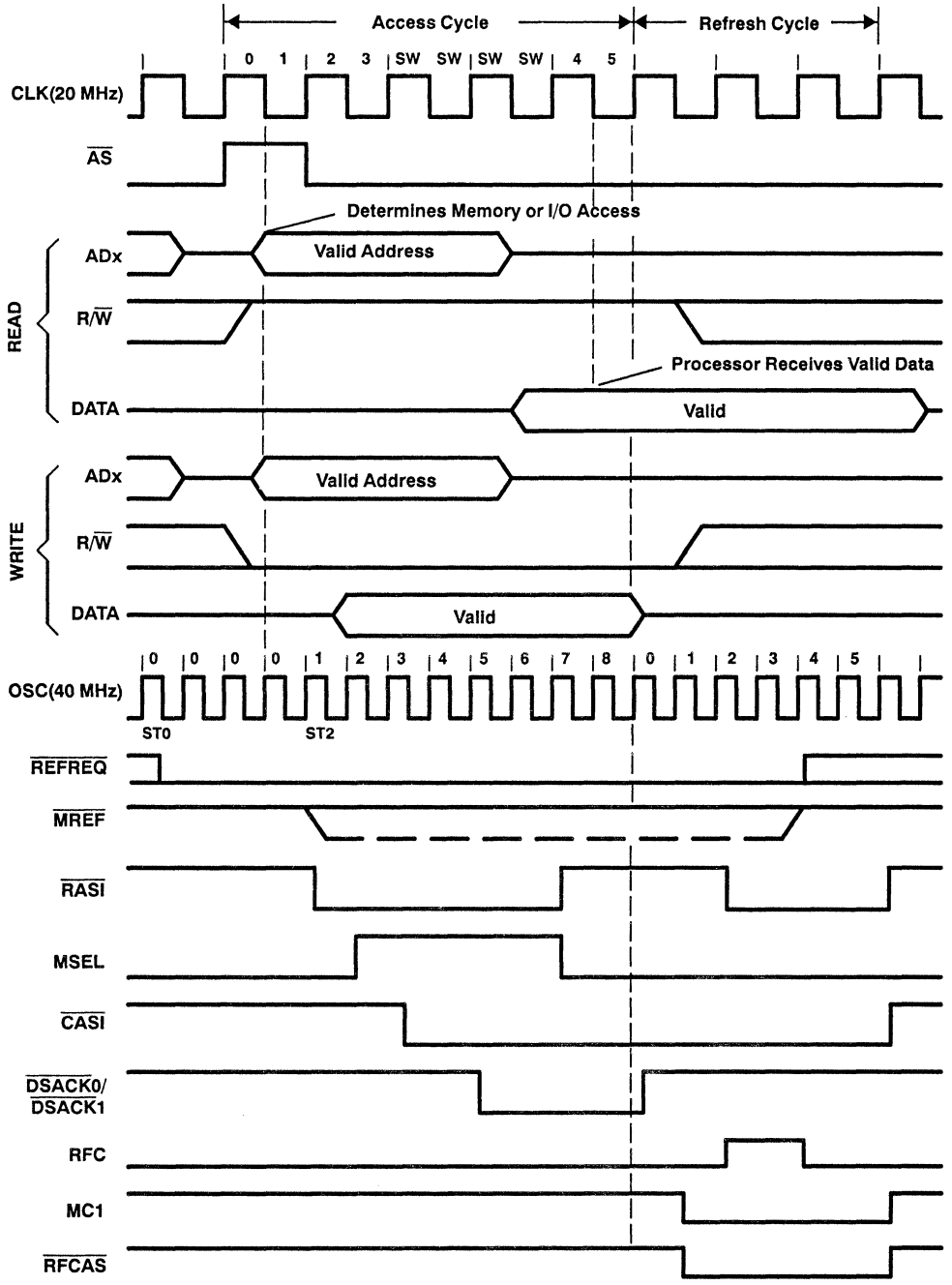

Figure 4. Access/Refresh Cycle (Hidden Refresh)

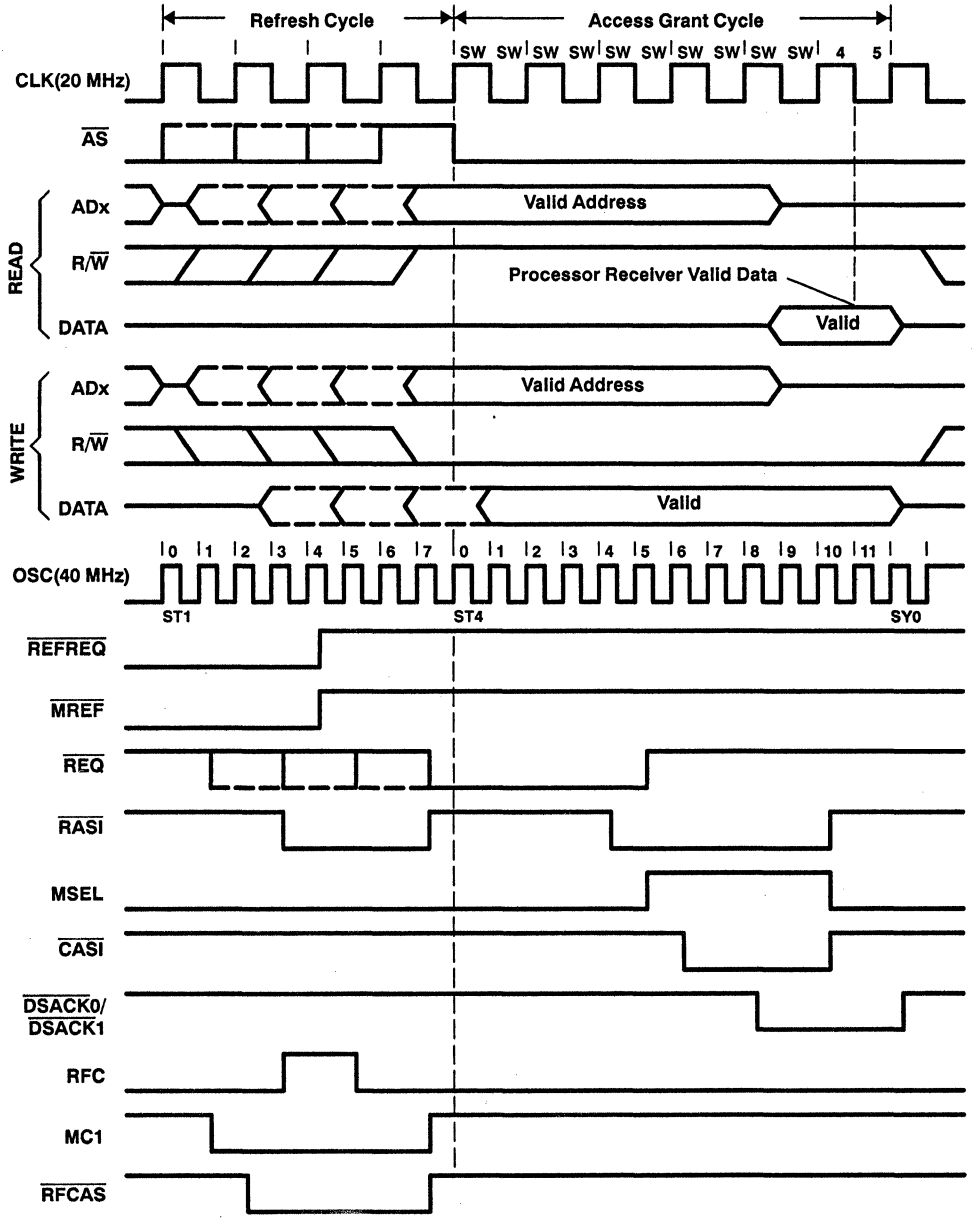

Figure 5. Mandatory Refresh/Access Grant Cycle

Appendix

```
module _HRFT flag '-F1'

title 'DRAM TIMING CONTROLLER WITH HIDDEN REFRESH
       BERTRAND LEIGH, TEXAS INSTRUMENTS, DECEMBER 17, 1987'

        HRFT device 'F507';

"Input pin assignments
  OSC       PIN 1;          " timing controller's input clock
  RESET_    PIN 2;          " system reset (active low)
  REFREQ_   PIN 3;          " refresh request
  MREF_     PIN 4;          " mandatory refresh request
  AS_       PIN 5;          " address strobe
  A23       PIN 6;          " memory/IO access indicator (memory access
                            " when high)
  CLK       PIN 7;          " system clock for synchronization (OSC/2)

"Output pin assignments
  RASI_     PIN 8;      RRASI_     NODE 47;   "row address strobe
  CASI_     PIN 9;      RCASI_     NODE 48;   "column address strobe
  MSEL      PIN 10;     RMSEL      NODE 49;   "row/col. mux select
  MC1       PIN 11;     RMC1       NODE 50;   "mode select
  RFC       PIN 13;     RRFC       NODE 51;   "refresh complete
  DSACK_    PIN 14;     RDSACK_    NODE 52;   "data transfer acknowledge
  RFCAS_    PIN 15;     RRFCAS_    NODE 53;   "refresh CAS

"Internal counter bits and control node declarations
  C0,C1,C2,C3,C4,C5    NODE 55,56,57,58,59,60;
  SCLR0       NODE 25;
  CNT_HLD0    NODE 28;
  CNT_HLD1    NODE 29;      RCNT_HLD1     NODE 30;

"Buried state registers node declarations
  P0     NODE 31;    RP0     NODE 39;        " state register
  P1     NODE 32;    RP1     NODE 40;        " state register
  P2     NODE 33;    RP2     NODE 41;        " state register
  REQ_   NODE 34;    RREQ_   NODE 42;        " access request status


"Intermediate declaration
  STATE_   = [P2,P1,P0];
  COUNT    = [C5,C4,C3,C2,C1,C0];
  H,L,C,X  = 1,0,.C.,.X.;

  HIGH = [1,0];
  LOW  = [0,1];

  XRASI_  = [RASI_,RRASI_];
  XCASI_  = [CASI_,RCASI_];
  XMSEL   = [MSEL,RMSEL];
  XMC1    = [MC1,RMC1];
  XRFC    = [RFC,RRFC];
  XDSACK_ = [DSACK_,RDSACK_];
  XREQ_   = [REQ_,RREQ_];
```

```
  XRFCAS_ = [RFCAS_,RRFCAS_];

equations

  [RASI_,CASI_,RFCAS_,MC1,DSACK_,REQ_,SCLR0]    := !RESET_;
  [RMSEL,RRFC,RP0,RP1,RP2]                      := !RESET_;

  SCLR0 = !RESET_
        # (STATE_ == 1) & (COUNT == 7)
        # (STATE_ == 2) & (COUNT == 8)
        # (STATE_ == 2) & (COUNT == 0) & !A23
        # (STATE_ == 3) & (COUNT == 5)
        # (STATE_ == 4) & (COUNT == 11)    ;

  CNT_HLD1 :=   !RESET_
             # (STATE_ == 1) & (COUNT == 7) & !(A23 & !REQ_)
             # (STATE_ == 2) & (COUNT == 8) & REFREQ_
             # (STATE_ == 2) & (COUNT == 0) & !A23
             # (STATE_ == 3) & (COUNT == 5) & !(A23 & !REQ_)
             # (STATE_ == 4) & (COUNT == 11)       ;

  RCNT_HLD1 :=   (STATE_ == 0) & !MREF_ & RESET_
              # (STATE_ == 0) & AS_ & CLK & RESET_
              # (STATE_ == 1) & (COUNT == 7) & (A23 & !REQ_) & RESET_
              # (STATE_ == 2) & (COUNT == 8) & !REFREQ_ & RESET_
              # (STATE_ == 3) & (COUNT == 5) & (A23 & !REQ_) & RESET_

state_diagram STATE_

State 0:                              "RESET OR HOLDING STATE
   XMC1     := HIGH ;
   XDSACK_  := HIGH ;
   XRFC     := LOW  ;
   XREQ_    := HIGH ;
   XRASI_   := HIGH ;
   XCASI_   := HIGH ;
   XMSEL    := LOW  ;
   XRFCAS_  := HIGH ;

   case
       !MREF_ & RESET_           : 1 ;
        AS_ & CLK & RESET_       : 2 ;
   endcase;

State 1:                              "MANDATORY REFRESH CYCLE
   XREQ_    := (AS_ & CLK) & LOW & RESET_   ;
   XRASI_   := (COUNT == 2) & LOW & RESET_  ;
   XRFC     := (COUNT == 2) & HIGH & RESET_ ;
   XMC1     := (COUNT == 0) & LOW & RESET_  ;
   XRFCAS_  := (COUNT == 1) & LOW & RESET_  ;
   XRFC     := (COUNT == 4) & LOW  ;
   XRASI_   := (COUNT == 6) & HIGH ;
   XMC1     := (COUNT == 6) & HIGH ;
   XRFCAS_  := (COUNT == 6) & HIGH ;
   XREQ_    := (COUNT == 7) & !A23 & HIGH ;
```

```
   case
       !RESET_ # !(!REQ_ & A23) & (COUNT == 7)  : 0 ;
       !REQ_ & A23 & (COUNT == 7) & RESET_      : 4 ;
   endcase;

State 2:                              "NORMAL ACCESS CYCLE
   XRASI_      := (COUNT == 0) & LOW & RESET_  ;
   XMSEL       := (COUNT == 1) & HIGH & RESET_ ;
   XCASI_      := (COUNT == 2) & LOW & RESET_  ;
   XDSACK_     := (COUNT == 4) & LOW & RESET_  ;
   XRASI_      := (COUNT == 6) & HIGH  ;
   XMSEL       := (COUNT == 6) & LOW   ;
   XCASI_      := (COUNT == 6) & REFREQ_ & HIGH ;
   XDSACK_     := (COUNT == 8) & HIGH  ;

   case
       !RESET_ # (COUNT == 0) & !A23              : 0 ;
       REFREQ_ & (COUNT == 8) & RESET_            : 0 ;
       !REFREQ_ & (COUNT == 8) & RESET_           : 3 ;
   endcase;

State 3:                              "HIDDEN REFRESH CYCLE
   XREQ_       := (AS_ & CLK) & LOW & RESET_  ;
   XMC1        := (COUNT == 0) & LOW & RESET_ ;
   XRFCAS_     := (COUNT == 0) & LOW & RESET_ ;
   XRASI_      := (COUNT == 1) & LOW & RESET_ ;
   XRFC        := (COUNT == 1) & HIGH & RESET_;
   XRFC        := (COUNT == 3) & LOW  ;
   XRASI_      := (COUNT == 5) & HIGH ;
   XMC1        := (COUNT == 5) & HIGH ;
   XCASI_      := (COUNT == 5) & HIGH ;
   XRFCAS_     := (COUNT == 5) & HIGH ;

   case
       !RESET_ # !(!REQ_ & A23) & (COUNT == 5)   : 0 ;
       !REQ_ & A23 & (COUNT == 5) & RESET_       : 4 ;
   endcase;

State 4:                              "ACCESS GRANT CYCLE
   XREQ_       := (COUNT == 4) & HIGH  ;
   XRASI_      := (COUNT == 3) & LOW & RESET_  ;
   XMSEL       := (COUNT == 4) & HIGH & RESET_ ;
   XCASI_      := (COUNT == 5) & LOW & RESET_  ;
   XDSACK_     := (COUNT == 7) & LOW & RESET_  ;
   XRASI_      := (COUNT == 9) & HIGH  ;
   XMSEL       := (COUNT == 9) & LOW   ;
   XCASI_      := (COUNT == 9) & HIGH  ;
   XDSACK_     := (COUNT == 11) & HIGH ;

   if (COUNT == 11) # !RESET_ then 0;

test_vectors

"MEMORY ACCESS FOLLOWED BY A HIDDEN REFRESH
([OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT]->[RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,STATE_])
 [ C ,  L  ,   X   ,  X  , X , X , X ,  0  ]->[  H  ,  H  ,  H  ,  L , H , L ,  H  ,  0  ];
```

```
 [ C , L , X , X , X , X , X , 0 ]->[ H , H , H , L , H , L , H , 0 ];
 [ C , H , L , H , L , X , X , 0 ]->[ H , H , H , L , H , L , H , 0 ];
 [ C , H , L , H , H , X , H , 0 ]->[ H , H , H , L , H , L , H , 2 ];
 [ C , H , L , H , X , H , X , 0 ]->[ L , H , H , L , H , L , H , 2 ];
 [ C , H , L , H , X , X , X , 1 ]->[ L , H , H , H , H , L , H , 2 ];
 [ C , H , L , H , X , X , X , 2 ]->[ L , L , H , H , H , L , H , 2 ];
 [ C , H , L , H , X , X , X , 3 ]->[ L , L , H , H , H , L , H , 2 ];
 [ C , H , L , H , X , X , X , 4 ]->[ L , L , H , H , H , L , L , 2 ];
 [ C , H , L , H , X , X , X , 5 ]->[ L , L , H , H , H , L , L , 2 ];
 [ C , H , L , H , X , X , X , 6 ]->[ H , L , H , L , H , L , L , 2 ];
 [ C , H , L , H , X , X , X , 7 ]->[ H , L , H , L , H , L , L , 2 ];
 [ C , H , L , H , X , X , X , 8 ]->[ H , L , H , L , H , L , H , 3 ];
 [ C , H , L , H , X , X , X , 0 ]->[ H , L , L , L , L , L , H , 3 ];
 [ C , H , L , H , X , X , X , 1 ]->[ L , L , L , L , L , H , H , 3 ];
 [ C , H , L , H , X , X , X , 2 ]->[ L , L , L , L , L , H , H , 3 ];
 [ C , H , L , H , X , X , X , 3 ]->[ L , L , L , L , L , L , H , 3 ];
 [ C , H , H , H , X , X , X , 4 ]->[ L , L , L , L , L , L , H , 3 ];
 [ C , H , H , H , X , X , X , 5 ]->[ H , H , H , L , H , L , H , 0 ];

test_vectors

"MANDATORY REFRESH FOLLOWED BY AN ACCESS GRANT CYCLE
([OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT]->[RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_])
 [ C , H , L , L , X , X , X , 0 ]->[ H , H , H , L , H , L , H , H , 1 ];
 [ C , H , L , L , X , X , X , 0 ]->[ H , H , H , L , L , L , H , H , 1 ];
 [ C , H , L , L , X , X , X , 1 ]->[ H , H , L , L , L , L , H , H , 1 ];
 [ C , H , L , L , H , X , H , 2 ]->[ L , H , L , L , L , H , H , L , 1 ];
 [ C , H , L , L , X , X , X , 3 ]->[ L , H , L , L , L , H , H , L , 1 ];
 [ C , H , H , H , X , X , X , 4 ]->[ L , H , L , L , L , L , H , L , 1 ];
 [ C , H , H , H , X , X , X , 5 ]->[ L , H , L , L , L , L , H , L , 1 ];
 [ C , H , H , H , X , X , X , 6 ]->[ H , H , H , L , H , L , H , L , 1 ];
 [ C , H , H , H , X , H , X , 7 ]->[ H , H , H , L , H , L , H , L , 4 ];
 [ C , H , H , H , X , X , X , 0 ]->[ H , H , H , L , H , L , H , L , 4 ];
 [ C , H , H , H , X , X , X , 1 ]->[ H , H , H , L , H , L , H , L , 4 ];
 [ C , H , H , H , X , X , X , 2 ]->[ H , H , H , L , H , L , H , L , 4 ];
 [ C , H , H , H , X , X , X , 3 ]->[ L , H , H , L , H , L , H , L , 4 ];
 [ C , H , H , H , X , X , X , 4 ]->[ L , H , H , H , H , L , H , H , 4 ];
 [ C , H , H , H , X , X , X , 5 ]->[ L , L , H , H , H , L , H , H , 4 ];
 [ C , H , H , H , X , X , X , 6 ]->[ L , L , H , H , H , L , H , H , 4 ];
 [ C , H , H , H , X , X , X , 7 ]->[ L , L , H , H , H , L , L , H , 4 ];
 [ C , H , H , H , X , X , X , 8 ]->[ L , L , H , H , H , L , L , H , 4 ];
 [ C , H , H , H , X , X , X , 9 ]->[ H , H , H , L , H , L , L , H , 4 ];
 [ C , H , H , H , X , X , X , 10 ]->[ H , H , H , L , H , L , L , H , 4 ];
 [ C , H , H , H , X , X , X , 11 ]->[ H , H , H , L , H , L , H , H , 0 ];

test_vectors

"NORMAL ACCESS CYCLE
([OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT]->[RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,STATE_])
 [ C , L , X , X , X , X , X , 0 ]->[ H , H , H , L , H , L , H , 0 ];
 [ C , L , X , X , X , X , X , 0 ]->[ H , H , H , L , H , L , H , 0 ];
 [ C , H , H , H , L , X , X , 0 ]->[ H , H , H , L , H , L , H , 0 ];
 [ C , H , H , H , H , X , H , 0 ]->[ H , H , H , L , H , L , H , 2 ];
 [ C , H , H , H , X , H , X , 0 ]->[ L , H , H , L , H , L , H , 2 ];
 [ C , H , H , H , X , X , X , 1 ]->[ L , H , H , H , H , L , H , 2 ];
 [ C , H , H , H , X , X , X , 2 ]->[ L , L , H , H , H , L , H , 2 ];
```

```
 [ C , H  ,  H  , H , X , X , X ,  3 ]->[ L , L , H  , H , H , L ,  H  ,  2  ];
 [ C , H  ,  H  , H , X , X , X ,  4 ]->[ L , L , H  , H , H , L ,  L  ,  2  ];
 [ C , H  ,  H  , H , X , X , X ,  5 ]->[ L , L , H  , H , H , L ,  L  ,  2  ];
 [ C , H  ,  H  , H , X , X , X ,  6 ]->[ H , H , H  , L , H , L ,  L  ,  2  ];
 [ C , H  ,  H  , H , X , X , X ,  7 ]->[ H , H , H  , L , H , L ,  L  ,  2  ];
 [ C , H  ,  H  , H , X , X , X ,  8 ]->[ H , H , H  , L , H , L ,  H  ,  0  ];
 [ C , H  ,  H  , H , X , X , X ,  0 ]->[ H , H , H  , L , H , L ,  H  ,  0  ];

test_vectors

"MANDATORY REFRESH CYCLE
([OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT]->[RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_])
 [ C , H  ,  L  , L , X , X , X ,  0 ]->[ H , H , H  , L , H , L ,  H  , H , 1  ];
 [ C , H  ,  L  , L , X , X , X ,  0 ]->[ H , H , H  , L , L , L ,  H  , H , 1  ];
 [ C , H  ,  L  , L , X , X , X ,  1 ]->[ H , H , L  , L , L , L ,  H  , H , 1  ];
 [ C , H  ,  L  , L , H , X , H ,  2 ]->[ L , H , L  , L , L , H ,  H  , L , 1  ];
 [ C , H  ,  L  , L , X , X , X ,  3 ]->[ L , H , L  , L , L , H ,  H  , L , 1  ];
 [ C , H  ,  H  , H , X , X , X ,  4 ]->[ L , H , L  , L , L , L ,  H  , L , 1  ];
 [ C , H  ,  H  , H , X , X , X ,  5 ]->[ L , H , L  , L , L , L ,  H  , L , 1  ];
 [ C , H  ,  H  , H , X , X , X ,  6 ]->[ H , H , H  , L , H , L ,  H  , L , 1  ];
 [ C , H  ,  H  , H , X , L , X ,  7 ]->[ H , H , H  , L , H , L ,  H  , H , 0  ];
 [ C , H  ,  H  , H , X , X , X ,  0 ]->[ H , H , H  , L , H , L ,  H  , H , 0  ];

end
```

```
module _CASDCODE
title 'CAS DECODER FOR DRAM TIMING CONTROLLER WITH HIDDEN REFRESH
       BERTRAND LEIGH, TEXAS INSTRUMENTS, DECEMBER 17, 1987'

        CASDCODE device 'P16L8';

"*********************************************************************
" This CAS decoder decodes CAS0-CAS3 from DRAM controller (ALS6301)
" and RCAS (refresh CAS) from DRAM timing controller for CAS before
" RAS option refresh and hidden refresh. ICAS0-ICAS3 are simply
" passed on to OCAS0-OCAS3 during access.  During refresh, RCAS
" overrides all ICAS.
"*********************************************************************

"Input pin assignments
  ICAS0_    PIN 1;
  ICAS1_    PIN 2;
  ICAS2_    PIN 3;
  ICAS3_    PIN 4;
  RCAS_     PIN 5;          "REFRESH CAS (FOR CAS BEFOR RAS REFRESH)

"Output pin assignments
  OCAS0_    PIN 19;
  OCAS1_    PIN 18;
  OCAS2_    PIN 17;
  OCAS3_    PIN 16;


"Intermediate declaration
  H,L,C,X  = 1,0,.C.,.X.;

truth_table

([ICAS0_,ICAS1_,ICAS2_,ICAS3_,RCAS_]->[OCAS0_,OCAS1_,OCAS2_,OCAS3_])
 [  L  ,  H  ,  H  ,  H  ,  H  ]->[  L  ,  H  ,  H  ,  H  ] ;
 [  H  ,  L  ,  H  ,  H  ,  H  ]->[  H  ,  L  ,  H  ,  H  ] ;
 [  H  ,  H  ,  L  ,  H  ,  H  ]->[  H  ,  H  ,  L  ,  H  ] ;
 [  H  ,  H  ,  H  ,  L  ,  H  ]->[  H  ,  H  ,  H  ,  L  ] ;
 [  X  ,  X  ,  X  ,  X  ,  L  ]->[  L  ,  L  ,  L  ,  L  ] ;

test_vectors

([ICAS0_,ICAS1_,ICAS2_,ICAS3_,RCAS_]->[OCAS0_,OCAS1_,OCAS2_,OCAS3_])
 [  L  ,  H  ,  H  ,  H  ,  H  ]->[  L  ,  H  ,  H  ,  H  ] ;
 [  H  ,  L  ,  H  ,  H  ,  H  ]->[  H  ,  L  ,  H  ,  H  ] ;
 [  H  ,  H  ,  L  ,  H  ,  H  ]->[  H  ,  H  ,  L  ,  H  ] ;
 [  H  ,  H  ,  H  ,  L  ,  H  ]->[  H  ,  H  ,  H  ,  L  ] ;
 [  X  ,  X  ,  X  ,  X  ,  L  ]->[  L  ,  L  ,  L  ,  L  ] ;

END
```

```
Partno          HRFT;
Name            HRFT;
Date            01/08/88;
Revision        00;
Designer        B. Leigh;
Company         Texas Instruments;
Assembly        None;
Location        Dallas, TX;
/*************************************************************/
/*       DRAM TIMING CONTROLLER WITH HIDDEN REFRESH          */
/*************************************************************/
/* Allowable Target Device Types: PSG507                     */
/*************************************************************/

/* Input pin assignments   */
  PIN 1    =OSC  ;          /* timing controller's input clock          */
  PIN 2    =RESET_;         /* system reset (active low)                */
  PIN 3    =REFREQ_;        /* refresh request                          */
  PIN 4    =MREF_;          /* mandatory refresh request                */
  PIN 5    =AS_  ;          /* address strobe                           */
  PIN 6    =A23 ;           /* memory/IO access indicator (memory access */
                            /* when high)                               */
  PIN 7    =CLK  ;          /* system clock for synchronization (OSC/2)  */

/*  Output pin assignments  */
  PIN 8    =RASI_    ;
  PIN 9    =CASI_    ;
  PIN 10   =MSEL     ;
  PIN 11   =MC1      ;
  PIN 13   =RFC      ;
  PIN 14   =DSACK_   ;
  PIN 15   =RFCAS_   ;

/*  Internal counter bits and control node declarations  */
  PINNODE [33..38]  = [C0..5]  ;
  PINNODE 39        = SCLR0    ;
  PINNODE 41        = CNT_HLD0 ;
  PINNODE 42        = CNT_HLD1 ;

/*  Buried state registers node declarations          */
  NODE   [P0..2];          /*   state register         */
  NODE   REQ_   ;          /*   access request status  */


/*  Intermediate declaration        */
  field  STATE    = [P2..0];
  field  COUNT    = [C5..0];
$define  ST0       'b'000
$define  ST1       'b'001
$define  ST2       'b'010
$define  ST3       'b'011
$define  ST4       'b'100

/* BUILT-IN COUNTER CONTROL EQUATIONS */
```

```
  SCLR0 =   !RESET_
          # ST1 & (COUNT:'d'7)
          # ST2 & (COUNT:'d'8)
          # ST2 & (COUNT:'d'0) & !A23
          # ST3 & (COUNT:'d'5)
          # ST4 & (COUNT:'d'11)    ;

  CNT_HLD1.S =   !RESET_
               # ST1 & (COUNT:'d'7) & !(A23 & !REQ_)
               # ST2 & (COUNT:'d'8) & REFREQ_
               # ST2 & (COUNT:'d'0) & !A23
               # ST3 & (COUNT:'d'5) & !(A23 & !REQ_)
               # ST4 & (COUNT:'d'11)       ;

  CNT_HLD1.R =   ST0 & !MREF_ & RESET_
               # ST0 & AS_ & CLK & RESET_
               # ST1 & (COUNT:'d'7) & (A23 & !REQ_) & RESET_
               # ST2 & (COUNT:'d'8) & !REFREQ_ & RESET_
               # ST3 & (COUNT:'d'5) & (A23 & !REQ_) & RESET_    ;

/* STATE MACHINE EQUATIONS  */

sequence STATE {
present ST0:                          /*    RESET OR HOLDING STATE   */
   if !MREF_ & RESET_                 next ST1  ;
   if AS_ & CLK & RESET_              next ST2  ;
   default                            next ST0
                  out [!RFC,MC1,DSACK_,REQ_,RASI_,CASI_,RFCAS_,!MSEL]  ;

present ST1:                          /*    MANDATORY REFRESH CYCLE  */
   if AS_ & CLK & RESET_                    next ST1 out [!REQ_];
   if (COUNT:'d'0) & RESET_                 next ST1 out [!MC1];
   if (COUNT:'d'1) & RESET_                 next ST1 out [!RFCAS_];
   if (COUNT:'d'2) & RESET_                 next ST1 out [!RASI_,RFC];
   if (COUNT:'d'4)                          next ST1 out [!RFC];
   if (COUNT:'d'6)                          next ST1 out [RASI_,MC1,RFCAS_];
   if (COUNT:'d'7) & !A23                   next ST1 out [REQ_];
   if !RESET_ # !(!REQ_ & A23) & (COUNT:'d'7)  next ST0  ;
   if !REQ_ & A23 & (COUNT:'d'7) & RESET_   next ST4  ;
   default                                  next ST1  ;


present ST2:                          /*      NORMAL ACCESS CYCLE  */
   if !RESET_ # (COUNT:'d'0) & !A23         next ST0 ;
   if (COUNT:'d'0) & RESET_                 next ST2 out [!RASI_] ;
   if (COUNT:'d'1) & RESET_                 next ST2 out [MSEL] ;
   if (COUNT:'d'2) & RESET_                 next ST2 out [!CASI_] ;
   if (COUNT:'d'4) & RESET_                 next ST2 out [!DSACK_] ;
   if (COUNT:'d'6)                          next ST2 out [RASI_,!MSEL];
   if (COUNT:'d'6) & REFREQ_                next ST2 out [CASI_];
   if (COUNT:'d'8)                          next ST2 out [DSACK_];
   if REFREQ_ & (COUNT:'d'8) & RESET_       next ST0 ;
   if !REFREQ_ & (COUNT:'d'8) & RESET_      next ST3 ;
   default                                  next ST2 ;

present ST3:                          /*      HIDDEN REFRESH CYCLE  */
```

```
   if AS_ & CLK & RESET_                        next ST3 out [!REQ_];
   if (COUNT:'d'0) & RESET_                     next ST3 out [!MC1];
   if (COUNT:'d'0) & RESET_                     next ST3 out [!RFCAS_];
   if (COUNT:'d'1) & RESET_                     next ST3 out [RFC,!RASI_];
   if (COUNT:'d'3)                              next ST3 out [!RFC];
   if (COUNT:'d'5)                              next ST3 out [RASI_,MC1,CASI_,RFCAS_];
   if !RESET_ # !(!REQ_ & A23) & (COUNT:'d'5)   next ST0 ;
   if !REQ_ & A23 & (COUNT:'d'5) & RESET_       next ST4 ;
   default                                      next ST3;

present ST4:                        /*      ACCESS GRANT CYCLE      */
   if (COUNT:'d'3) & RESET_                     next ST4 out [!RASI_];
   if (COUNT:'d'4)                              next ST4 out [REQ_] ;
   if (COUNT:'d'4) & RESET_                     next ST4 out [MSEL];
   if (COUNT:'d'5) & RESET_                     next ST4 out [!CASI_];
   if (COUNT:'d'7) & RESET_                     next ST4 out [!DSACK_];
   if (COUNT:'d'9)                              next ST4 out [RASI_,!MSEL,CASI_];
   if (COUNT:'d'11)                             next ST4 out [DSACK_];
   if (COUNT:'d'11) # !RESET_                   next ST0 ;
   default                                      next ST4; }


APPEND RASI_.S = !RESET_;   APPEND CASI_.S = !RESET_;   APPEND RFCAS_.S = !RESET_;
APPEND MC1.S   = !RESET_;   APPEND DSACK_.S= !RESET_;   APPEND REQ_.S   = !RESET_;
APPEND SCLR0   = !RESET_;   APPEND MSEL.R  = !RESET_;   APPEND RFC.R    = !RESET_;
APPEND P0.R    = !RESET_;   APPEND P1.R    = !RESET_;   APPEND P2.R     = !RESET_;
```

```
Partno          HRFT;
Name            HRFT;
Date            01/08/88;
Revision        00;
Designer        B. Leigh;
Company         Texas Instruments;
Assembly        None;
Location        Dallas, TX;
/*************************************************************/
/*              SIMULATION FILE FOR                          */
/*       DRAM TIMING CONTROLLER WITH HIDDEN REFRESH          */
/*************************************************************/
/* Allowable Target Device Types: PSG507                     */
/*************************************************************/

ORDER: OSC,%4,RESET_,%7,REFREQ_,%6,MREF_,%4,AS_,%3,A23,%3,CLK,%4,COUNT,%3,
       RASI_,%5,CASI_,%5,RFCAS_,%6,MSEL,%3,MC1,%3,RFC,%4,DSACK_,%5,REQ_,%5,STATE ;

BASE: DECIMAL;

VECTORS:

$msg"   MEMORY ACCESS FOLLOWED BY A HIDDEN REFRESH  " ;
$msg"-----------------input-----------------    -----------------output-----------------------  ";
$msg"  OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT    RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_  ";
$msg"-----------------------------------------    ---------------------------------------------- ";
       C   0      1     1    X   X   X   '0'      H    H    H    L    H    L    H    H    "0"
       C   0      1     1    X   X   X   '0'      H    H    H    L    H    L    H    H    "0"
       C   1      0     1    0   X   X   '0'      H    H    H    L    H    L    H    H    "0"
       C   1      0     1    1   X   1   '0'      H    H    H    L    H    L    H    H    "2"
       C   1      0     1    X   1   X   '0'      L    H    H    L    H    L    H    H    "2"
       C   1      0     1    X   X   X   '1'      L    H    H    H    H    L    H    H    "2"
       C   1      0     1    X   X   X   '2'      L    L    H    H    H    L    H    H    "2"
       C   1      0     1    X   X   X   '3'      L    L    H    H    H    L    H    H    "2"
       C   1      0     1    X   X   X   '4'      L    L    H    H    H    L    L    H    "2"
       C   1      0     1    X   X   X   '5'      L    L    H    H    H    L    L    H    "2"
       C   1      0     1    X   X   X   '6'      H    L    H    L    H    L    L    H    "2"
       C   1      0     1    X   X   X   '7'      H    L    H    L    H    L    L    H    "2"
       C   1      0     1    X   X   X   '8'      H    L    H    L    H    L    H    H    "3"
       C   1      0     1    0   0   X   '0'      H    L    L    L    L    L    H    H    "3"
       C   1      0     1    0   0   X   '1'      L    L    L    L    L    H    H    H    "3"
       C   1      0     1    0   0   X   '2'      L    L    L    L    L    H    H    H    "3"
       C   1      0     1    0   0   X   '3'      L    L    L    L    L    L    H    H    "3"
       C   1      1     1    0   0   X   '4'      L    L    L    L    L    L    H    H    "3"
       C   1      1     1    0   0   X   '5'      H    H    H    L    H    L    H    H    "0"


$msg" MANDATORY REFRESH FOLLOWED BY AN ACCESS GRANT CYCLE ";
$msg"-----------------input-----------------    -----------------output-----------------------  ";
$msg"  OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT    RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_  ";
$msg"-----------------------------------------    ---------------------------------------------- ";
       C   1      0     0    0   0   X   '0'      H    H    H    L    H    L    H    H    "1"
       C   1      0     0    0   0   X   '0'      H    H    H    L    L    L    H    H    "1"
       C   1      0     0    0   0   X   '1'      H    H    L    L    L    L    H    H    "1"
       C   1      0     0    1   0   1   '2'      L    H    L    L    L    H    H    L    "1"
       C   1      0     0    0   0   X   '3'      L    H    L    L    L    H    H    L    "1"
```

```
        C   1       1       1       0   0   X   '4'     L   H   L       L   L   L   H   L   "1"
        C   1       1       1       0   0   X   '5'     L   H   L       L   L   L   H   L   "1"
        C   1       1       1       0   0   X   '6'     H   H   H       L   H   L   H   L   "1"
        C   1       1       1       0   1   X   '7'     H   H   H       L   H   L   H   L   "4"
        C   1       1       1       0   0   X   '0'     H   H   H       L   H   L   H   L   "4"
        C   1       1       1       0   0   X   '1'     H   H   H       L   H   L   H   L   "4"
        C   1       1       1       0   0   X   '2'     H   H   H       L   H   L   H   L   "4"
        C   1       1       1       0   0   X   '3'     L   H   H       L   H   L   H   L   "4"
        C   1       1       1       0   0   X   '4'     L   H   H       H   H   L   H   H   "4"
        C   1       1       1       0   0   X   '5'     L   L   H       H   H   L   H   H   "4"
        C   1       1       1       0   0   X   '6'     L   L   H       H   H   L   H   H   "4"
        C   1       1       1       0   0   X   '7'     L   L   H       H   H   L   L   H   "4"
        C   1       1       1       0   0   X   '8'     L   L   H       H   H   L   L   H   "4"
        C   1       1       1       0   0   X   '9'     H   H   H       L   H   L   L   H   "4"
        C   1       1       1       0   0   X   '10'    H   H   H       L   H   L   L   H   "4"
        C   1       1       1       0   0   X   '11'    H   H   H       L   H   L   H   H   "0"

$msg"NORMAL ACCESS CYCLE  ";
$msg"------------------input-------------------   -------------------output----------------------  ";
$msg"  OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT   RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_  ";
$msg"-------------------------------------------   ------------------------------------------------- ";
        C   0       X       X       0   0   X   '0'     H   H   H       L   H   L   H   H   "0"
        C   0       X       X       0   0   X   '0'     H   H   H       L   H   L   H   H   "0"
        C   1       1       1       0   0   X   '0'     H   H   H       L   H   L   H   H   "0"
        C   1       1       1       1   0   1   '0'     H   H   H       L   H   L   H   H   "2"
        C   1       1       1       0   1   X   '0'     L   H   H       L   H   L   H   H   "2"
        C   1       1       1       0   0   X   '1'     L   H   H       H   H   L   H   H   "2"
        C   1       1       1       0   0   X   '2'     L   L   H       H   H   L   H   H   "2"
        C   1       1       1       0   0   X   '3'     L   L   H       H   H   L   H   H   "2"
        C   1       1       1       0   0   X   '4'     L   L   H       H   H   L   L   H   "2"
        C   1       1       1       0   0   X   '5'     L   L   H       H   H   L   L   H   "2"
        C   1       1       1       0   0   X   '6'     H   H   H       L   H   L   L   H   "2"
        C   1       1       1       0   0   X   '7'     H   H   H       L   H   L   L   H   "2"
        C   1       1       1       0   0   X   '8'     H   H   H       L   H   L   H   H   "0"
        C   1       1       1       0   0   X   '0'     H   H   H       L   H   L   H   H   "0"

$msg"MANDATORY REFRESH CYCLE  ";
$msg"------------------input-------------------   -------------------output----------------------  ";
$msg"  OSC,RESET_,REFREQ_,MREF_,AS_,A23,CLK,COUNT   RASI_,CASI_,RFCAS_,MSEL,MC1,RFC,DSACK_,REQ_,STATE_  ";
$msg"-------------------------------------------   ------------------------------------------------- ";
        C   1       0       0       0   0   X   '0'     H   H   H       L   H   L   H   H   "1"
        C   1       0       0       0   0   X   '0'     H   H   H       L   L   L   H   H   "1"
        C   1       0       0       0   0   X   '1'     H   H   L       L   L   L   H   H   "1"
        C   1       0       0       1   0   1   '2'     L   H   L       L   L   H   H   L   "1"
        C   1       0       0       0   0   X   '3'     L   H   L       L   L   H   H   L   "1"
        C   1       1       1       0   0   X   '4'     L   H   L       L   L   L   H   L   "1"
        C   1       1       1       0   0   X   '5'     L   H   L       L   L   L   H   L   "1"
        C   1       1       1       0   0   X   '6'     H   H   H       L   H   L   H   L   "1"
        C   1       1       1       0   0   X   '7'     H   H   H       L   H   L   H   H   "0"
        C   1       1       1       0   0   X   '0'     H   H   H       L   H   L   H   H   "0"
```

```
Partno          CASDCODE;
Name            CASDCODE;
Date            05/04/88;
Revision        00;
Designer        B. Leigh;
Company         Texas Instruments;
Assembly        None;
Location        Dallas, TX;
/*************************************************************/
/*        CAS DECODER DRAM TIMING CONTROLLER                 */
/*************************************************************/
/* Allowable Target Device Types: TIBPAL16L8-10              */
/*************************************************************/

/*************************************************************************
  This CAS decoder decodes CAS0-CAS3 from DRAM controller (ALS6301)
  and RCAS (refresh CAS) from DRAM timing controller for CAS before
  RAS option refresh and hidden refresh. ICAS0-ICAS3 are simply
  passed on to OCAS0-OCAS3 during access.  During refresh, RCAS
  overrides all ICAS.
 *************************************************************************/

/* Input pin assignments  */
  PIN 1 = ICAS0_ ;
  PIN 2 = ICAS1_ ;
  PIN 3 = ICAS2_ ;
  PIN 4 = ICAS3_ ;
  PIN 5 = RCAS_  ;         /* REFRESH CAS (FOR CAS-BEFORE-RAS REFRESH) */

/* Output pin assignments  */
  PIN 19 = OCAS0_  ;
  PIN 18 = OCAS1_  ;
  PIN 17 = OCAS2_  ;
  PIN 16 = OCAS3_  ;


table
 [ICAS0_,ICAS1_,ICAS2_,ICAS3_,RCAS_]=>[OCAS0_,OCAS1_,OCAS2_,OCAS3_]{
 'b'01111=>'b'0111 ;
 'b'10111=>'b'1011 ;
 'b'11011=>'b'1101 ;
 'b'11101=>'b'1110 ;
 'b'XXXX0=>'b'0000 ;
```

```
Partno          CASDCODE;
Name            CASDCODE;
Date            05/04/88;
Revision        00;
Designer        B. Leigh;
Company         Texas Instruments;
Assembly        None;
Location        Dallas, TX;
/*************************************************************/
/*                SIMULATION FILE FOR                        */
/*        CAS DECODER DRAM TIMING CONTROLLER                 */
/*************************************************************/
/* Allowable Target Device Types: TIBPAL16L8-10              */
/*************************************************************/

ORDER: ICAS0_,%2,ICAS1_,%2,ICAS2_,%2,ICAS3_,%2,RCAS_,%8,
       OCAS0_,%2,OCAS1_,%2,OCAS2_,%2,OCAS3_ ;


VECTORS:

$msg"     ----input----         ---output--  ";
$msg"     I  I  I  I            O  O  O  O   ";
$msg"     C  C  C  C  R         C  C  C  C   ";
$msg"     A  A  A  A  C         A  A  A  A   ";
$msg"     S  S  S  S  A         S  S  S  S   ";
$msg"     0  1  2  3  S         0  1  2  3   ";
$msg"     -------------------------------- ";
          0  1  1  1  1         L  H  H  H
          1  0  1  1  1         H  L  H  H
          1  1  0  1  1         H  H  L  H
          1  1  1  0  1         H  H  H  L
          X  X  X  X  0         L  L  L  L
```

Contents

General Information for Use of an Error Detection and Correction (EDAC) Device

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Contents

List of Illustrations

List of Tables

Introduction

The DRAM technology of today (i.e., 256K, 1M) has enabled system designers to use much larger memory sizes than ever before. However, as with most advances in technology, this has brought a new problem. For system memory sizes larger than 1/2 million bits, it is generally considered that error detection and correction is required to guarantee system reliability without a tradeoff in performance. Although present methods of parity checking will identify errors, they are not able to correct them. And not correcting these errors can be costly. For example, in personal computers when parity errors are encountered, the system has to be reset to eliminate the problem. This system reset destroys any data stored in RAM and it must be reentered. This is obviously unacceptable to your customers. To eliminate this problem, TI has produced cost-effective Error Detection and Correction (EDAC) devices.

Error Types and Sources in Dynamic Memories

Two kinds of errors occur in memory devices; soft and/or hard errors. A hard error is a physical failure of the memory device (e.g., an internal short or an open lead). This type of error causes the memory location to always be either a high or a low. A soft error is a random occurrence of a memory location change from a high level to low level. These errors may be caused by system noise, alpha particle radiation, or power surges.

In spite of design techniques used by memory chip manufactures to reduce these errors, they are still a source of major concern in your system. Table 1 indicates that as the density of memory chips increase their probability of errors also increase. Therefore, your data integrity decreases in larger memory arrays.

Table 1. Chip Densities vs Soft-Error Rates

CHIP DENSITY BITS/CHIP	TYPICAL SOFT-ERROR RATE (% PER 1000 HOURS)
64K	0.10 – 0.20
256K	0.15 – 0.30
1M	0.20 – 0.35

Solutions to Boost System Reliability

There are several alternatives available that will either decrease or eliminate these errors in your system. One method used to determine data integrity is the incorporation of parity checking. This can be accomplished by using an SN74ALS29833 Parity Bus Transceiver. To identify an error, the data word and the generated parity are compared by performing an exclusive-OR operation. If several bits in the data word are in error or the parity has changed, the exclusive-OR output would be low. While data integrity can be determined using this method, it is unable to correct errors.

To obtain the desired level of quality, some type of error-correction scheme must be incorporated. An EDAC chip provides the simple solution to the problem, while dramatically extending the system Mean Time Between Failures (MTBF). This is accomplished by detecting and correcting single bit errors and detecting double bit errors. See Table 2.

Table 2. System MTBF Increases with an EDAC

	MTBF†	
	Without EDAC	**With EDAC**
Correctable Soft Error (single bit)	7 Months	>200 Years

†Based on 16M-bit memory system using 256K DRAMs with a 0.30% per 1000 hour soft error rate.

When you include the other system variables causing errors (power surges, noisy systems, etc.), your memory system MTBF, without an EDAC could be reduced to several days. These types of memory-cell errors can be corrected using an EDAC.

EDAC Operation

When data is written to memory, the TI SN74AS632 (32-Bit EDAC) generates parity check bits. Each check bit is generated by performing a specific parity check on the 32-bit data word. For example, CB0 is obtained by comparing specific bits of the 32-bit word with those corresponding to an "X" in the Hamming Code Parity Algorithm (see Table 3). CB0 will be at a high level if the total number of highs corresponding to these locations is an odd number. CB0 will be at a low level if this number is even. This procedure is repeated 7 times to obtain the 7 check bits, CB0-CB6 of the Hamming Code. Check bits CB0-CB2 are used to determine odd parity. Check bits CB3-CB6 are used for even parity.

Table 3. Hamming Code Parity Algorithm

CHECK WORD BIT	32-BIT DATA WORD																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CB0	X		X	X		X					X		X	X	X			X			X		X	X	X	X		X				X
CB1				X		X		X		X		X		X	X	X				X		X		X		X		X		X	X	X
CB2	X		X			X	X		X			X	X			X	X		X			X	X		X			X	X			X
CB3			X	X	X				X	X	X				X	X			X	X	X				X	X	X				X	X
CB4	X	X							X	X	X	X	X	X			X	X							X	X	X	X	X	X		
CB5	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X								
CB6	X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X

The seven check bits are parity bits derived from the matrix of data bits as indicated by "X" for each bit.

These check bits are stored along with the data in your systems main memory. This additional memory requirement is the only overhead involved with the use of an EDAC. Figure 1 shows a typical system using an EDAC and illustrates this overhead.

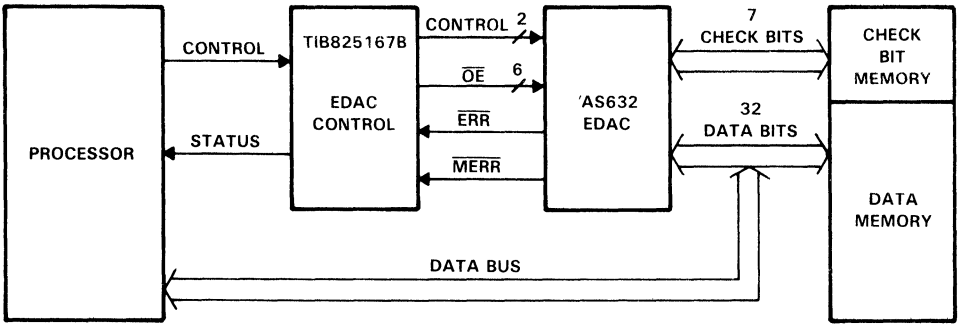

Figure 1. Typical 'AS632 System

During a read cycle, the data and check bits are read from memory, any of which may be invalid. New check bits are computed from the stored data bits. To determine the validity of the data, the new and old check bits are exclusive-ORed producing a 7-bit syndrome code. When decoded, these syndrome bits describe the condition of the data word: free of errors, having a single-bit error, or having multiple errors. See Table 4. Any single error in the 32-bit word can be corrected. Both single- and double-bit errors are indicated to the processor via single- and double-bit error flags.

There are two additional options for implementing EDAC into your system; detect only and correct always. Of these two, correct always is the easiest to implement. The EDAC always corrects single-bit errors and writes this corrected word onto the system data bus or into memory.

Because days can elapse between errors, correction can be done only when needed. The detect-only option increases your system performance during a read cycle by allowing data to be written directly to the system processor. If a single- or double-bit error occurs, the EDAC will flag the processor. This enables the processor to enter a wait cycle until the word is corrected. This method of implementation does not use the error correction portion of the EDAC until the processor determines what action to take in the event of an error.

Another method of ensuring data integrity in your system is to use an EDAC unit during memory refresh. The EDAC will "clean" every memory location of errors during the mandatory refresh cycles. This process is known as memory scrubbing. The data can then be checked again during a memory-access cycle. By checking the data twice, the time between corrections is reduced. Therefore, the probability of multibit errors in your system declines.

Table 4. 'AS632 Syndrome Decoding

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	L	L	L	L	L	L	unc
L	L	L	L	L	L	H	2-bit
L	L	L	L	L	H	L	2-bit
L	L	L	L	L	H	H	unc
L	L	L	L	H	L	L	2-bit
L	L	L	L	H	L	H	unc
L	L	L	L	H	H	L	unc
L	L	L	L	H	H	H	2-bit
L	L	L	H	L	L	L	2-bit
L	L	L	H	L	L	H	unc
L	L	L	H	L	H	L	DB31
L	L	L	H	L	H	H	2-bit
L	L	L	H	H	L	L	unc
L	L	L	H	H	L	H	2-bit
L	L	L	H	H	H	L	2-bit
L	L	L	H	H	H	H	DB30
L	L	H	L	L	L	L	2-bit
L	L	H	L	L	L	H	unc
L	L	H	L	L	H	L	DB29
L	L	H	L	L	H	H	2-bit
L	L	H	L	H	L	L	DB28
L	L	H	L	H	L	H	2-bit
L	L	H	L	H	H	L	2-bit
L	L	H	L	H	H	H	DB27
L	L	H	H	L	L	L	DB26
L	L	H	H	L	L	H	2-bit
L	L	H	H	L	H	L	2-bit
L	L	H	H	L	H	H	DB25
L	L	H	H	H	L	L	2-bit
L	L	H	H	H	L	H	DB24
L	L	H	H	H	H	L	unc
L	L	H	H	H	H	H	2-bit

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
L	H	L	L	L	L	L	2-bit
L	H	L	L	L	L	H	unc
L	H	L	L	L	H	L	DB7
L	H	L	L	L	H	H	2-bit
L	H	L	L	H	L	L	DB6
L	H	L	L	H	L	H	2-bit
L	H	L	L	H	H	L	2-bit
L	H	L	L	H	H	H	DB5
L	H	L	H	L	L	L	DB4
L	H	L	H	L	L	H	2-bit
L	H	L	H	L	H	L	2-bit
L	H	L	H	L	H	H	DB3
L	H	L	H	H	L	L	2-bit
L	H	L	H	H	L	H	DB2
L	H	L	H	H	H	L	unc
L	H	L	H	H	H	H	2-bit
L	H	H	L	L	L	L	DB0
L	H	H	L	L	L	H	2-bit
L	H	H	L	L	H	L	2-bit
L	H	H	L	L	H	H	unc
L	H	H	L	H	L	L	2-bit
L	H	H	L	H	L	H	DB1
L	H	H	L	H	H	L	unc
L	H	H	L	H	H	H	bit
L	H	H	H	L	L	L	2-bit
L	H	H	H	L	L	H	unc
L	H	H	H	L	H	L	unc
L	H	H	H	L	H	H	2-bit
L	H	H	H	H	L	L	unc
L	H	H	H	H	L	H	2-bit
L	H	H	H	H	H	L	2-bit
L	H	H	H	H	H	H	CB6

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

Table 4. 'AS632 Syndrome Decoding (continued)

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	L	L	L	L	L	L	2-bit
H	L	L	L	L	L	H	unc
H	L	L	L	L	H	L	unc
H	L	L	L	L	H	H	2-bit
H	L	L	L	H	L	L	unc
H	L	L	L	H	L	H	2-bit
H	L	L	L	H	H	L	2-bit
H	L	L	L	H	H	H	unc
H	L	L	H	L	L	L	unc
H	L	L	H	L	L	H	2-bit
H	L	L	H	L	H	L	2-bit
H	L	L	H	L	H	H	DB3
H	L	L	H	H	L	L	2-bit
H	L	L	H	H	L	H	unc
H	L	L	H	H	H	L	DB14
H	L	L	H	H	H	H	2-bit
H	L	H	L	L	L	L	unc
H	L	H	L	L	L	H	2-bit
H	L	H	L	L	H	L	2-bit
H	L	H	L	L	H	H	DB13
H	L	H	L	H	L	L	2-bit
H	L	H	L	H	L	H	DB12
H	L	H	L	H	H	L	DB11
H	L	H	L	H	H	H	2-bit
H	L	H	H	L	L	L	2-bit
H	L	H	H	L	L	H	DB10
H	L	H	H	L	H	L	DB9
H	L	H	H	L	H	H	2-bit
H	L	H	H	H	L	L	DB8
H	L	H	H	H	L	H	2-bit
H	L	H	H	H	H	L	2-bit
H	L	H	H	H	H	H	CB5

SYNDROME BITS							ERROR
6	5	4	3	2	1	0	
H	H	L	L	L	L	L	unc
H	H	L	L	L	L	H	2-bit
H	H	L	L	L	H	L	2-bit
H	H	L	L	L	H	H	DB23
H	H	L	L	H	L	L	2-bit
H	H	L	L	H	L	H	DB22
H	H	L	L	H	H	L	DB21
H	H	L	L	H	H	H	2-bit
H	H	L	H	L	L	L	2-bit
H	H	L	H	L	L	H	DB20
H	H	L	H	L	H	L	DB19
H	H	L	H	L	H	H	2-bit
H	H	L	H	H	L	L	DB18
H	H	L	H	H	L	H	2-bit
H	H	L	H	H	H	L	2-bit
H	H	L	H	H	H	H	CB4
H	H	H	L	L	L	L	2-bit
H	H	H	L	L	L	H	DB16
H	H	H	L	L	H	L	unc
H	H	H	L	L	H	H	2-bit
H	H	H	L	H	L	L	DB17
H	H	H	L	H	L	H	2-bit
H	H	H	L	H	H	L	2-bit
H	H	H	L	H	H	H	CB3
H	H	H	H	L	L	L	unc
H	H	H	H	L	L	H	2-bit
H	H	H	H	L	H	L	2-bit
H	H	H	H	L	H	H	CB2
H	H	H	H	H	L	L	2-bit
H	H	H	H	H	L	H	CB1
H	H	H	H	H	H	L	CB0
H	H	H	H	H	H	H	none

CB X = error in check bit X
DB Y = error in data bit Y
2-bit = double-bit error
unc = uncorrectable multibit error

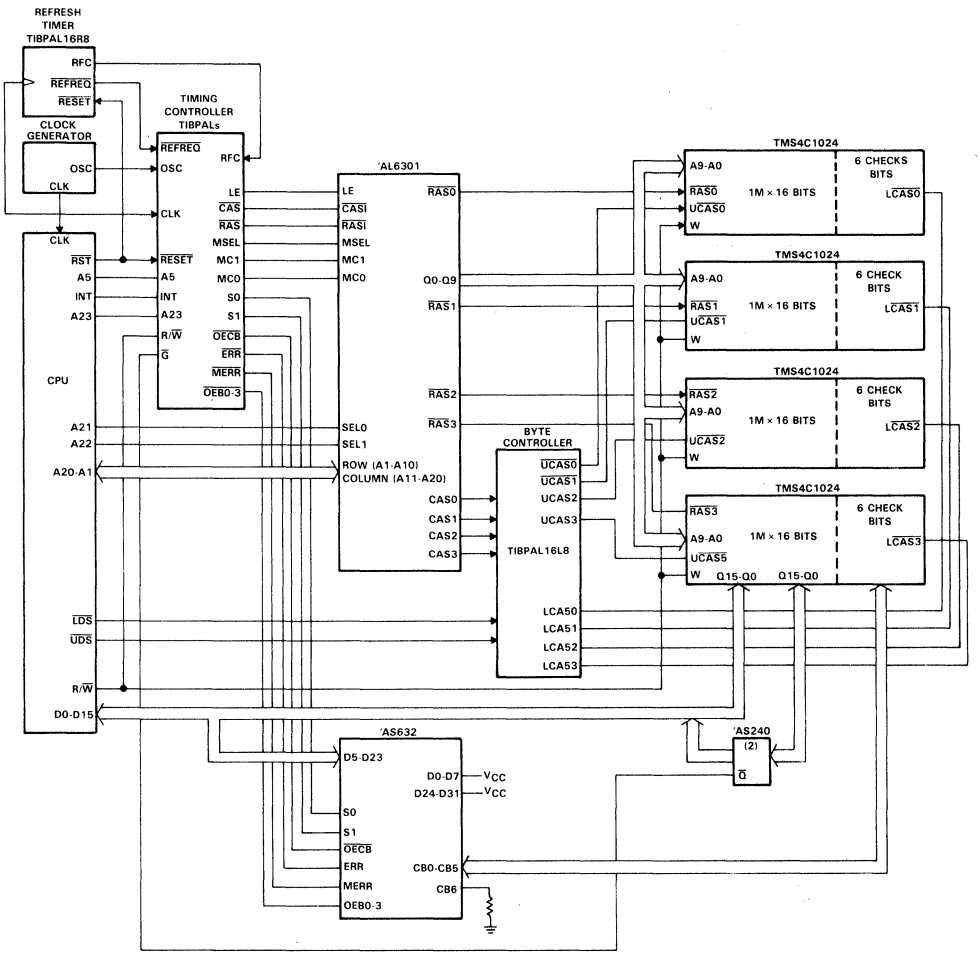

Figure 2. Memory Management Systems Using Scrubbing

The circuit illustrated in Figure 2 is an example of a memory system that used scrubbing. This circuit consists of the TI SN74ALS6302, a 1M-DRAM Controller, the TMS4C1024, 1M DRAMs, the SN74AS632, a 32-bit EDAC, and control circuits.

Texas Instruments EDAC Family

Because of the increase in MTBF, the SN74AS632 can increase system reliability typically by well over 500-fold. The 'AS632 provides built-in diagnostics to assure reliable device operation. Byte-write capability is included to allow operation on 8-bit, 16-bit, or

32-bit word widths in 3-state bus applications. The 'AS632 provides fast correction time, 32 ns, and error-detection time, 25 ns. The architecture of the 'AS632 is illustrated in Figure 3.

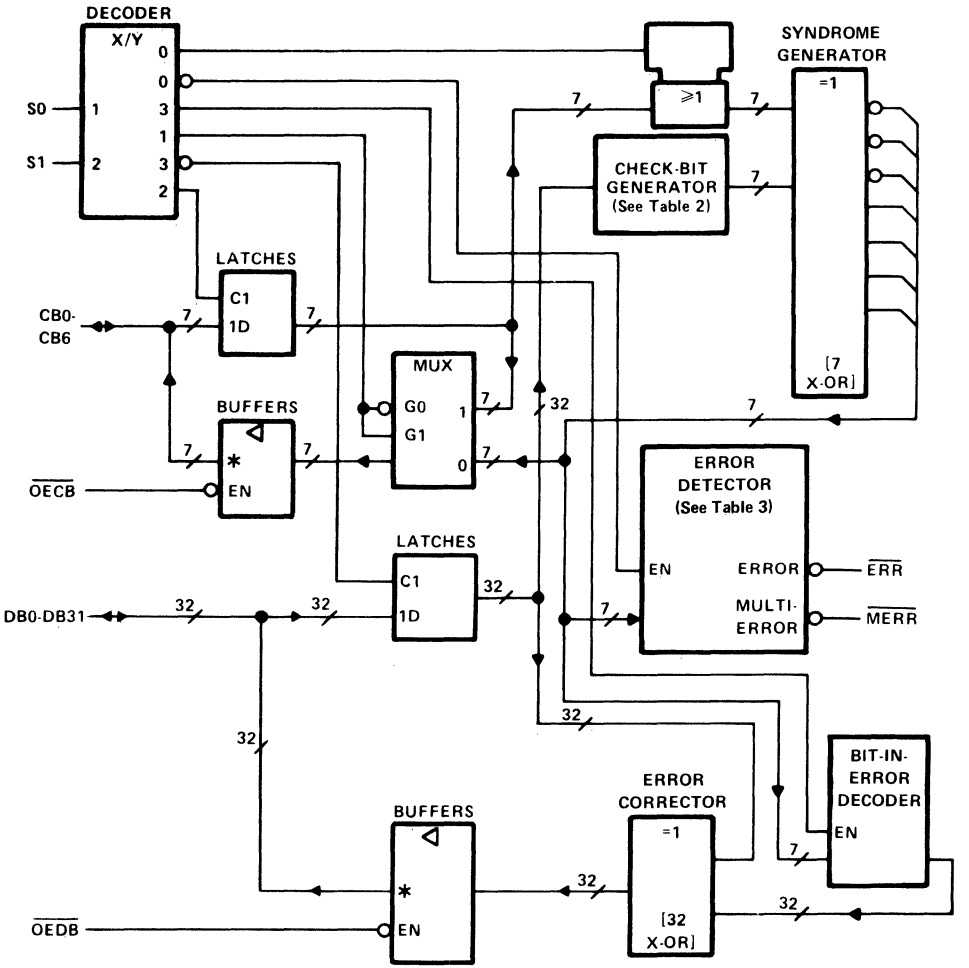

Figure 3. 'AS632 Logic Diagram

Summary

Memory errors are becoming a very important concern to the system designer. To effectively ensure data integrity, a method of correcting data errors is necessary. An EDAC unit provides you with this essential function along with increasing system MTBF from days to years. The TI EDAC family offers you ease of implementation, high performance, and a device that is compatible with any microprocessor you might be using.

For more information on the TI family of EDAC devices, please contact your local TI Sales Representative or the Customer Response Center at 1-800-232-3200.

Error Detection and Correction Using SN74ALS632B and SN74AS632

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Contents

List of Illustrations

Introduction

Need for Error Correction

With memory systems continuing to expand, it has become increasingly important that system designers consider error detection and correction. Generally, the larger the chip density, the greater the probability for device errors. It is easy to recognize this probability when one considers that a 32-bit × 64K memory, using 64K DRAMs, equates to approximately 2.1 million bits of information. This expands to 8.4 million bits of information when using 256K DRAMs. For memory sizes larger than 1/2 million bits, it is generally considered that error detection and correction is required to guarantee high reliability.

The SN74ALS632B and SN74AS632 provide a simple solution to these requirements in 32-bit machines. In addition, the 'ALS632B and 'AS632 provide the necessary hardware to perform byte-write operations which are typically used in the more advanced systems. To ensure the integrity of the error detection and correction circuit itself, diagnostic capabilities have been provided in both devices.

The 'ALS632B and 'AS632 devices are not limited to only 32-bit systems. They can easily be implemented in 16- or 24-bit systems. In the case of 16-bit systems, the additional memory needed for holding the check bits can be reduced when compared to conventional 16-bit EDACs.

The terminal functions for the 'ALS632B and 'AS632 are shown in Table 1.

Operational Description

Write Mode

During a memory write cycle, the EDAC is required to generate a 7-bit check word to accompany the 32-bit data word before being written into memory. To place the 'ALS632B and 'AS632 in the write mode, simply take S1 and S0 low. Output enable controls $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ must be taken high before the data word can be applied. Output enable control $\overline{\text{OECB}}$ must be taken low to pass the check word to the external bus.

The check word will be generated in not more than 30 ns for the 'ALS632B and 26 ns for the 'AS632 after the data word has been applied. The 'ALS632B and 'AS632 EDACs can be made to appear transparent to memory during the write mode because typical write times of most DRAMs are much larger than the propagation delay of data to check word.

Table 1. Terminal Functions for 'ALS632B and 'AS632

PIN NAME	DESCRIPTION
S1, S0	Selects the operating mode of the EDAC **S1 S0 MODE OPERATION** L L WRITE Input dataword and output checkword H L READ & FLAG Input dataword and output error flags H H CORRECT Latched input data and checkword/output corrected data and error syndrome code. L H DIAGNOSTIC Input various datawords against latched checkword/output valid error flags
DB0 through DB31	I/O port for entering or outputting data
$\overline{OEB0}$ through $\overline{OEB3}$	Three-state control for the data I/O port. A high allows data to be entered; and a low level outputs the data. Each pin controls 8 data I/O ports (or one byte). $\overline{OEB0}$ controls DB0 through DB7, $\overline{OEB1}$ controls DB8 through DB15, $\overline{OEB2}$ controls DB16 through DB23, and $\overline{OEB3}$ controls DB24 through DB31.
$\overline{OEDB}$ (ALS634, ALS635)	Three-state control for the data I/O port. A low level allows data to be outputted and a high allows data to be entered.
$\overline{LEDB0}$	Controls the dataword output latch. When low, the data output latch is transparent. When high, the latch stores whatever data was setup at its inputs when the last low to high transition occurred on the pin.
CS0 through CS6	I/O port for entering or outputting the checkword. It is also used to output the syndrome error code during the error correction mode.
$\overline{OECS}$	Three-state control for the checkword I/O port. A high allows data to be entered and a low allows either the checkword or syndrome code (depending on EDAC mode) to be outputted.
$\overline{ERR}$	Single Error output flag, a low indicates at least a single bit error.
$\overline{MERR}$	Multiple Error output flag, when low indicates two or more errors present.

Read-Flag-Correct Operation

During a memory read cycle, the function of the these EDACs is to compare the 32-bit data word against the 7-bit check word previously stored in memory. It will then flag and correct any single-bit error which may have occurred. Single bit errors will be detected through the $\overline{ERR}$ flag and double bit errors will be detected through the $\overline{MERR}$ flag. Figure 1 shows a typical timing diagram of the read-flag-correct operation.

When S0 is taken high, the EDAC will internally begin the correction process, although it should be noted that the error flags are enabled while in the read mode. For many applications, the simplest operation can be obtained by always executing the correction cycle, regardless if a single-bit error has occurred.

Important Timing Considerations for Read-Flag-Correct Mode

The most frequently asked question for an EDAC is how fast can a correction cycle be executed. Before S0 can be taken high, the data and check word must be set up at least 5 ns. In addition, the data and check word must be held for at least 10 ns after S0 goes high. This ensures the data and check word is saved in the EDAC's input latches. After the hold time has been satisfied, the source which is driving the data bus can be placed in high impedance and the EDAC's output drivers can be enabled. This is accomplished by taking $\overline{OEB0}$ through $\overline{OEB3}$ low.

If the minimum data setup time is used as a reference, and the output drivers are enabled after the minimum data hold time, then correction will be accomplished in not more than 37 ns for the 'ALS632B and 32 ns for the 'AS632.

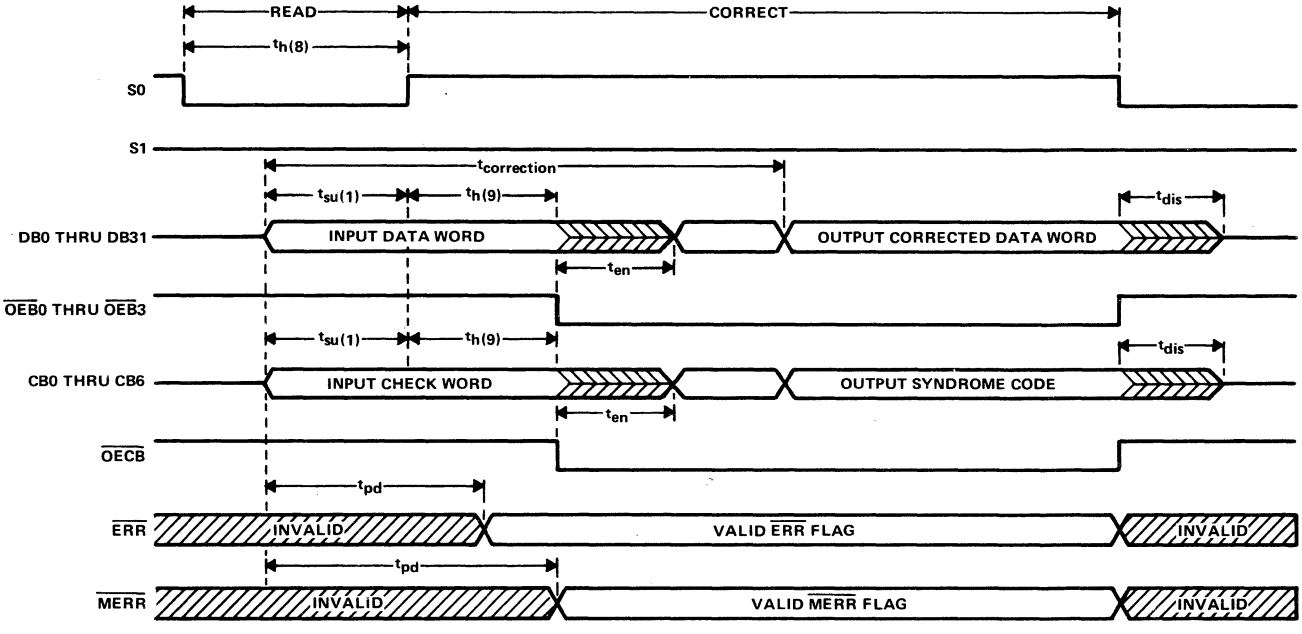

Figure 1. Read-Flag-Correct Timing Diagram

Read-Modify-Write Operations

The 'ALS632B and 'AS632 contain the necessary hardware to perform byte-write operations. When performing a read-modify-write function, typically the user would first want to perform the read-flag-correct cycle as discussed before and shown in Figure 1. This ensures that corrected data is used at the start of the modify-write operation.

The corrected data is then latched into the output data latch by taking $\overline{\text{LEDBO}}$ from low to high. Upon completing this, modifying any byte or bytes is easily accomplished by taking the appropriate byte control $\overline{\text{OEB0}}$ through $\overline{\text{OEB3}}$ high. This allows the user to place the modified byte or bytes back onto the data bus while retaining the other byte or bytes. An example of a read-modify-write for byte 0 is shown in Figure 2. Since the check word is no longer valid for the modified data word, a new one is easily generated by taking S0 and S1 low. After the appropriate propagation delay, the new check word will be available.

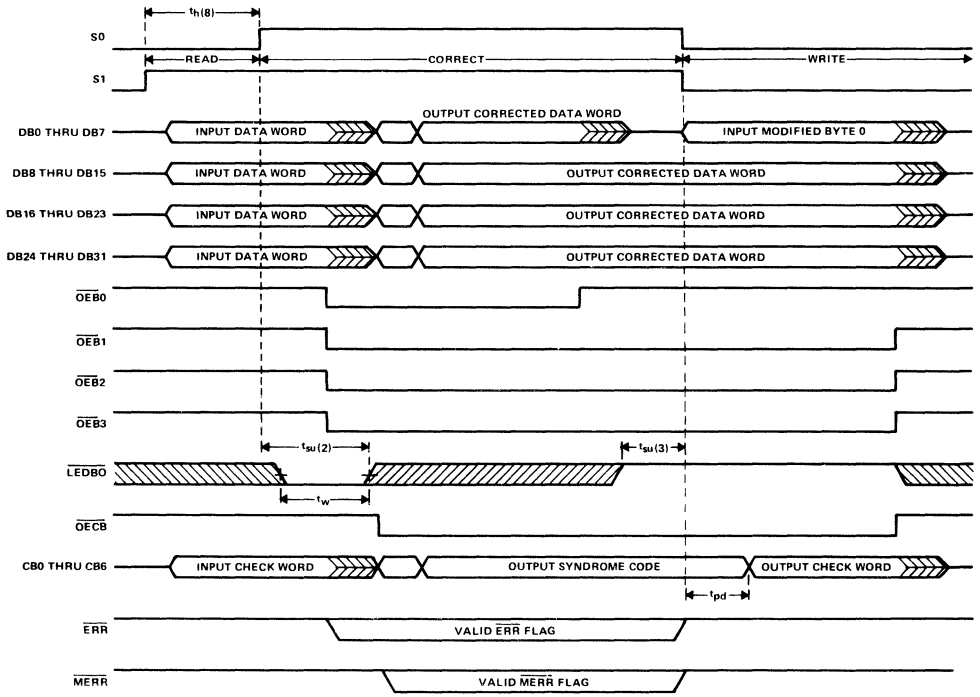

Figure 2. Read-Modify-Write Operation

Important Timing Considerations for Read-Modify-Write Operations

$\overline{\text{LEDBO}}$ should not be brought from low to high until 30 ns for the 'ALS632B and 25 ns for the 'AS632 after S0 goes high. 'AS632. This will ensure that corrected data is latched into the data output latches. On the other hand, $\overline{\text{LEDBO}}$ should be brought high no later than 0 ns before S0 and S1 goes low. Again, this is to ensure that the corrected data is stored into the data output latches. Also of importance is the new check word will be available no later than 32 ns after S0 and S1 goes low for the 'ALS632B and 28 ns for the 'AS632.

Diagnostic Mode Operation

The purpose of the diagnostic mode is to provide the user with the capability of easily detecting when the EDAC or memory is failing. There are several possibilities as to how a user might employ this feature, but Figure 3 shows a typical timing diagram of some diagnostics which can be performed with these devices. Generally, the user would first place the EDAC in the read mode (S0 = L, S1 = H), then apply a valid check word and data word. A valid check word is defined as a check word for which the user knows the associated data word. The user would next place the EDAC into the diagnostic mode by taking S0 high and S1 low. This latches the valid check word into its input latches but leaves the data input latches transparent. To verify that the valid check word was latched properly, $\overline{\text{OECS}}$ can be taken low causing the valid check word to be placed back onto the bus. Since the data input latches remain transparent, this allows the user to apply various diagnostic data words against the valid check word. A diagnostic data word is one in which either a single or double bit error exists. In either case, the error flags should respond. The output data latch can be verified by taking $\overline{\text{LEDBO}}$ high and confirming that the stored diagnostic data word is the same. This is made possible because error correction is disabled while in the diagnostic mode (S0 = H, S1 = L). Taking S1 high and $\overline{\text{LEDBO}}$ low will verify that the EDAC will correct the data word. Also, the error syndrome code can be verified by taking $\overline{\text{OECB}}$ low.

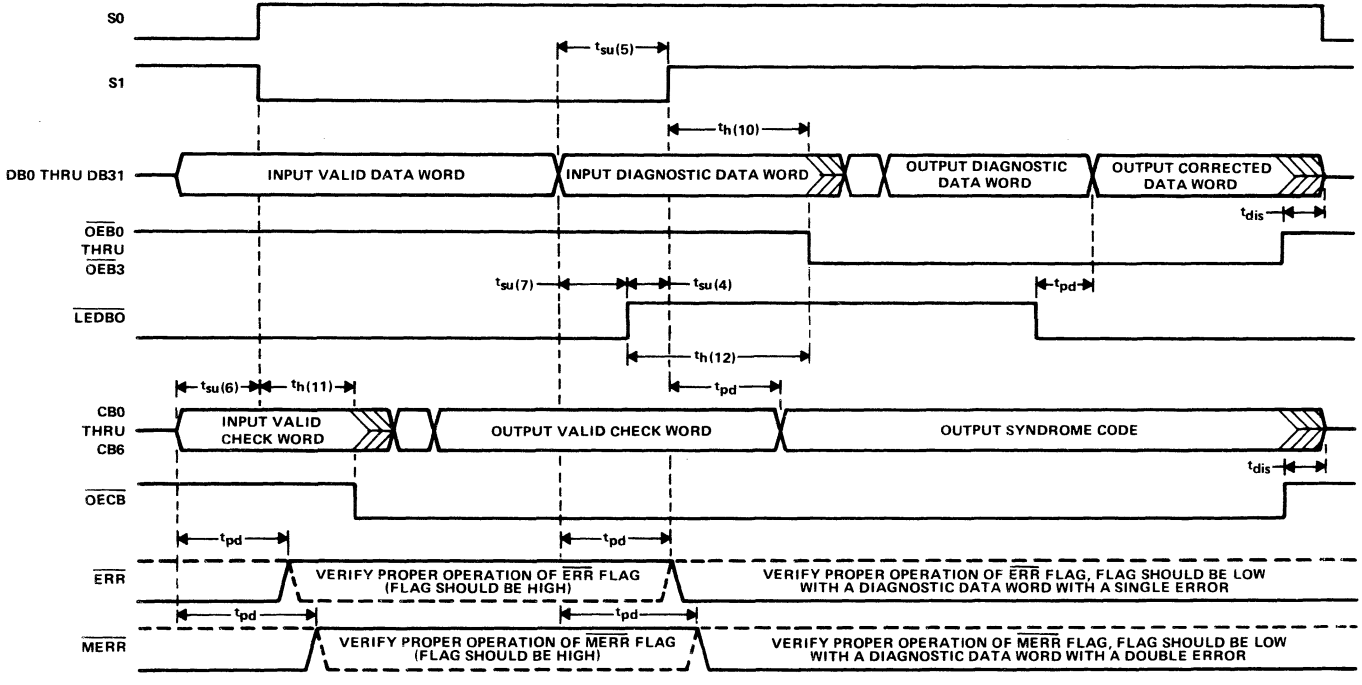

Figure 3. Diagnostic Mode Timing Diagram

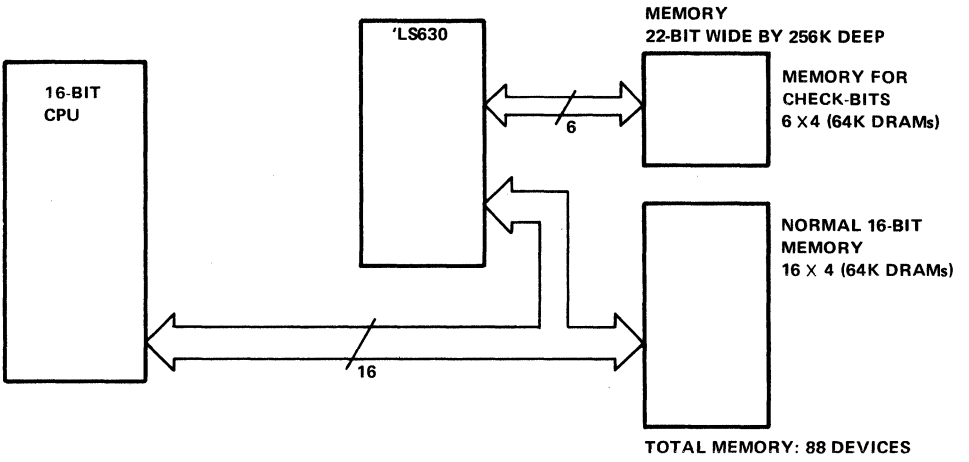

Figure 4. 16-Bit System Using Conventional 16-Bit EDAC

16-Bit Systems Using the 'ALS632B and 'AS632 EDACs

The 'ALS632B and 'AS632 EDACs can reduce the memory size required in 16-bit systems where conventional 16-bit EDACs (6 check bits, 16 data bits) are presently used. Figure 4 shows the typical system architecture for the 16-bit EDAC. In this system, 88 devices would be required for the 22-bit × 256K memory array, assuming 64K DRAMs are used. It is easy to see that 27.3% or 24 devices are required for storing the check bits. When using the 'ALS632B and 'AS632 EDACs, the memory required for the check bits can be reduced to 17.9% or only 14 devices. This reduces the total number of DRAMs required by 10 devices. Figure 5 shows the architecture when using the 32-bit EDAC. The four 'ALS646s are used to group two 16-bit data words into one 32-bit data word. In addition, this type of system can be used in byte-write operations where the other system cannot.

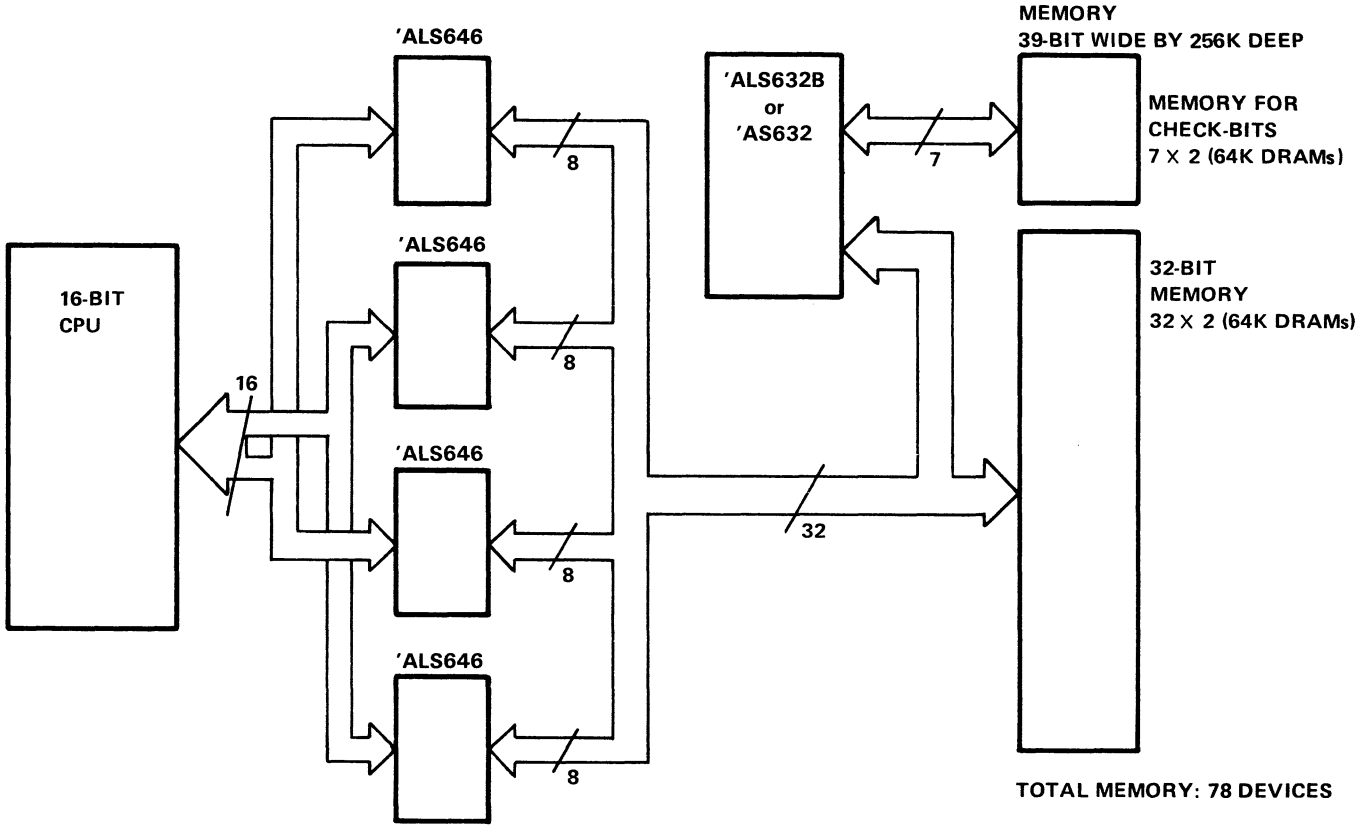

Figure 5. 16-Bit System Using 32-Bit EDAC

SN74AS6364 Flow-Through EDAC

An Improved Method of Error Correction

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Contents

List of Illustrations

Introduction

With the increasing size of memory in electronic equipment, the need to implement Error Detection And Correction (EDAC) has increased to ensure memory integrity and to improve equipment reliability. The Texas Instruments SN74ALS632 and SN74AS632 have been leading the way in the 32-bit EDAC market over the past several years and now TI is leading the way in the 64-bit EDAC market with a new flow-through architecture by introducing the SN74AS6364. This application report shows the different configurations of designing with the flow-through architecture. Two specific examples of interfacing the 'AS6364 with the MC68030 microprocessor are given in this application report; the correct-always configuration, with optional memory-scrubbing, and the correct-only-on-error configuration. The purpose of this application report is to explain the use of the 'AS6364 and to show the advantages of the flow-through architecture. Deciding whether to use an EDAC is left to the designer.

Flow-Through Architecture

A conventional EDAC uses a single I/O port to access memory and processor data for detecting and correcting data errors. One disadvantage of this single I/O port operation is that, during the memory read and write operations, both input and output operations share the same port and one operation must wait for the other to be completed. The I/O port has to be turned around from input to output or vice versa. This turn-around time contributes significantly to correction time when using conventional EDACs.

With the flow-through architecture, the I/O port turn-around time is eliminated by having two separate I/O ports, the processor I/O port and the memory I/O port. During a memory-write cycle, the processor I/O port functions as an input and the memory I/O port functions as an output. During read cycles, these functions are reversed. The correction-speed advantage of this architecture stems from the processor being able to read and write through the EDAC without having to wait for the I/O port turn-around time. The unique flow-through architecture of the 'AS6364 is such that the bus transceiver function, which is required in most memory designs, is also integrated into the flow-through architecture. This feature makes memory system design using the 'AS6364 as simple as putting a transceiver on the data bus. When the EDAC is in transceiver mode, bypassing the correction circuitry, the propagation delay through the EDAC is faster than the propagation delay when the EDAC is correcting data. The correct-only-on-error mode, explained later, takes advantage of this faster propagation delay specification.

'AS6364 Functional Description

The 'AS6364 is a 64-bit EDAC with two 64-bit parallel I/O ports and control signals similar to that of the 'AS245 bus transceiver (see Figure 1). For the processor bus interface, one of the 64-bit I/O ports, D0-63, are provided with 48-mA drive capability. The memory data bus (MD0-63) supports 12-mA drive with a balanced output impedance of 25 Ω high and low.

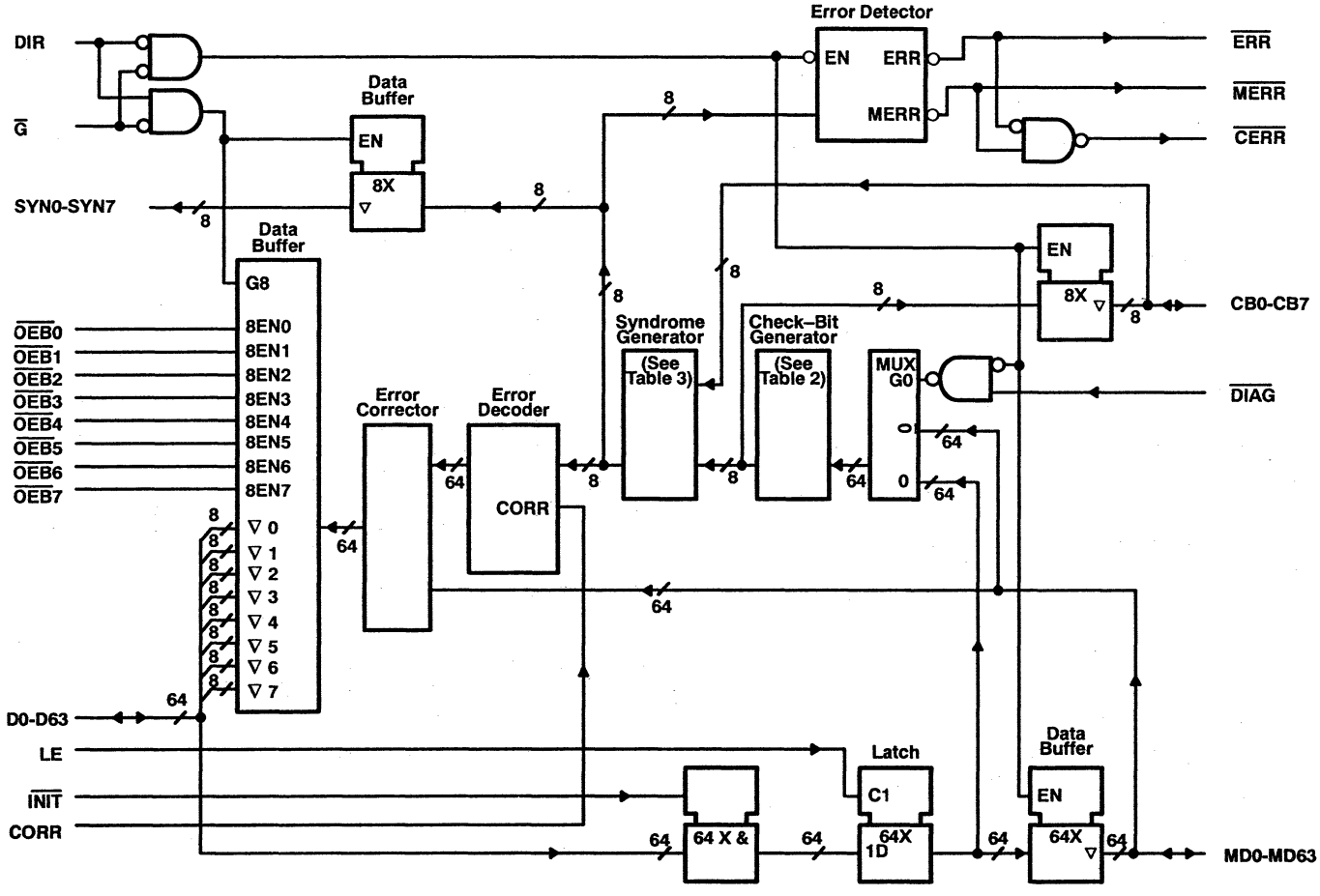

Figure 1. Functional Block Diagram of the 'AS6364

Three error flags are provided for the system interface; $\overline{ERR}$, $\overline{MERR}$, and $\overline{CERR}$. The single-bit error flag, $\overline{ERR}$, informs the system that there is at least a single-bit error. $\overline{MERR}$, on the other hand, informs the system that there is at least a double-bit error. The correctable-error condition of $\overline{ERR}$ = low and $\overline{MERR}$ = high is indicated by the $\overline{CERR}$ flag.

To make the interface simple, the 'AS6364 has the same data-flow control as used on conventional bus transceivers, such as the SN74AS245: a direction (DIR) pin and output enable ($\overline{G}$) pin. In addition to the master output-enable control signal, there are eight output-enable control lines ($\overline{OEB}$0-7) on the processor side for byte write operations. Other control signals consist of CORR, LE, $\overline{INIT}$, and $\overline{DIAG}$ signals.

A high on the CORR input enables the internal correction circuitry. When the correctior circuit is disabled (CORR low), the 'AS6364 passes the data straight from the memory bus to the processor bus and puts the EDAC in the transceiver mode.

The latch enable signal, LE, controls the latching function from the processor bus to the memory bus. A low level on this signal latches the data on the processor bus.

For memory initialization, a low on $\overline{INIT}$ during write cycles forces the memory data outputs low and generates the appropriate set of check bits.

Running diagnostics are possible via the $\overline{DIAG}$ input signal. This signal reverses data flow during read cycles by selecting the processor data through the input latches when $\overline{DIAG}$ is active (low). The selected data from the latches can then be compared with known sets of check bits applied through CB0-7.

To determine the data bit at fault during the read operations, the syndrome codes are available through the error syndrome bus (SYN0-7). The bit in error is located by decoding the syndrome bits according to the table given in the data sheet.

System Implementation

Two of the most common modes of EDAC system configurations are the correct-always mode and the correct-only-on-error mode. The CORR input on the flow-through architecture greatly simplifies the implementation of both of these modes.

As shown in Figure 4, correct-always mode can be implemented using the 'AS6364 by simply connecting the CORR signal to V_{CC} (logic high). Figure 9 is a block diagram of the correct-always setup with memory scrubbing. Notice that this setup uses two EDACs; one for normal memory-access cycles and one for memory-refresh cycles (memory scrubbing). Memory scrubbing is used to significantly reduce the probability of the dual-bit errors by reducing single bit errors from accumulating.

In correct-only-on-error mode, the CORR input is controlled by the timing controller based on the result of the error flags. If there is no error on the memory data bus, the flow-through EDAC simply acts like a bus transceiver, passing the data from the memory data bus to the processor data bus. This correct-only on-error mode is faster because the correction circuitry is bypassed in this mode. Figure 12 is a block diagram of the correct-only-on-error implementation.

The following paragraphs explain in detail how these three different configurations are implemented in a system using the 20-MHz MC68030 processor and the TMS44400-80 DRAM. Figure 2 shows a typical processor access cycle with all the timing details of the memory control signals. This figure in conjunction with the above mentioned block diagrams will form the basis for all the timing diagrams.

Correct-Always Configuration

The correct-always configuration is one of the simplest ways to implement error detection and correction into a system. This implementation becomes as easy as putting a bus transceiver between the processor and the memory data bus. The flow chart for this implementation is given in Figure 3. Figure 4 is the system block diagram of how correct-always mode can be implemented for a 32-bit system. For a 32-bit system, only seven check bits (CB0-6) are used. The corresponding data bits to these seven check bits are described in the footnote of the diagram.

Normal Read and Write Cycle

Read and write cycles from memory are controlled by the AS, IO/M (A23), and R/W signals of the processor. The direction signal (DIR) of the timing controller is derived from these three signals and controls the read and write operations on both the EDAC and DRAM. To control the direction of the EDAC, the DIR signal from the timing controller is connected directly to the DIR pin on the EDAC. The same DIR signal is inverted and connected to the output enable ($\overline{G}$) pin of the DRAM. This same signal is delayed by 15 ns and connected to the write ($\overline{W}$) pin of the DRAM. Figure 5 shows the timing sequence of all the control signals for normal read and write operations. For these operations, the $\overline{ERR}$ flag is always high indicating that there are no errors associated with the memory data bits during read cycles.

On the Motorola MC68030 processor, the falling edge of AS indicates that there is a valid address on the processor address bus. The timing controller, cycling between the idle state and the $\overline{RAS}$ delay state, checks for a refresh request ($\overline{REFREQ}$) and access request via A23 which is used to define main (DRAM) memory address space. If A23 indicates a main memory access just before the high to low transition of the AS signal, the timing controller goes into the access-check cycle where it checks the read/write (R/$\overline{W}$) signal and the IO/$\overline{M}$ signal to determine the type of access cycle, either a read-access or a write-access cycle to the DRAM. After this decision, the timing controller issues the appropriate $\overline{RAS}$ and $\overline{CAS}$ signals, DIR signal, and the output enable signals (see Figure 5). If there is no error near the end of the cycle, as indicated by the $\overline{ERR}$ flag of the EDAC, the access cycle is terminated.

Read and Correct Cycles

When a data bit is in error during a read cycle, the data bit is automatically corrected by the flow-through EDAC when data is presented by the processor data bus. This is a feature of the correct-always mode where the CORR signal of the EDAC is tied directly to V_{CC} (to always put the EDAC in the correct mode). The corrected data is then latched into the

EDAC's data latch with the LE signal of the timing controller (refer to Figure 6). This latched data is used later during the correct cycle to write the corrected data back into DRAM. The $\overline{ERR}$ flag signals the timing controller to go through the correct cycle, right after the read cycle. As shown in Figure 6, the correction cycle is similar to a normal write cycle. During a correct cycle, the corrected data previously stored in the EDAC's input latch is used as data for the memory write cycle. This stored data enables the memory system to write to the DRAMs within three clock cycles.

As shown in the timing diagram, the basic read cycle remains unchanged for this read and correct cycle combination. Because the latched data is written back into memory, the first read cycle does not suffer any speed penalty. This is one advantage of the correct-always mode. The penalty for the correction cycle is incurred only when there is an access cycle following a read cycle. The following paragraphs explain how this back-to-back access cycle is handled by the timing controller.

Read and Correct/Access Cycle

Right after each read cycle, the $\overline{ERR}$ flag is checked for a single-bit error condition as mentioned in the previous paragraph. A low level on the $\overline{ERR}$ flag indicates that there was an error during the read cycle and the data must be written back into DRAM. At this point, the timing controller takes control of the memory bus and the corrected data stored in the EDAC's latch is written back to DRAM. This process takes three complete clock cycles after the read operation. If another access cycle is requested during the correct cycle, the access cycle will be delayed by the three clock cycles which are needed to write the corrected data back to DRAM. After the correct cycle, the IO/M input is checked for any access which may have been requested during the correct cycle. A low IO/M signal indicates a pending access request which causes the timing controller to go to the access cycle. Figure 7 illustrates the timing sequence of this read, correct, and access cycle combination.

The read and correct cycle shown in Figure 7 is similar to that shown in Figure 6. The addition of the access cycle in Figure 7 is initiated by the high-to-low transition of the AS signal, which in turn causes the IO/M signal to go low. The delay in an access cycle is controlled by inserting wait states to the processor via the $\overline{DSACK}$ signal. As Figure 7 illustrates, the appropriate direction, enable, $\overline{RAS}$, $\overline{CAS}$, and other control signals are issued for the access cycle, which is identical to normal read or write cycles shown previously.

Refresh and Access Cycles

As shown in the flow chart of Figure 3, the request for a refresh cycle is checked before every access cycle. Refresh request has a higher priority if access and refresh are being requested at the same time. If the refresh request occurs during an access cycle, the refresh cycle will follow immediately after the access cycle. If an access request occurs during the refresh cycle, the access cycle is delayed until the refresh cycle is completed. Again the IO/M signal is used to indicate to the timing controller that there is a pending access cycle. The sequence of how the access cycle takes place after a refresh cycle is shown in Figure 8. The transition sequence between refresh and access cycle uses the same method as the correct and access

cycle combination, as described in the previous paragraphs where the DSACK signal is used to insert wait states which in turn delays the access cycle.

Memory scrubbing is a method of correcting errors during refresh cycle. Because of the speed advantages of the flow-through architecture, implementing memory scrubbing does not penalize system performance as much as traditional EDAC implementations. The following paragraphs give the details of memory scrubbing in correct-always mode using two 'AS6364s.

Correct-Always Configuration with Memory Scrubbing Option

Memory scrubbing is implemented using two EDACs (see Figure 9). One EDAC is used for normal access cycles and the scrubbing EDAC is used for refresh cycles. The underlying idea behind memory scrubbing is to reduce the occurrence of dual-bit errors by eliminating (or scrubbing) single-bit soft errors, thereby preventing their accumulation. Therefore, even if the system is in the idle state, the entire memory still gets checked for errors once every 16.384 s, when 4 banks of 1M × 4 DRAMs are used as shown in Figure 9. In some systems, memory scrubbing may be the only error-correction scheme necessary to fulfill the reliability requirements.

Refresh with Scrubbing and Access Cycles

To implement scrubbing, an extra EDAC must be used for this flow-through architecture. The function of the original (access) EDAC is the same as in the correct-always mode. It will still correct the single-bit errors during read operations and will write back to DRAM to update memory during read cycles. The extra (scrubbing) EDAC is used to correct errors during refresh cycles. At the beginning of a refresh cycle (see Figure 10), the direction signal (DIR) and the enable signal ($\overline{G}$) are driven to a state which enables the scrubbing EDAC to read data and its associated check bits from memory. Simultaneously, the access EDAC monitors the same data and check bits. If there is a single-bit error, indicated by the error flag of the access EDAC, the memory is written back with data which has been corrected by the scrubbing EDAC. Throughout this process, the processor data bus (D0-63) of the access EDAC is disabled by keeping the output enable signal ($\overline{G}$) high. By keeping the data bus disabled, the processor is free to use the data bus for non-memory accesses. For memory scrubbing, the refresh cycle must be extended by three clock periods to make a decision on whether or not there is an error. These extra clock periods appear as CNT3-5 as shown in Figure 10. If the error flag is low at the end of CNT3, the controller scrubs the memory during CNT4 and CNT5. Otherwise, the refresh cycle terminates without scrubbing after CNT5. Any access that is requested during the refresh cycle is handled the same way as in the previously mentioned refresh and access cycle transition of the correct-always configuration. For this configuration, the access cycle is delayed until the refresh and memory scrubbing process is complete.

Correct-Only-On-Error Configuration

Correct-only-on-error eliminates some of the disadvantages of the correct-always mode which corrects data indiscriminately. Since the occurrence of errors is expected to be sparse,

correcting always may unnecessarily delay data during every read cycle. This is due to data having to go through the slower correction path. This is only a problem if this delay causes extra wait states on the microprocessor. The correct-only-on-error mode checks for errors before turning on the correction circuit of the EDAC. This feature enables data to flow through the EDAC faster for data which does not need correcting. The 8-ns difference between the two t_{pd} specs from MD_X and CB_X to D_X of the data sheet reflects the speed difference between these two paths. Figure 11 is a flowchart of the correct-only-on-error implementation. There are two noticeable differences between the system block diagrams of the correct-always mode (Figure 4) and the correct-only-on-error mode (Figure 12). First, the CORR signal of the EDAC in Figure 4 is always in the correct mode, as opposed to the CORR signal being driven by the timing controller in Figure 12. Second, the $\overline{ERR}$ flag also drives the $\overline{BERR}$ and $\overline{HALT}$ inputs of the processor to rerun a read cycle when the error occurs while the controller is in a read cycle (indicated by DIR high). The gating of DIR and $\overline{ERR}$ (see Figure 12) allows the processor not to have bus error conditions during write cycles. In the correct-always mode, the error flag simply drives the $\overline{ERR}$ input of the timing controller. The rest of the configuration of correct-only-on-error mode shown in Figure 12 is similar to the correct-always mode shown in Figure 4.

Normal Read and Write Cycles

The basic sequence of the write cycle is identical to the correct-always mode, where AS, IO/$\overline{M}$, and R/$\overline{W}$ initiates the cycle. For read cycles, the only difference is the early availability of data on the processor bus because the correction circuit of the EDAC is bypassed. The CORR signal of the EDAC shown in Figure 13 is kept low throughout these read and write cycles because of the no error condition. During the read cycle, the decision to keep CORR signal low is the result of the $\overline{ERR}$ flag going high, which indicates that there are no errors.

Read and Correct Cycles

The transition between the read and the correct cycles is the main distinguishing factor between the correct-always mode and the correct-only-on-error mode. Figure 14 shows the $\overline{ERR}$ flag going low after the low-to-high clock transition of CNT3 during read cycles. A low $\overline{ERR}$ flag is caused by a single bit error. At the end of CNT3, the timing controller decides to go into a modify-write cycle based on the low $\overline{ERR}$ flag condition. In the meantime, the processor is being halted by the $\overline{ERR}$ flag since it is connected to the $\overline{BERR}$ (bus error) and $\overline{HALT}$ signals of the processor through the NAND gate. While the processor cycle is being halted by the $\overline{BERR}$ and $\overline{HALT}$ signals, the timing controller takes control of the memory bus to correct the memory bit in error (modify-write cycle shown in Figure 14). This modify-write cycle is different from typical DRAM modify-write cycles in that the latched address of the DRAM controller SN74ALS6301 is used to write to memory. The latching operation of 'ALS6301 is also controlled by the $\overline{ERR}$ flag. After completion of the modify-write cycle, the processor rerun feature of the MC68030 retries its original read cycle and terminates the cycle when there are no errors.

Refresh and Access Cycles

Access requests coming in during refresh cycles for the correct-only-on-error operation are handled the same way as the correct-always mode. Again, the timing controller makes use of the IO/$\overline{M}$ signal to check for the pending access request. This signal is checked at the end of refresh cycle to determine whether there is a pending access request. Figure 15 illustrates the transition between the refresh and access cycle.

Timing Controller Implementation

Three sets of timing controller files and their functional test vectors for each of the implementations are given in the appendix; one file each for correct-always mode and correct-only-on-error mode, and two files for the memory scrubbing option. The timing controllers are implemented using the TI programmable sequence generator TIBPSG507A (refer to data sheet document number SRPS002A). Because of the additional outputs required by the memory scrubbing option, two of the TIBPSG507A devices (two files in the appendix) are used. ABEL™ development software, which supports the TIBPSG507A, is used to reduce and generate the fuse map required to program the device.

Summary

By taking advantage of the flow-through architecture of the 'AS6364, a designer can improve his memory system design in two ways. One way is the overall performance improvement of the system which is achieved by the speed advantage and simplicity of using the flow-through architecture over conventional EDACs. The second advantage is achieved through board space savings. The wide data bus, heavy-duty bus driving capability, and the integration of the transceiver function greatly contribute towards board space savings.

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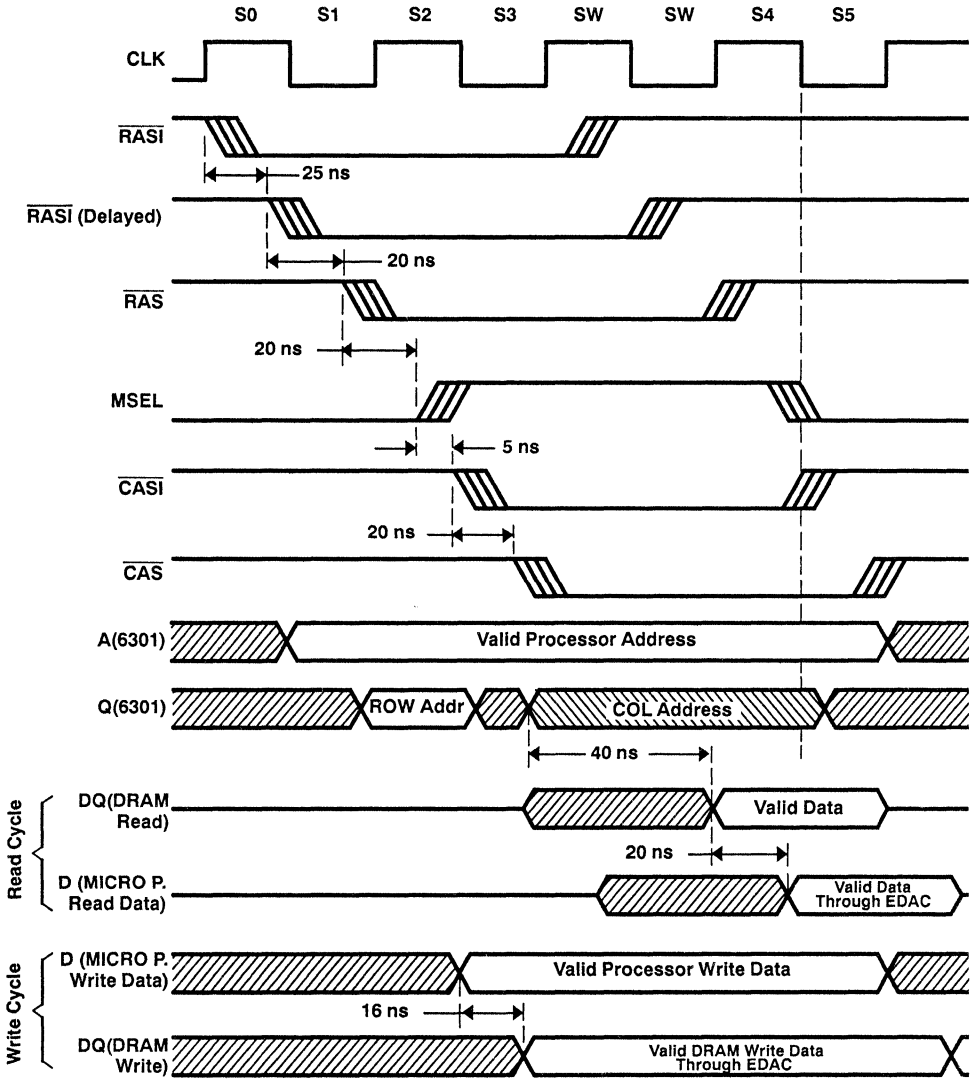


Figure 2. Details of DRAM Controller and DRAM Signals for Typical Access Cycle

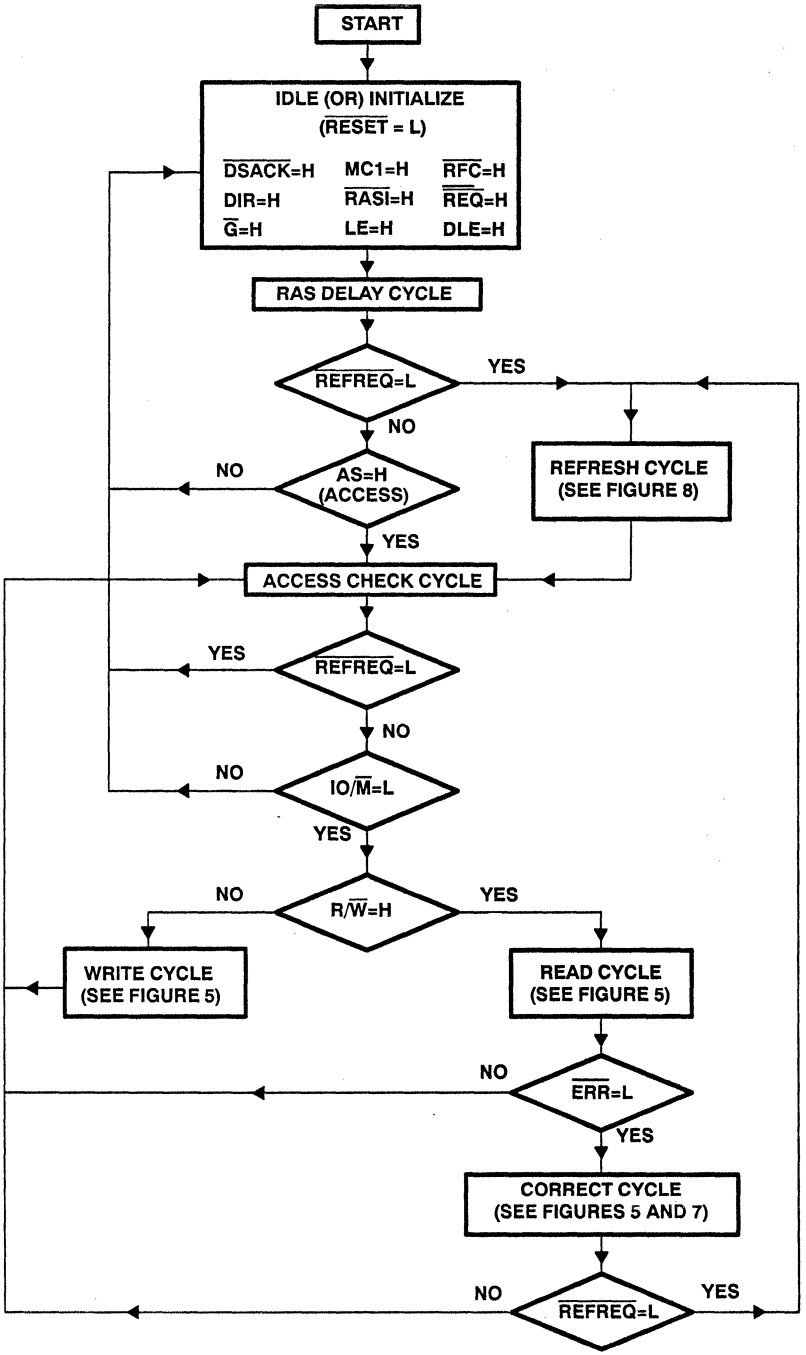
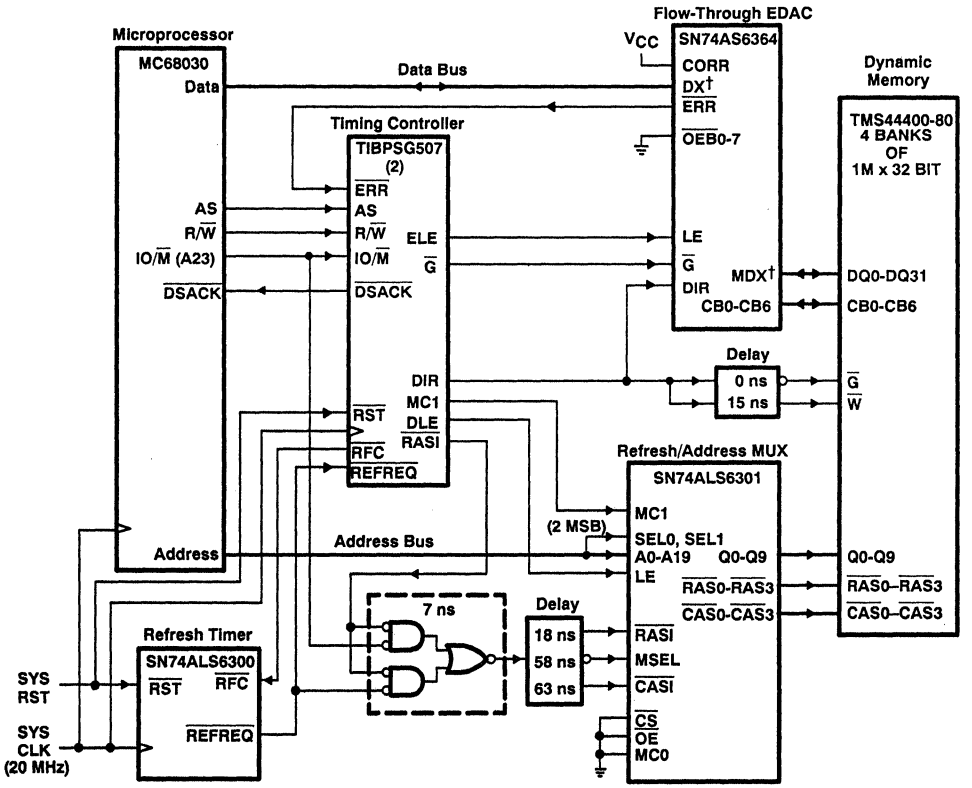


Figure 3. Correct-Always Mode Flowchart



† For 32-bit data bus MDX consists of MD8-15, MD16-23, MD32-39, and MD56-63, and DX consists of D8-15, D16-23, D32-39, and D56-63.

Figure 4. Flow-through EDACs Correct-Always Mode Interface

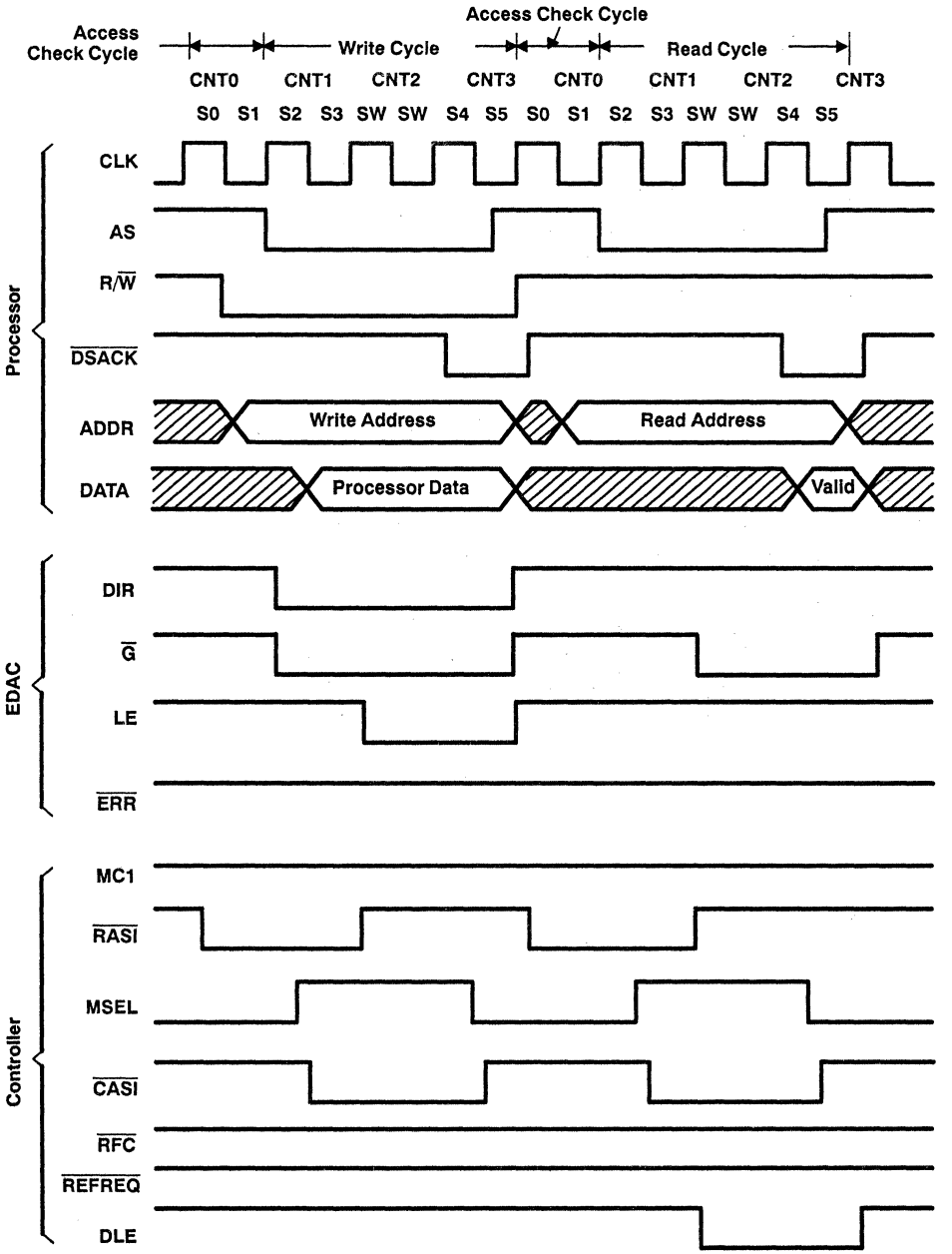


Figure 5. Normal Read and Write Cycle

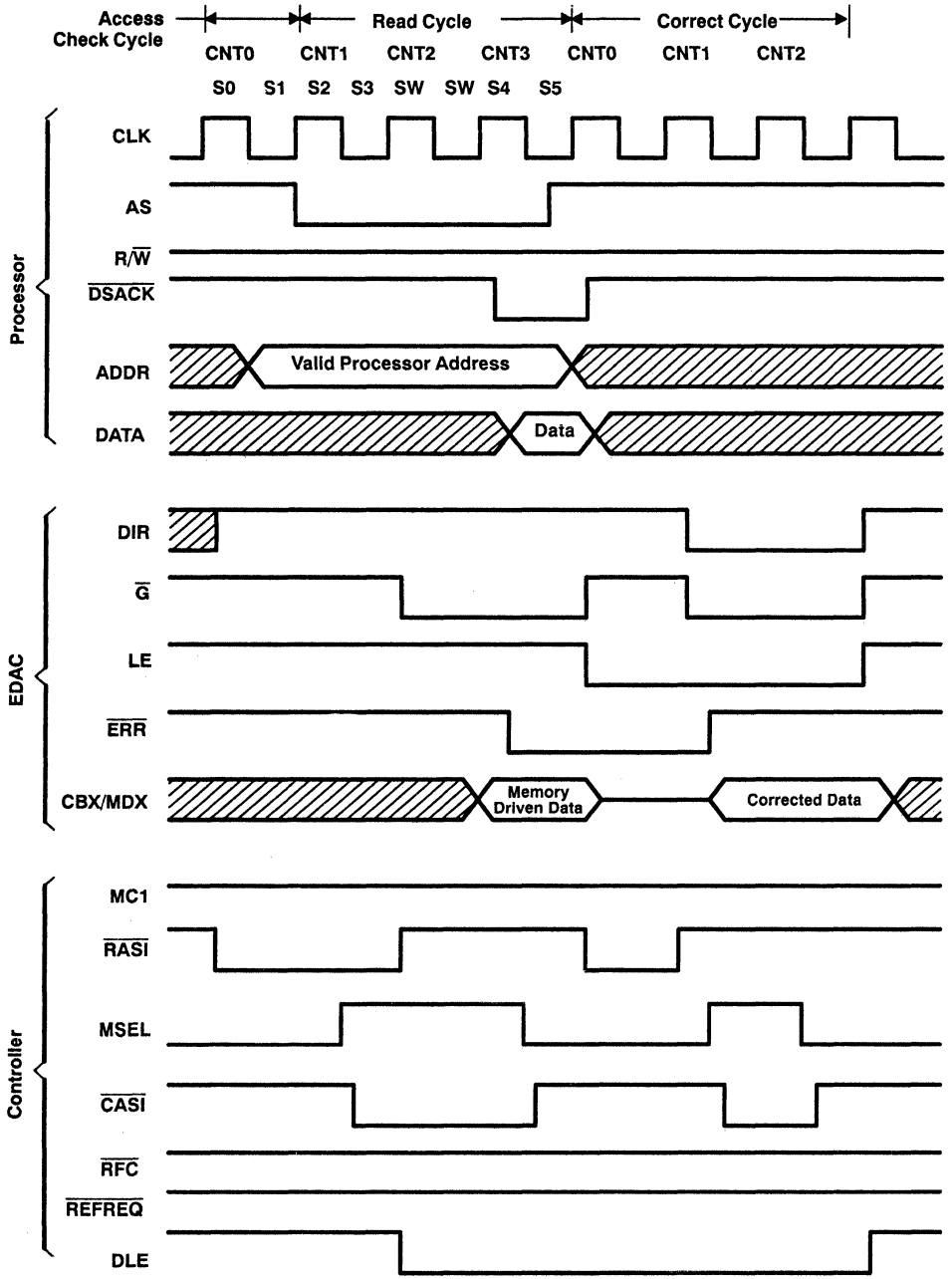


Figure 6. Read and Correct Cycle

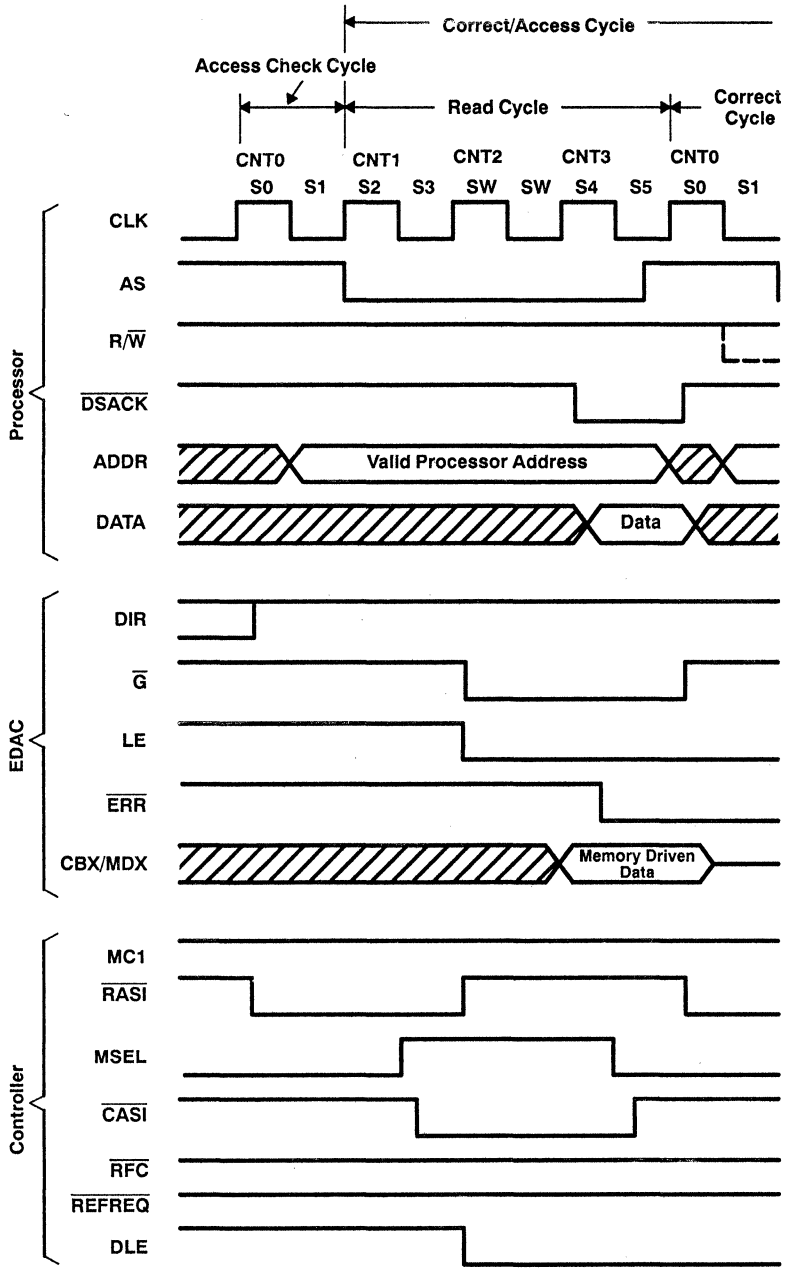


Figure 7(a). Read and Correct/Access Cycle

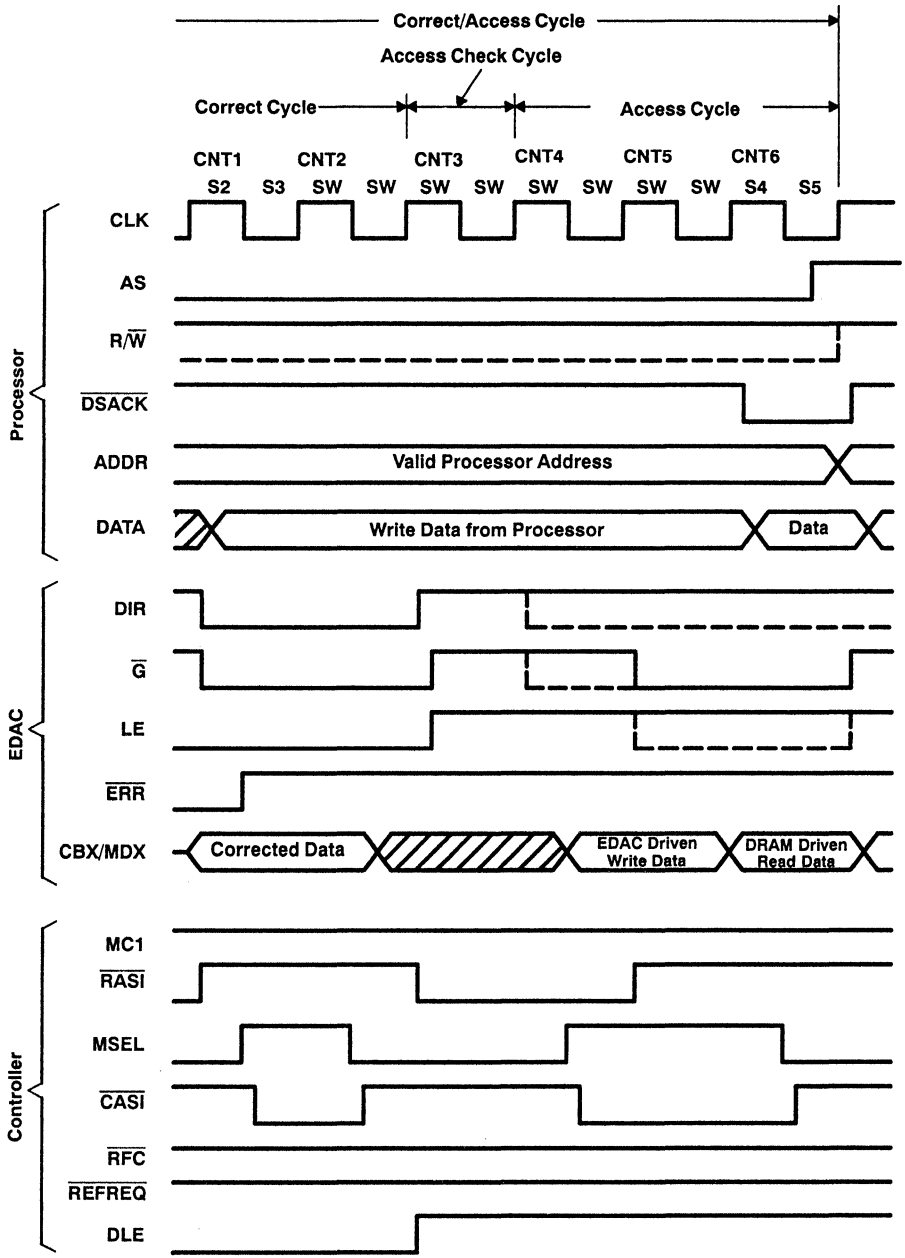


Figure 7(b). Read and Correct/Access Cycle

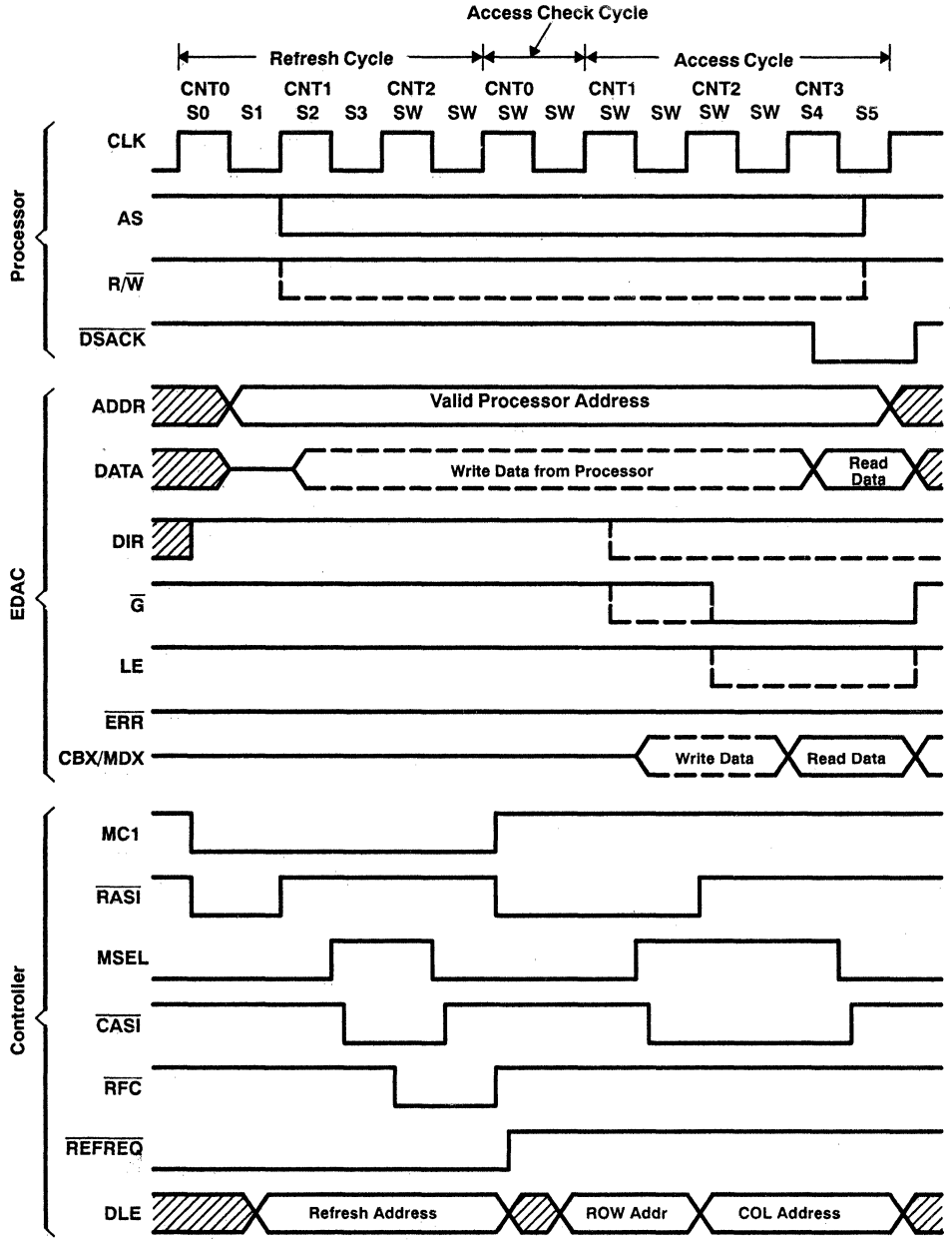


Figure 8. Refresh and Access Cycle

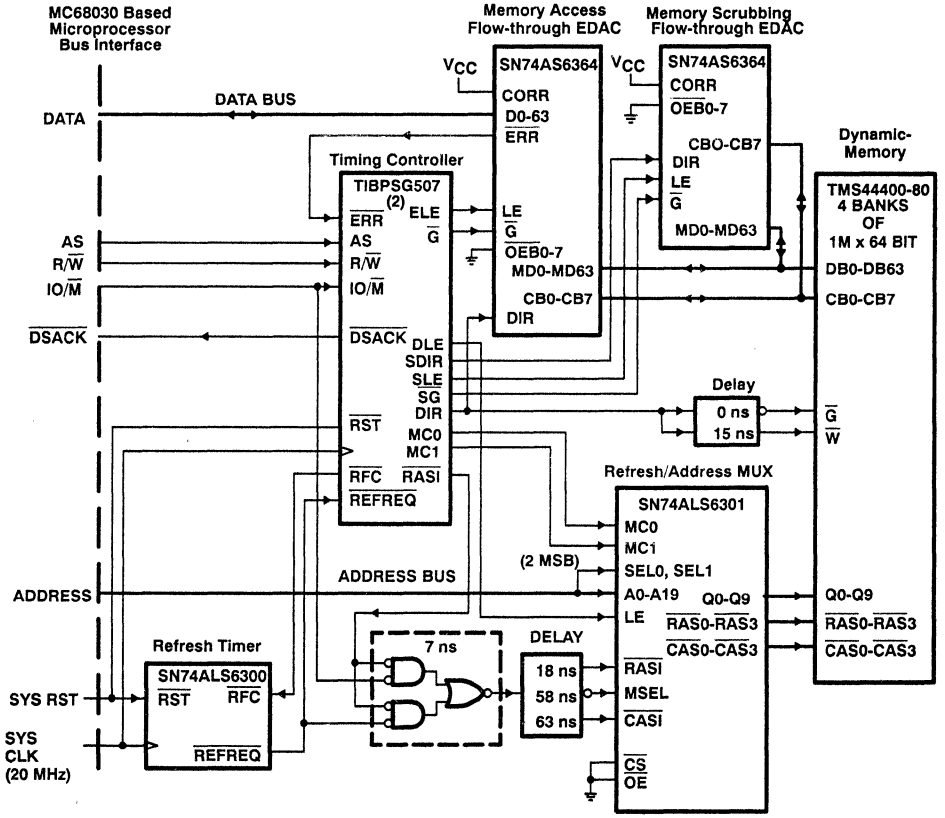


Figure 9. Flow-through EDACs Correct-Always Mode with Memory Scrubbing

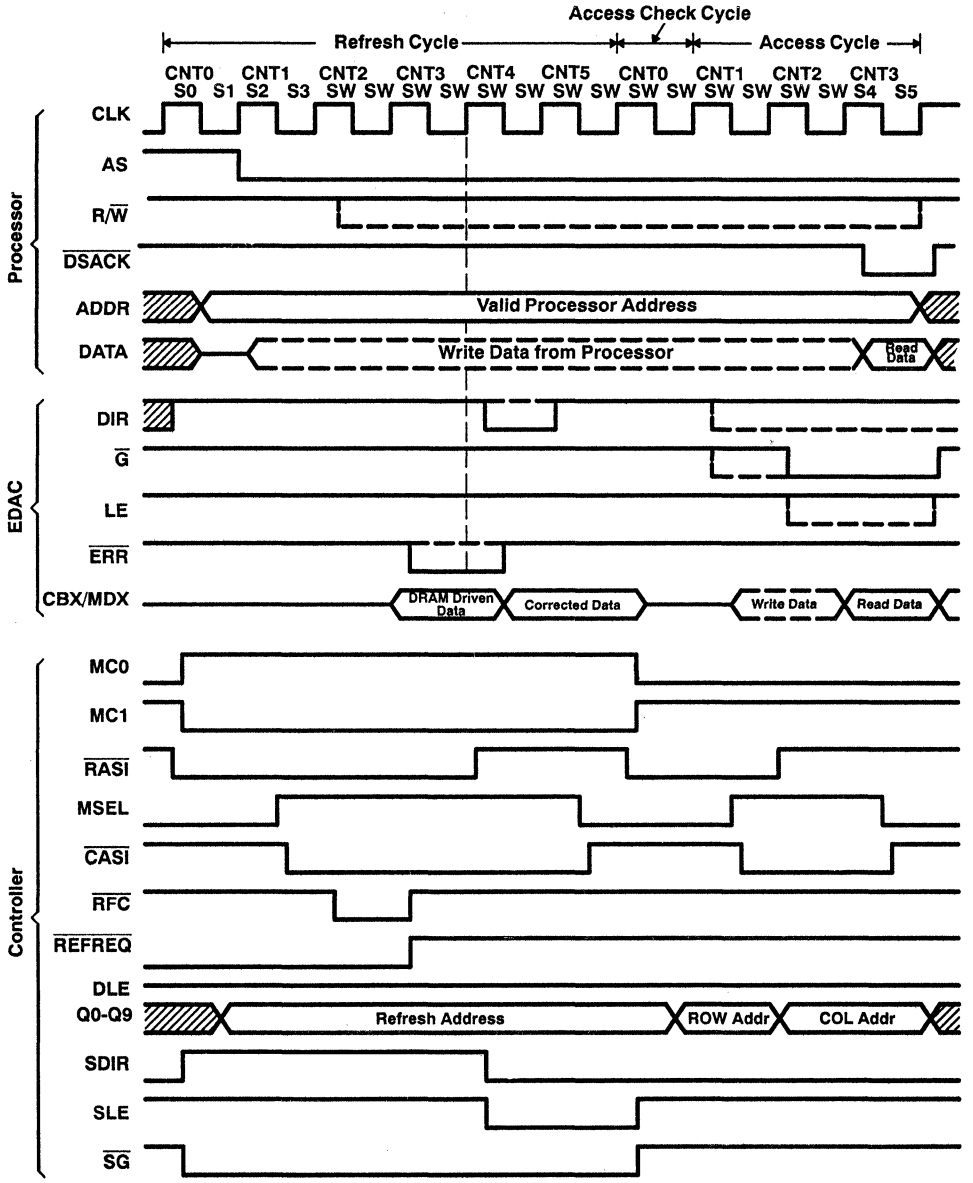


Figure 10. Refresh with Scrubbing and Access Cycle

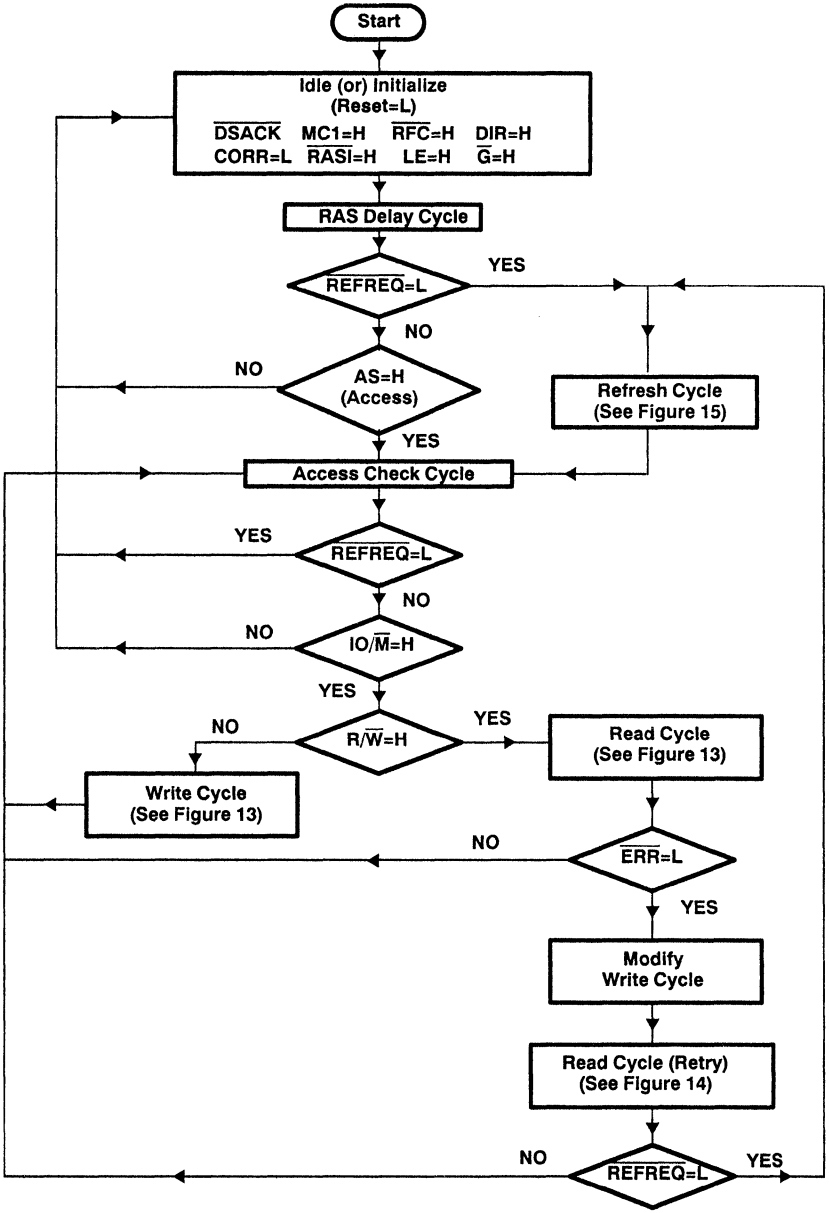


Figure 11. Correct-Only-on-Error Mode Flowchart

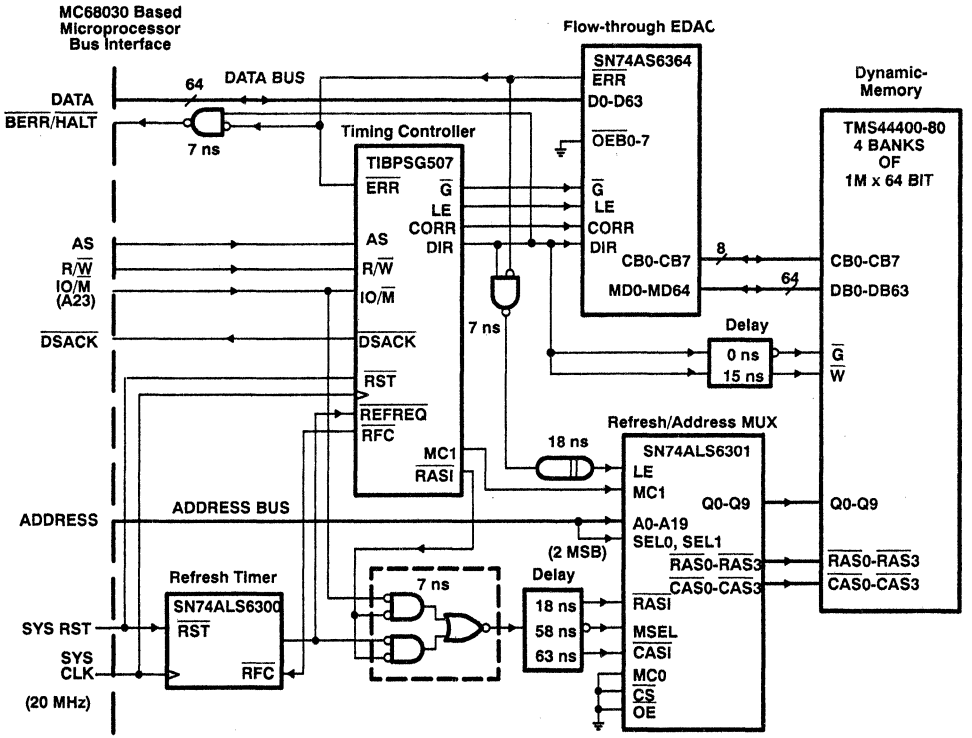


Figure 12. Flow-through EDACs Correct-Only-on-Error Mode Interface

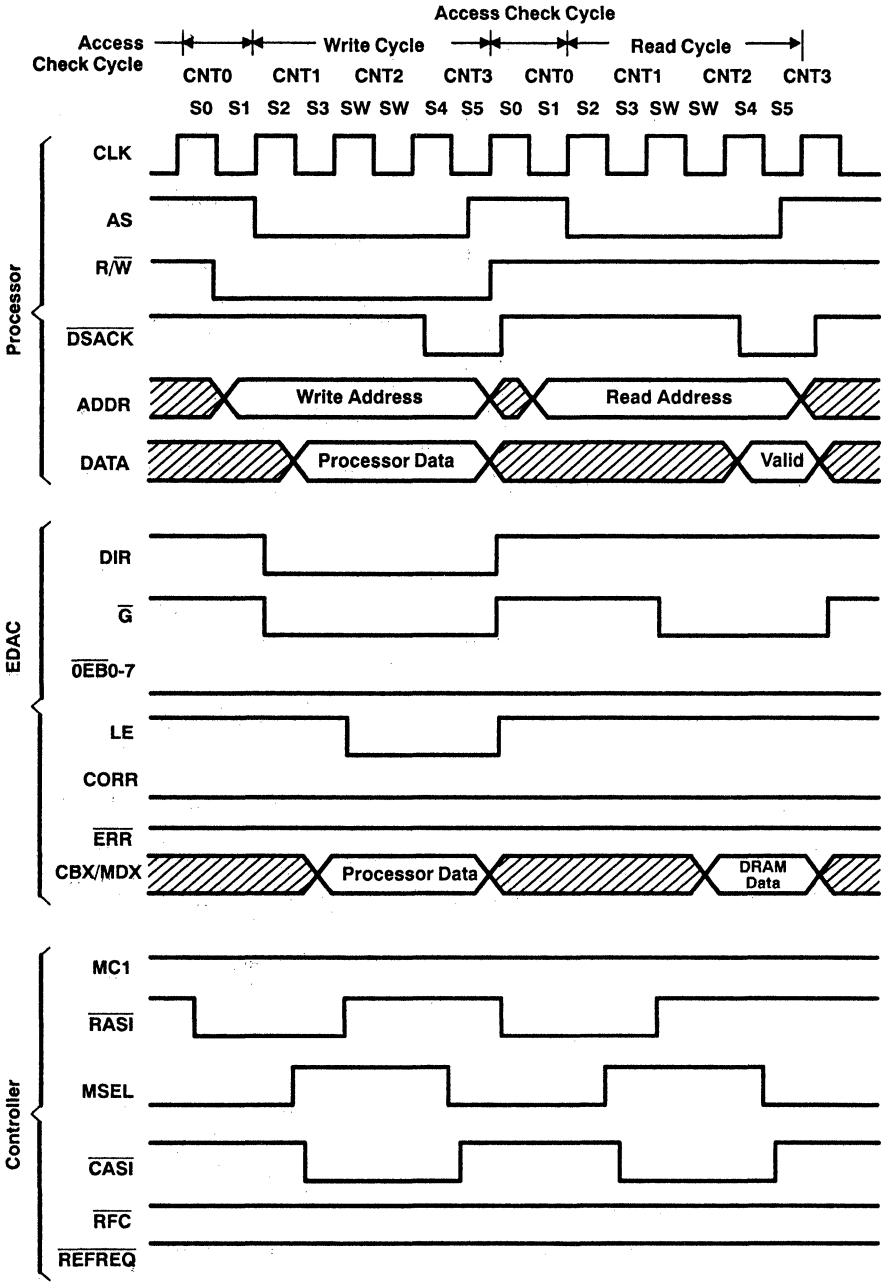


Figure 13. Normal Read and Write Cycle

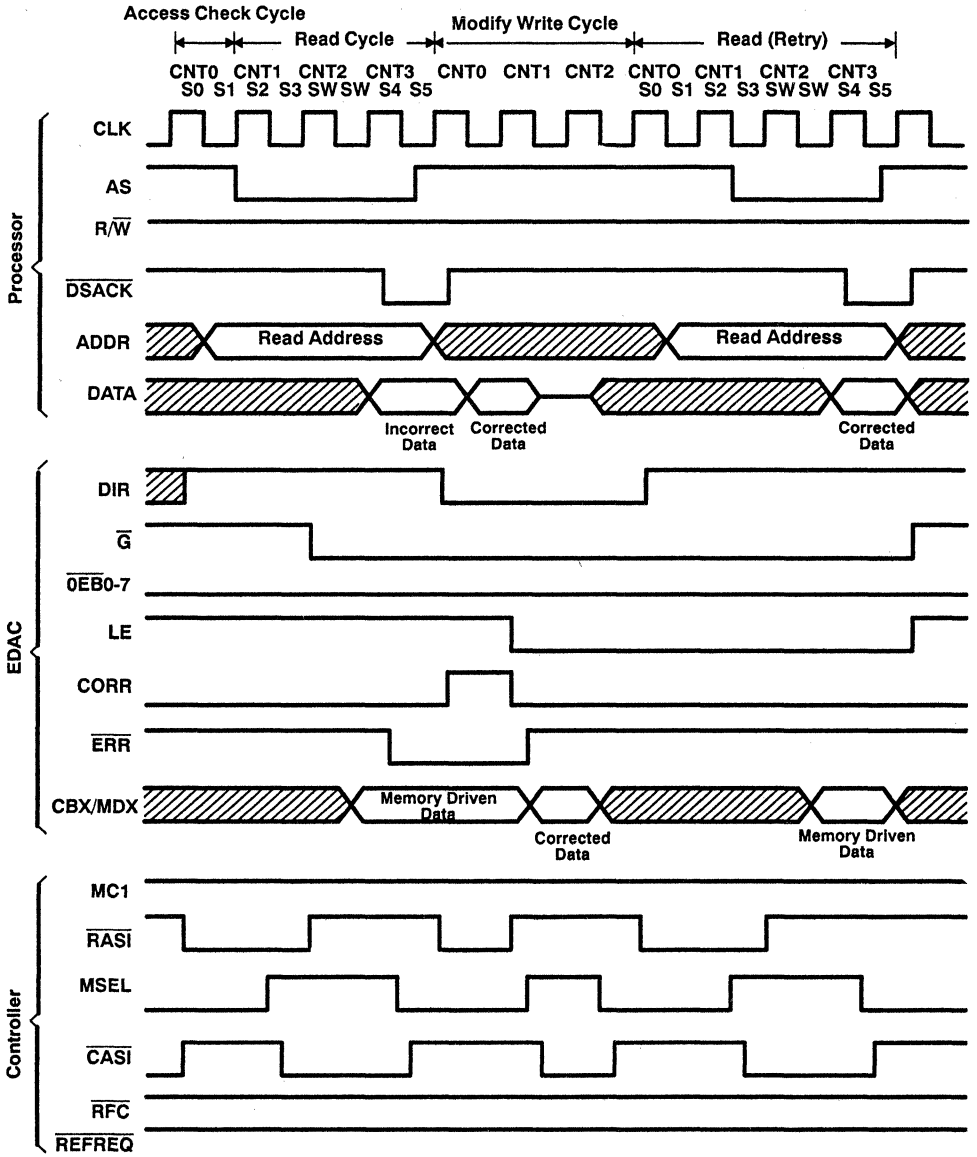


Figure 14. Read and Correct Cycle

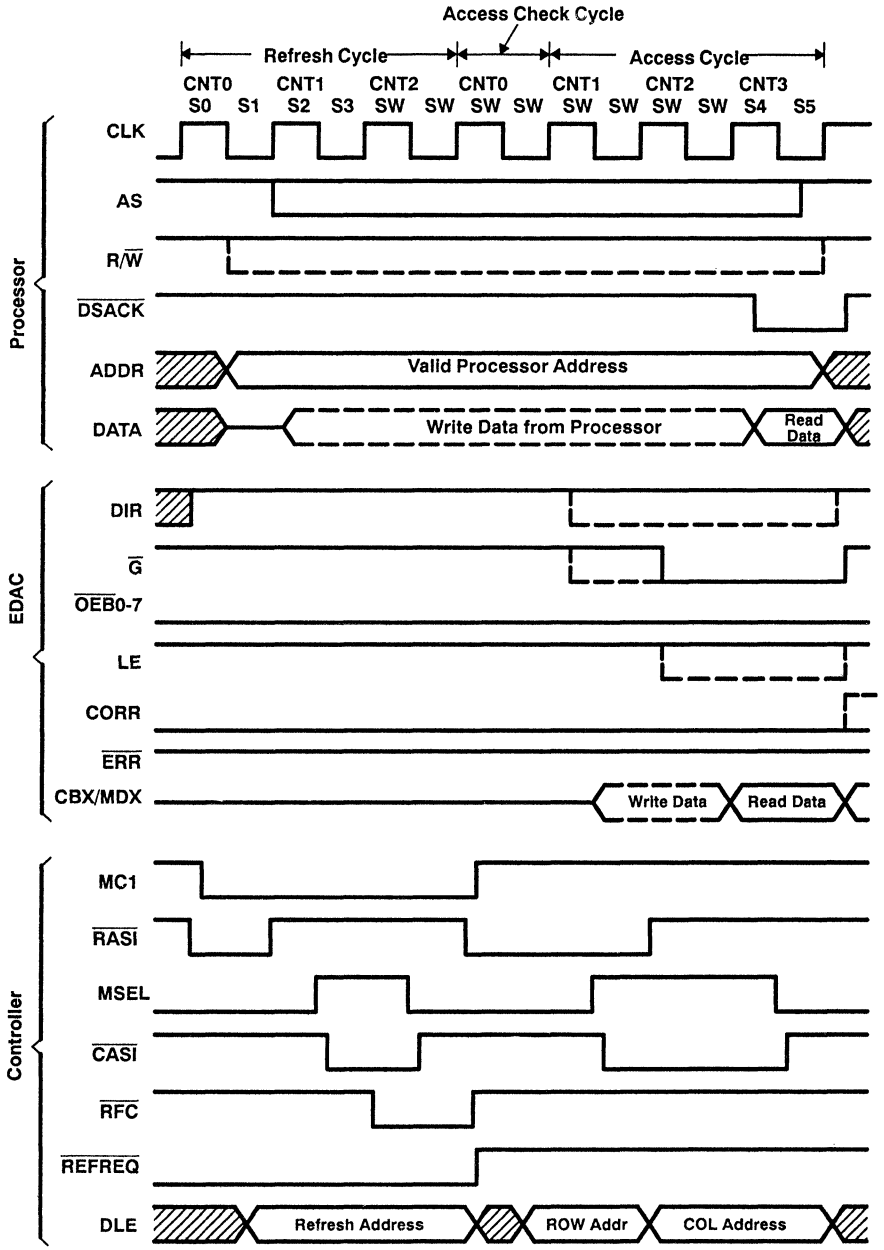


Figure 15. Refresh and Access Cycle

```
Module _EDACCA
title 'FLOW_THRU EDAC MEMORY CONTROLLER FOR CORRECT ALWAYS MODE,
      BERTRAND LEIGH, TEXAS INSTRUMENTS, JANUARY 11, 1990'

   EDACCA device 'F507';

" Input pin assignments

  CLK      pin  1;    " CLOCK INPUT
  RST_     pin  2;    " ACTIVE LOW SYSTEM RESET
  AS       pin  3;    " ADDRESS STROBE FROM PROCESSOR
  IOM_     pin  4;    " IO/MEMORY SPACE INDICATOR
  REFREQ_  pin  5;    " REFRESH REQUEST
  RW_      pin  6;    " READ/WRITE SIGNAL
  ERR_     pin  7;    " ERROR FLAG FROM EDAC

" Output pin and node assignments

  ELE    pin  8;  ELE_R    node 47;  " EDAC'S LATCH ENABLE
  G_     pin  9;  G_R      node 48;  " EDAC'S OUTPUT ENABLE
  DIR    pin 10;  DIR_R    node 49;  " DIRECTION CONTROL
  DLE    pin 11;  DLE_R    node 50;  " DMC'S LATCH ENABLE
  MC1    pin 13;  MC1_R    node 51;  " DMC'S MODE CONTROL
  RASI_  pin 14;  RASI_R   node 52;  " RAS INPUT TO DMC
  RFC_   pin 15;  RFC_R    node 53;  " REFRESH COMPLETE
  DSACK_ pin 16;  DSACK_R  node 54;  " DATA ACKNOWLEDGE

" Internal counter bits & control, and state reg - node declarations

  C0       node 55;                        " INTERNAL COUNTER BIT
  C1       node 56;                        " INTERNAL COUNTER BIT
  C2       node 57;                        " INTERNAL COUNTER BIT
  SCLR0    node 25;                        " SYNC. CLEAR COUNTER CONTROL
  CNTHOLD1 node 29;  CNTHOLD1_R  node 30;  " COUNT/HOLD CONTROL REGISTER
  P0       node 31;  P0_R        node 39;  " BURIED STATE REGISTER
  P1       node 32;  P1_R        node 40;  " BURIED STATE REGISTER
  P2       node 33;  P2_R        node 41;  " BURIED STATE REGISTER
  ASCHK    node 34;  ASCHK_R     node 42;  " INTERNAL AS REGISTER

" Set and reset definition for registers

  ELEX     = [ELE, ELE_R];
  GX_      = [G_, G_R];
  DIRX     = [DIR, DIR_R];
  DLEX     = [DLE, DLE_R];
  MC1X     = [MC1, MC1_R];
  RASIX_   = [RASI_, RASI_R];
  RFCX_    = [RFC_, RFC_R];
  DSACKX_  = [DSACK_, DSACK_R];
  ASCHKX   = [ASCHK, ASCHK_R];

" Intermediate declarations for simplification.

  HIGH      = [ 1,  0];
  LOW       = [ 0,  1];
  COUNT     = [C2,C1,C0];
  STATE_    = [P2,P1,P0];   " STATE REGISTER SET DEFINED
  H,L,C,X = 1, 0, .C., .X.;

" Intermediate state declarations
```

```
  IDLE       = ^B000;    " SAME AS INITIALIZE STATE
  ACCESS_CHK = ^B001;
  WRITE      = ^B010;
  READ       = ^B011;
  CORRECT    = ^B100;
  REFRESH    = ^B101;
  RAS_DLY    = ^B110;

equations

" Initialization when RST_ is low

   [DSACK_,MC1,RFC_,RASI_,G_,DLE,ELE,DIR]    :=  !RST_;
   [P0_R,P1_R,P2_R,ASCHK_R]                  :=  !RST_;

" Counter controls defined

  SCLR0 =  !RST_
         # (STATE_==ACCESS_CHK) & ((IOM_ & REFREQ_) # !REFREQ_)
         # (STATE_==WRITE) & (COUNT==3)
         # (STATE_==READ) & (COUNT==3)
         # (STATE_==CORRECT) & (COUNT==2)
         # (STATE_==REFRESH) & (COUNT==2)
         # (STATE_==IDLE)
         # (STATE_==RAS_DLY);


" State definition

state_diagram STATE_
     State IDLE:      ASCHKX:= HIGH & AS;
                      if RST_ then RAS_DLY;

     State RAS_DLY:    MC1X     := LOW & !REFREQ_ & RST_;
                       RASIX_   := LOW & ((AS # ASCHK) & REFREQ_ # !REFREQ_)
                                   & RST_;
                       ASCHKX   := LOW & ASCHK;
                       if AS & REFREQ_ & RST_    then  ACCESS_CHK
                         else
                       if !REFREQ_ & RST_        then  REFRESH
                         else
                       IDLE;

     State ACCESS_CHK: DIRX    := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       GX_     := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & IOM_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & !REFREQ_ & RST_;
                       if !IOM_ & !RW_ & REFREQ_ & RST_  then  WRITE
                         else
                       if !IOM_ &  RW_ & REFREQ_ & RST_  then  READ
                         else
                       if (!REFREQ_ # IOM_ & REFREQ_) & RST_ then IDLE
                         else
                          IDLE;

     State WRITE:      ELEX   := (COUNT==1) & LOW & RST_;
                       RASIX_ := (COUNT==1) & HIGH & RST_;
                       DSACKX_:= (COUNT==2) & LOW & RST_;
                       DSACKX_:= (COUNT==3) & HIGH & RST_;
```

```
                    ELEX   := (COUNT==3) & HIGH & RST_;
                    GX_    := (COUNT==3) & HIGH & RST_;
                    RASIX_ := (COUNT==3) & LOW & RST_;
                    DIRX   := (COUNT==3) & HIGH & RST_;
                    case
                        (COUNT==3) & RST_        : ACCESS_CHK;
                    endcase;

    State READ:   GX_    := (COUNT==1) & LOW & RST_;
                  RASIX_ := (COUNT==1) & HIGH & RST_;
                  DLEX   := (COUNT==1) & LOW & RST_;
                  DSACKX_:= (COUNT==2) & LOW & RST_;
                  DSACKX_:= (COUNT==3) & HIGH & RST_;
                  GX_    := (COUNT==3) & HIGH & RST_;
                  DLEX   := (COUNT==3) & HIGH & ERR_ & RST_;
                  RASIX_ := (COUNT==3) & LOW & RST_;
                  ELEX   := (COUNT==3) & LOW & !ERR_ & RST_;
                  case
                      (COUNT==3) & ERR_ & RST_      : ACCESS_CHK;
                      (COUNT==3) & !ERR_ & RST_     : CORRECT;
                  endcase;

    State CORRECT:  DIRX    := (COUNT==0) & LOW & RST_;
                    GX_     := (COUNT==0) & LOW & RST_;
                    RASIX_  := (COUNT==0) & HIGH & RST_;
                    GX_     := (COUNT==2) & HIGH & RST_;
                    ELEX    := (COUNT==2) & HIGH & RST_;
                    DLEX    := (COUNT==2) & HIGH & RST_;
                    RASIX_  := (COUNT==2) & LOW & RST_;
                    MC1X    := (COUNT==2) & LOW & !REFREQ_ & RST_;
                    DIRX    := (COUNT==2) & HIGH & RST_;
                    case
                        (COUNT==2) & REFREQ_ & RST_    : ACCESS_CHK;
                        (COUNT==2) & !REFREQ_ & RST_   : REFRESH;
                    endcase;

    State REFRESH:  RASIX_  := (COUNT==0) & HIGH & RST_;
                    RFCX_   := (COUNT==1) & LOW & RST_;
                    MC1X    := (COUNT==2) & HIGH & RST_;
                    RASIX_  := (COUNT==2) & LOW & RST_;
                    RFCX_   := (COUNT==2) & HIGH & RST_;
                    case
                        (COUNT==2)             :ACCESS_CHK;
                    endcase;

test_vectors ' REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  L , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H , H ,  H  , H  ,   H  ,  IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H , H ,  H  , H  ,   H  , RAS_DLY  ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H , L ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H , L ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , H, H , H , L ,  H  , L  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , H, H , H , H ,  L  , H  ,   H  ,ACCESS_CHK];
 [ C ,  H , X,  H ,   H   , X ,  X ,  0  ] -> [ H , H, H , H , H ,  H  , H  ,   H  ,  IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H , H ,  H  , H  ,   H  , RAS_DLY  ];
 [ C ,  H , H,  X ,   H   , X ,  X ,  0  ] -> [ H , H, H , H , H ,  L  , H  ,   H  ,ACCESS_CHK];
test_vectors ' WRITE SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  L ,   H   , L ,  X ,  0  ] -> [ H , L, L , H , H ,  L  , H  ,   H  ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ L , L, L , H , H ,  H  , H  ,   H  ,  WRITE   ];
```

```
 [ C , H , X, X ,  X  , X , X ,  2 ] -> [ L , L, L , H , H ,  H  , H  ,  L  , WRITE   ];
 [ C , H , X, X ,  X  , X , X ,  3 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X, L ,  H  , H , X ,  0 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ H , L, H , L , H ,  H  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  2 ] -> [ H , L, H , L , H ,  H  , H  ,  L  ,  READ   ];
 [ C , H , X, X ,  X  , X , H ,  3 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ, CORRECT & ACCESS SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X, L ,  H  , H , X ,  0 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ H , L, H , L , H ,  H  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  2 ] -> [ H , L, H , L , H ,  H  , H  ,  L  ,  READ   ];
 [ C , H , X, X ,  X  , X , L ,  3 ] -> [ L , H, H , L , H ,  L  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  X  , X , X ,  0 ] -> [ L , L, L , L , H ,  H  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ L , L, L , L , H ,  H  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  H  , X , X ,  2 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ, CORRECT & REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X, L ,  H  , H , X ,  0 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ H , L, H , L , H ,  H  , H  ,  H  ,  READ   ];
 [ C , H , X, X ,  X  , X , X ,  2 ] -> [ H , L, H , L , H ,  H  , H  ,  L  ,  READ   ];
 [ C , H , X, X ,  X  , X , L ,  3 ] -> [ L , H, H , L , H ,  L  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  X  , X , X ,  0 ] -> [ L , L, L , L , H ,  H  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ L , L, L , L , H ,  H  , H  ,  H  ,  CORRECT ];
 [ C , H , X, X ,  L  , X , X ,  2 ] -> [ H , H, H , H , L ,  L  , H  ,  H  ,  REFRESH ];
 [ C , H , X, X ,  X  , X , X ,  0 ] -> [ H , H, H , H , L ,  H  , H  ,  H  ,  REFRESH ];
 [ C , H , X, X ,  X  , X , X ,  1 ] -> [ H , H, H , H , L ,  H  , L  ,  H  ,  REFRESH ];
 [ C , H , X, X ,  X  , X , X ,  2 ] -> [ H , H, H , H , H ,  L  , H  ,  H  ,ACCESS_CHK];
 [ C , H , X, X ,  L  , X , X ,  0 ] -> [ H , H, H , H , H ,  H  , H  ,  H  ,  IDLE   ];
 [ C , H , X, X ,  L  , X , X ,  0 ] -> [ H , H, H , H , H ,  H  , H  ,  H  ,  RAS_DLY ];
 [ C , H , X, X ,  L  , X , X ,  0 ] -> [ H , H, H , H , L ,  L  , H  ,  H  ,  REFRESH ];

 end _EDACCA
```

```
Module _EDACMS1
title 'FLOW_THRU EDAC MEMORY CONTROLLER FOR CORRECT ALWAYS MODE
      WITH MEMORY SCRUBBING, DEVICE #1
      BERTRAND LEIGH, TEXAS INSTRUMENTS, JANUARY 26, 1990'

  EDACMS1 device 'F507';

" Input pin assignments

  CLK      pin  1;    " CLOCK INPUT
  RST_     pin  2;    " ACTIVE LOW SYSTEM RESET
  AS       pin  3;    " ADDRESS STROBE FROM PROCESSOR
  IOM      pin  4;    " IO/MEMORY SPACE INDICATOR
  REFREQ_  pin  5;    " REFRESH REQUEST
  RW_      pin  6;    " READ/WRITE SIGNAL
  ERR_     pin  7;    " ERROR FLAG FROM EDAC

" Output pin and node assignments

  ELE    pin  8;  ELE_R    node 47;  " EDAC'S LATCH ENABLE
  G_     pin  9;  G_R      node 48;  " EDAC'S OUTPUT ENABLE
  DIR    pin 10;  DIR_R    node 49;  " DIRECTION CONTROL
  DLE    pin 11;  DLE_R    node 50;  " DMC'S LATCH ENABLE
  RASI_  pin 14;  RASI_R   node 52;  " RAS INPUT TO DMC
  RFC_   pin 15;  RFC_R    node 53;  " REFRESH COMPLETE
  DSACK_ pin 16;  DSACK_R  node 54;  " DATA ACKNOWLEDGE

" Internal counter bits & control, and state reg - node declarations

  C0       node 55;                        " INTERNAL COUNTER BIT
  C1       node 56;                        " INTERNAL COUNTER BIT
  C2       node 57;                        " INTERNAL COUNTER BIT
  SCLR0    node 25;                        " SYNC. CLEAR COUNTER CONTROL
  CNTHOLD1 node 29;  CNTHOLD1_R  node 30;  " COUNT/HOLD CONTROL REGISTER
  P0       node 31;  P0_R        node 39;  " BURIED STATE REGISTER
  P1       node 32;  P1_R        node 40;  " BURIED STATE REGISTER
  P2       node 33;  P2_R        node 41;  " BURIED STATE REGISTER
  ASCHK    node 34;  ASCHK_R     node 42;  " INTERNAL AS REGISTER

" Set and reset definition for registers

  ELEX     = [ELE, ELE_R];
  GX_      = [G_, G_R];
  DIRX     = [DIR, DIR_R];
  DLEX     = [DLE, DLE_R];
  RASIX_   = [RASI_, RASI_R];
  RFCX_    = [RFC_, RFC_R];
  DSACKX_  = [DSACK_, DSACK_R];
  ASCHKX   = [ASCHK, ASCHK_R];

" Intermediate declarations for simplification.

  HIGH      = [ 1,  0];
  LOW       = [ 0,  1];
  COUNT     = [C2,C1,C0];
  STATE_    = [P2,P1,P0];   " STATE REGISTER SET DEFINED
  H,L,C,X = 1, 0, .C., .X.;

" Intermediate state declarations
```

```
  IDLE       = ^B000;    " SAME AS INITIALIZE STATE
  ACCESS_CHK = ^B001;
  WRITE      = ^B010;
  READ       = ^B011;
  CORRECT    = ^B100;
  REFRESH    = ^B101;
  RAS_DLY    = ^B110;

equations

" Initialization when RST_ is low

   [DSACK_,RFC_,RASI_,G_,DLE,ELE,DIR]        :=  !RST_;
   [P0_R,P1_R,P2_R,ASCHK_R]                  :=  !RST_;

" Counter controls defined

  SCLR0 =  !RST_
        # (STATE_==ACCESS_CHK) & IOM_
        # (STATE_==ACCESS_CHK) & !REFREQ_
        # (STATE_==WRITE) & (COUNT==3)
        # (STATE_==READ) & (COUNT==3)
        # (STATE_==CORRECT) & (COUNT==2)
        # (STATE_==REFRESH) & (COUNT==5)
        # (STATE_==IDLE)
        # (STATE_==RAS_DLY);


" State definition

state_diagram STATE_
     State IDLE:      ASCHKX := HIGH & AS;
                      if RST_ then RAS_DLY;

     State RAS_DLY:   RASIX_   := LOW & ((AS # ASCHK) & REFREQ_ # !REFREQ_)
                                  & RST_;
                      ASCHKX   := LOW & ASCHK;
                      if  AS & REFREQ_ & RST_    then  ACCESS_CHK
                        else
                      if  !REFREQ_ & RST_        then  REFRESH
                        else
                      IDLE;

     State ACCESS_CHK: DIRX    := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       GX_     := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & IOM_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & !REFREQ_ & RST_;
                       if !IOM_ & !RW_ & REFREQ_ & RST_  then  WRITE
                         else
                       if !IOM_ &  RW_ & REFREQ_ & RST_  then  READ
                         else
                       if (!REFREQ_ # IOM_ & REFREQ_) & RST_ then IDLE
                         else
                          IDLE;

     State WRITE:      ELEX   := (COUNT==1) & LOW & RST_;
                       RASIX_ := (COUNT==1) & HIGH & RST_;
                       DSACKX_:= (COUNT==2) & LOW & RST_;
                       DSACKX_:= (COUNT==3) & HIGH & RST_;
                       ELEX   := (COUNT==3) & HIGH & RST_;
```

```
                    GX_    := (COUNT==3) & HIGH & RST_;
                    RASIX_ := (COUNT==3) & LOW & RST_;
                    DIRX   := (COUNT==3) & HIGH & RST_;
                    case
                        (COUNT==3) & RST_        : ACCESS_CHK;
                    endcase;

    State READ:   GX_    := (COUNT==1) & LOW & RST_;
                  RASIX_ := (COUNT==1) & HIGH & RST_;
                  DLEX   := (COUNT==1) & LOW & RST_;
                  DSACKX_:= (COUNT==2) & LOW & RST_;
                  DSACKX_:= (COUNT==3) & HIGH & RST_;
                  GX_    := (COUNT==3) & HIGH & RST_;
                  DLEX   := (COUNT==3) & HIGH & ERR_ & RST_;
                  RASIX_ := (COUNT==3) & LOW & RST_;
                  ELEX   := (COUNT==3) & LOW & !ERR_ & RST_;
                  case
                      (COUNT==3) & ERR_ & RST_      : ACCESS_CHK;
                      (COUNT==3) & !ERR_ & RST_     : CORRECT;
                  endcase;

    State CORRECT:  DIRX   := (COUNT==0) & LOW & RST_;
                    GX_    := (COUNT==0) & LOW & RST_;
                    RASIX_ := (COUNT==0) & HIGH & RST_;
                    GX_    := (COUNT==2) & HIGH & RST_;
                    ELEX   := (COUNT==2) & HIGH & RST_;
                    DLEX   := (COUNT==2) & HIGH & RST_;
                    RASIX_ := (COUNT==2) & LOW & RST_;
                    DIRX   := (COUNT==2) & HIGH & RST_;
                    case
                        (COUNT==2) & REFREQ_ & RST_    : ACCESS_CHK;
                        (COUNT==2) & !REFREQ_ & RST_   : REFRESH;
                    endcase;

    State REFRESH:  RFCX_  := (COUNT==1) & LOW & RST_;
                    RFCX_  := (COUNT==2) & HIGH & RST_;
                    DIRX   := (COUNT==3) & LOW & !ERR_ & RST_;
                    RASIX_ := (COUNT==3) & HIGH & RST_;
                    DIRX   := (COUNT==4) & HIGH & RST_;
                    RASIX_ := (COUNT==5) & LOW & RST_;
                    case
                        (COUNT==5)              :ACCESS_CHK;
                    endcase;

test_vectors ' REFRESH SEQUENCE WITH ERROR '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  L , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,   IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  , RAS_DLY  ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , H, H , H ,  L  , L  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [ H , H, L , H ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [ H , H, H , H ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
 [ C ,  H , X,  H ,   H   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,   IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  , RAS_DLY  ];
 [ C ,  H , H,  X ,   H   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,    IDLE   ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,  RAS_DLY  ];
```

```
test_vectors ' REFRESH SEQUENCE WITHOUT ERROR '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , H, H , H ,  L  , L  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , H, H , H ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  H ,  3  ] -> [ H , H, H , H ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [ H , H, H , H ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
test_vectors ' WRITE SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  L ,   H   , L ,  X ,  0  ] -> [ H , L, L , H ,  L  , H  ,   H  ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ L , L, L , H ,  H  , H  ,   H  ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ L , L, L , H ,  H  , H  ,   L  ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  3  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
test_vectors ' READ SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , L, H , L ,  H  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , L, H , L ,  H  , H  ,   L  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  H ,  3  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
test_vectors ' READ, CORRECT & ACCESS SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , L, H , L ,  H  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , L, H , L ,  H  , H  ,   L  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [ L , H, H , L ,  L  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ L , L, L , L ,  H  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ L , L, L , L ,  H  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   H   , X ,  X ,  2  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
test_vectors ' READ, CORRECT & REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [ELE,G_,DIR,DLE,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , L, H , L ,  H  , H  ,   H  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , L, H , L ,  H  , H  ,   L  ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [ L , H, H , L ,  L  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ L , L, L , L ,  H  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ L , L, L , L ,  H  , H  ,   H  ,  CORRECT ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  2  ] -> [ H , H, H , H ,  L  , H  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H , H, H , H ,  L  , L  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [ H , H, H , H ,  L  , H  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [ H , H, L , H ,  H  , H  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [ H , H, H , H ,  H  , H  ,   H  ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [ H , H, H , H ,  L  , H  ,   H  ,ACCESS_CHK];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,   IDLE   ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  H  , H  ,   H  ,  RAS_DLY ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H , H, H , H ,  L  , H  ,   H  ,  REFRESH ];

 end _EDACMS1
```

```
Module _EDACMS2
title 'FLOW_THRU EDAC MEMORY CONTROLLER FOR CORRECT ALWAYS MODE
      WITH MEMORY SCRUBBING, DEVICE #2
      BERTRAND LEIGH, TEXAS INSTRUMENTS, JANUARY 26, 1990'

   EDACMS2 device 'F507';

" Input pin assignments

  CLK      pin  1;    " CLOCK INPUT
  RST_     pin  2;    " ACTIVE LOW SYSTEM RESET
  AS       pin  3;    " ADDRESS STROBE FROM PROCESSOR
  IOM_     pin  4;    " IO/MEMORY SPACE INDICATOR
  REFREQ_  pin  5;    " REFRESH REQUEST
  RW_      pin  6;    " READ/WRITE SIGNAL
  ERR_     pin  7;    " ERROR FLAG FROM EDAC

" Output pin and node assignments

  SDIR   pin  8;  SDIR_R   node 47;  " SCRUBBING EDAC'S DIRECTION CONTROL
  SLE    pin  9;  SLE_R    node 48;  " SCRUBBING EDAC'S LATCH ENABLE
  SG_    pin 10;  SG_R     node 49;  " SCRUBBING EDAC'S OUTPUT ENABLE
  MC0    pin 11;  MC0_R    node 50;  " DMC'S MODE CONTROL 0
  MC1    pin 14;  MC1_R    node 52;  " DMC'S MODE CONTROL 1

" Internal counter bits & control, and state reg - node declarations

  C0       node 55;                        " INTERNAL COUNTER BIT
  C1       node 56;                        " INTERNAL COUNTER BIT
  C2       node 57;                        " INTERNAL COUNTER BIT
  SCLR0    node 25;                        " SYNC. CLEAR COUNTER CONTROL
  CNTHOLD1 node 29;  CNTHOLD1_R  node 30; " COUNT/HOLD CONTROL REGISTER
  P0       node 31;  P0_R        node 39; " BURIED STATE REGISTER
  P1       node 32;  P1_R        node 40; " BURIED STATE REGISTER
  P2       node 33;  P2_R        node 41; " BURIED STATE REGISTER
  ASCHK    node 34;  ASCHK_R     node 42; " INTERNAL AS REGISTER

" Set and reset definition for registers

  SDIRX    = [SDIR, SDIR_R];
  SLEX     = [SLE, SLE_R];
  SGX_     = [SG_, SG_R];
  MC0X     = [MC0, MC0_R];
  MC1X     = [MC1, MC1_R];
  ASCHKX   = [ASCHK, ASCHK_R];

" Intermediate declarations for simplification.

  HIGH     = [ 1,  0];
  LOW      = [ 0,  1];
  COUNT    = [C2,C1,C0];
  STATE_   = [P2,P1,P0];   " STATE REGISTER SET DEFINED
  H,L,C,X = 1, 0, .C., .X.;

" Intermediate state declarations

  IDLE       = ^B000;    " SAME AS INITIALIZE STATE
  ACCESS_CHK = ^B001;
  WRITE      = ^B010;
  READ       = ^B011;
```

```
  CORRECT    = ^B100;
  REFRESH    = ^B101;
  RAS_DLY    = ^B110;

equations

" Initialization when RST_ is low

   [MC1,SLE,SG_]                          :=  !RST_;
   [P0_R,P1_R,P2_R,SDIR_R,ASCHK_R]        :=  !RST_;

" Counter controls defined

  SCLR0 =  !RST_
        # (STATE_==ACCESS_CHK) & IOM_
        # (STATE_==ACCESS_CHK) & !REFREQ_
        # (STATE_==WRITE) & (COUNT==3)
        # (STATE_==READ) & (COUNT==3)
        # (STATE_==CORRECT) & (COUNT==2)
        # (STATE_==REFRESH) & (COUNT==5)
        # (STATE_==IDLE)
        # (STATE_==RAS_DLY);

" State definition

state_diagram STATE_
     State IDLE:      ASCHKX := HIGH & AS;
                      if RST_ then RAS_DLY;

     State RAS_DLY:    MC0X     := HIGH & !REFREQ_ & RST_;
                       MC1X     := LOW & !REFREQ_ & RST_;
                       SDIRX    := HIGH & !REFREQ_ & RST_;
                       SGX_     := LOW & !REFREQ_ & RST_;
                       ASCHKX   := LOW & ASCHK;
                       if  AS & REFREQ_ & RST_    then  ACCESS_CHK
                         else
                       if  !REFREQ_ & RST_        then  REFRESH
                         else
                       IDLE;

     State ACCESS_CHK:
                       if !IOM_ & !RW_ & REFREQ_ & RST_  then  WRITE
                         else
                       if !IOM_ &  RW_ & REFREQ_ & RST_  then  READ
                         else
                       if (!REFREQ_ # IOM_ & REFREQ_) & RST_ then IDLE
                         else
                          IDLE;

     State WRITE:      case
                           (COUNT==3) & RST_         : ACCESS_CHK;
                       endcase;

     State READ:   case
                       (COUNT==3) & ERR_ & RST_      : ACCESS_CHK;
                       (COUNT==3) & !ERR_ & RST_     : CORRECT;
                   endcase;

     State CORRECT:  MC0X    := (COUNT==2) & HIGH & !REFREQ_ & RST_;
                     MC1X    := (COUNT==2) & LOW & !REFREQ_ & RST_;
```

```
                SDIRX   := (COUNT==2) & HIGH & !REFREQ_ & RST_;
                SGX_    := (COUNT==2) & LOW & !REFREQ_ & RST_;
                case
                    (COUNT==2) & REFREQ_ & RST_     : ACCESS_CHK;
                    (COUNT==2) & !REFREQ_ & RST_    : REFRESH;
                endcase;

   State REFRESH: MC0X    := (COUNT==5) & LOW & RST_;
                  MC1X    := (COUNT==5) & HIGH & RST_;
                  SDIRX   := (COUNT==3) & LOW & !ERR_ & RST_;
                  SLEX    := (COUNT==3) & LOW & !ERR_ & RST_;
                  SLEX    := (COUNT==5) & HIGH & RST_;
                  SGX     := (COUNT==5) & HIGH & RST_;
                  SDIRX   := (COUNT==5) & LOW & RST_;
                  case
                      (COUNT==5)                :ACCESS_CHK;
                  endcase;

test_vectors ' REFRESH SEQUENCE WITH ERROR '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  L , X,  X ,   X   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  L , H , H , L , H , RAS_DLY  ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [  L , L , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [  L , L , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [  L , H , H , L , H ,ACCESS_CHK];
 [ C ,  H , X,  H ,   H   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  IDLE    ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  L , H , H , L , H , RAS_DLY  ];
 [ C ,  H , H,  X ,   H   , X ,  X ,  0  ] -> [  L , H , H , L , H ,ACCESS_CHK];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  IDLE    ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  L , H , H , L , H , RAS_DLY  ];
test_vectors ' REFRESH SEQUENCE WITHOUT ERROR '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  H ,  3  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [  H , H , L , H , L , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [  L , H , H , L , H ,ACCESS_CHK];
test_vectors ' WRITE SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  H , X,  L ,   H   , L ,  X ,  0  ] -> [  L , H , H , L , H ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  L , H , H , L , H ,  WRITE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  3  ] -> [  L , H , H , L , H ,ACCESS_CHK];
test_vectors ' READ SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  H ,  3  ] -> [  L , H , H , L , H ,ACCESS_CHK];
test_vectors ' READ, CORRECT & ACCESS SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  L , H , H , L , H ,   READ   ];
```

```
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   H   , X ,  X ,  2  ] -> [  L , H , H , L , H ,ACCESS_CHK];
test_vectors ' READ, CORRECT & REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [SDIR,SLE,SG_,MC0,MC1,  STATE_  ])
 [ C ,  H , X,  L ,   H   , H ,  X ,  0  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  L , H , H , L , H ,   READ   ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  L , H , H , L , H ,  CORRECT ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  2  ] -> [  H , H , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [  H , H , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [  H , H , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  2  ] -> [  H , H , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  L ,  3  ] -> [  L , L , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  4  ] -> [  L , L , L , H , L ,  REFRESH ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  5  ] -> [  L , H , H , L , H ,ACCESS_CHK];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  L , H , H , L , H ,   IDLE   ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  L , H , H , L , H ,  RAS_DLY ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [  H , H , L , H , L ,  REFRESH ];

 end _EDACMS2
```

```
Module _EDACCOE
title 'FLOW_THRU EDAC MEMORY CONTROLLER FOR CORRECT ONLY ON ERROR MODE,
      BERTRAND LEIGH, TEXAS INSTRUMENTS, JANUARY 30, 1990'

   EDACCOE  device 'F507';

" Input pin assignments

  CLK      pin  1;    " CLOCK INPUT
  RST_     pin  2;    " ACTIVE LOW SYSTEM RESET
  AS       pin  3;    " ADDRESS STROBE FROM PROCESSOR
  IOM_     pin  4;    " IO/MEMORY SPACE INDICATOR
  REFREQ_  pin  5;    " REFRESH REQUEST
  RW_      pin  6;    " READ/WRITE SIGNAL
  ERR_     pin  7;    " ERROR FLAG FROM EDAC

" Output pin and node assignments

  LE     pin  8;  LE_R     node 47;  " EDAC'S LATCH ENABLE
  G_     pin  9;  G_R      node 48;  " EDAC'S OUTPUT ENABLE
  DIR    pin 10;  DIR_R    node 49;  " DIRECTION CONTROL
  CORR   pin 11;  CORR_R   node 50;  " EDAC'S CORRECT CONTROL
  MC1    pin 13;  MC1_R    node 51;  " DMC'S MODE CONTROL
  RASI_  pin 14;  RASI_R   node 52;  " RAS INPUT TO DMC
  RFC_   pin 15;  RFC_R    node 53;  " REFRESH COMPLETE
  DSACK_ pin 16;  DSACK_R  node 54;  " DATA ACKNOWLEDGE

" Internal counter bits & control, and state reg - node declarations

  C0       node 55;                        " INTERNAL COUNTER BIT
  C1       node 56;                        " INTERNAL COUNTER BIT
  C2       node 57;                        " INTERNAL COUNTER BIT
  SCLR0    node 25;                        " SYNC. CLEAR COUNTER CONTROL
  P0       node 31;  P0_R       node 39;  " BURIED STATE REGISTER
  P1       node 32;  P1_R       node 40;  " BURIED STATE REGISTER
  P2       node 33;  P2_R       node 41;  " BURIED STATE REGISTER
  ASCHK    node 34;  ASCHK_R    node 42;  " INTERNAL AS REGISTER

" Set and reset definition for registers

  LEX      = [LE, LE_R];
  GX_      = [G_, G_R];
  DIRX     = [DIR, DIR_R];
  CORRX    = [CORR, CORR_R];
  MC1X     = [MC1, MC1_R];
  RASIX_   = [RASI_, RASI_R];
  RFCX_    = [RFC_, RFC_R];
  DSACKX_  = [DSACK_, DSACK_R];
  ASCHKX   = [ASCHK, ASCHK_R];


" Intermediate declarations for simplification.

  HIGH     = [ 1,  0];
  LOW      = [ 0,  1];
  COUNT    = [C2,C1,C0];
  STATE_   = [P2,P1,P0];   " STATE REGISTER SET DEFINED
  H,L,C,X = 1, 0, .C., .X.;

" Intermediate state declarations
```

```
  IDLE       = ^B000;    " SAME AS INITIALIZE STATE
  ACCESS_CHK = ^B001;
  WRITE      = ^B010;
  READ       = ^B011;
  MOD_WRITE  = ^B100;
  REFRESH    = ^B101;
  RETRY      = ^B110;
  RAS_DLY    = ^B111;

equations

" Initialization when RST_ is low

   [DSACK_,MC1,RFC_,RASI_,G_,LE,DIR]            :=  !RST_;
   [P0_R,P1_R,P2_R,CORR_R,ASCHK_R]              :=  !RST_;

" Counter controls defined

  SCLR0 =  !RST_
         # (STATE_==ACCESS_CHK) & IOM_
         # (STATE_==ACCESS_CHK) & !REFREQ_
         # (STATE_==WRITE) & (COUNT==3)
         # (STATE_==READ) & (COUNT==3)
         # (STATE_==MOD_WRITE) & (COUNT==2)
         # (STATE_==REFRESH) & (COUNT==2)
         # (STATE_==RETRY) & (COUNT==3)
         # (STATE_==RAS_DLY)
         # (STATE_==IDLE);

" State definition

state_diagram STATE_
     State IDLE:       ASCHKX := HIGH & AS;
                       if RST_ then RAS_DLY;

     State RAS_DLY:    MC1X     := LOW & !REFREQ_ & RST_;
                       RASIX_   := LOW & ((AS # ASCHK) & REFREQ_ # !REFREQ_)
                                   & RST_;
                       ASCHKX   := LOW & ASCHK;
                       if (AS # ASCHK) & REFREQ_ & RST_  then ACCESS_CHK
                         else
                       if !REFREQ_ & RST_                then REFRESH
                         else
                       IDLE;

     State ACCESS_CHK: DIRX    := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       GX_     := LOW & !IOM_ & !RW_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & IOM_ & REFREQ_ & RST_;
                       RASIX_  := HIGH & !REFREQ_ & RST_;
                       if !IOM_ & !RW_ & REFREQ_ & RST_  then  WRITE
                         else
                       if !IOM_ &  RW_ & REFREQ_ & RST_  then  READ
                         else
                       if (!REFREQ_ # IOM_ & REFREQ_) & RST_ then IDLE
                         else
                          IDLE;

     State WRITE:      LEX    := (COUNT==1) & LOW & RST_;
                       RASIX_ := (COUNT==1) & HIGH & RST_;
```

```
                    DSACKX_:= (COUNT==2) & LOW & RST_;
                    DSACKX_:= (COUNT==3) & HIGH & RST_;
                    LEX    := (COUNT==3) & HIGH & RST_;
                    GX_    := (COUNT==3) & HIGH & RST_;
                    RASIX_ := (COUNT==3) & LOW & RST_;
                    DIRX   := (COUNT==3) & HIGH & RST_;
                    case
                        (COUNT==3) & RST_        : ACCESS_CHK;
                    endcase;

    State READ:   GX_    := (COUNT==1) & LOW & RST_;
                  RASIX_ := (COUNT==1) & HIGH & RST_;
                  DSACKX_:= (COUNT==2) & LOW & RST_;
                  DSACKX_:= (COUNT==3) & HIGH & RST_;
                  GX_    := (COUNT==3) & HIGH & ERR_ & RST_;
                  RASIX_ := (COUNT==3) & LOW & RST_;
                  CORRX  := (COUNT==3) & HIGH & !ERR_ & RST_;
                  case
                      (COUNT==3) & ERR_ & RST_      : ACCESS_CHK;
                      (COUNT==3) & !ERR_ & RST_     : MOD_WRITE;
                  endcase;

    State MOD_WRITE:  DIRX    := (COUNT==0) & LOW & RST_;
                      RASIX_  := (COUNT==0) & HIGH & RST_;
                      LEX     := (COUNT==0) & LOW & RST_;
                      CORRX   := (COUNT==0) & LOW & RST_;
                      RASIX_  := (COUNT==2) & LOW & RST_;
                      DIRX    := (COUNT==2) & HIGH & !REFREQ_ & RST_;
                      case
                          (COUNT==2) & RST_    : RETRY;
                      endcase;

    State RETRY:    RASIX_   := (COUNT==1) & HIGH & RST_;
                    DSACKX_  := (COUNT==2) & LOW & RST_;
                    DSACKX_  := (COUNT==3) & HIGH & RST_;
                    RASIX_   := (COUNT==3) & LOW & RST_;
                    LEX      := (COUNT==3) & HIGH & RST_;
                    GX_      := (COUNT==3) & HIGH & RST_;
                    MC1X     := (COUNT==3) & LOW & !REFREQ_ & RST_;
                    case
                        (COUNT==3) & REFREQ_ & RST_   : ACCESS_CHK;
                        (COUNT==3) & !REFREQ_ & RST_  : REFRESH;
                    endcase;

    State REFRESH:  RASIX_   := (COUNT==0) & HIGH & RST_;
                    RFCX_    := (COUNT==1) & LOW & RST_;
                    MC1X     := (COUNT==2) & HIGH & RST_;
                    RASIX_   := (COUNT==2) & LOW & RST_;
                    RFCX_    := (COUNT==2) & HIGH & RST_;
                    case
                        (COUNT==2)            : ACCESS_CHK;
                    endcase;

test_vectors ' REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [LE,G_,DIR,CORR,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C ,  L , X,  X ,   X   , X ,  X ,  0  ] -> [ H, H, H ,  L , H ,  H  , H  ,   H  ,  IDLE   ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H, H, H ,  L , H ,  H  , H  ,   H  , RAS_DLY  ];
 [ C ,  H , X,  X ,   L   , X ,  X ,  0  ] -> [ H, H, H ,  L , L ,  L  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  0  ] -> [ H, H, H ,  L , L ,  H  , H  ,   H  , REFRESH  ];
 [ C ,  H , X,  X ,   X   , X ,  X ,  1  ] -> [ H, H, H ,  L , L ,  H  , L  ,   H  , REFRESH  ];
```

```
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
 [ C , H , X,  H ,   H   , X ,  X ,  0 ] -> [ H, H, H ,  L , H ,  H  , H  ,  H  ,  IDLE   ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ H, H, H ,  L , H ,  H  , H  ,  H  , RAS_DLY  ];
 [ C , H , H,  X ,   H   , X ,  X ,  0 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' WRITE SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [LE,G_,DIR,CORR,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X,  L ,   H   , L ,  X ,  0 ] -> [ H, L, L ,  L , H ,  L  , H  ,  H  ,  WRITE   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ L, L, L ,  L , H ,  H  , H  ,  H  ,  WRITE   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ L, L, L ,  L , H ,  H  , H  ,  L  ,  WRITE   ];
 [ C , H , X,  X ,   X   , X ,  X ,  3 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [LE,G_,DIR,CORR,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X,  L ,   H   , H ,  X ,  0 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ H, L, H ,  L , H ,  H  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ H, L, H ,  L , H ,  H  , H  ,  L  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  H ,  3 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ, MOD_WRITE, RETRY & ACCESS SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [LE,G_,DIR,CORR,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X,  L ,   H   , H ,  X ,  0 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ H, L, H ,  L , H ,  H  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ H, L, H ,  L , H ,  H  , H  ,  L  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  L ,  3 ] -> [ H, L, H ,  H , H ,  L  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ L, L, L ,  L , H ,  H  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ L, L, L ,  L , H ,  H  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ L, L, H ,  L , H ,  L  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ L, L, H ,  L , H ,  L  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ L, L, H ,  L , H ,  H  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ L, L, H ,  L , H ,  H  , H  ,  L  ,  RETRY   ];
 [ C , H , X,  X ,   H   , X ,  X ,  3 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
test_vectors ' READ, MOD_WRITE, RETRY & REFRESH SEQUENCE '
([CLK,RST_,AS,IOM_,REFREQ_,RW_,ERR_,COUNT] -> [LE,G_,DIR,CORR,MC1,RASI_,RFC_,DSACK_,  STATE_  ])
 [ C , H , X,  L ,   H   , H ,  X ,  0 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ H, L, H ,  L , H ,  H  , H  ,  H  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ H, L, H ,  L , H ,  H  , H  ,  L  ,   READ   ];
 [ C , H , X,  X ,   X   , X ,  L ,  3 ] -> [ H, L, H ,  H , H ,  L  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ L, L, L ,  L , H ,  H  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ L, L, L ,  L , H ,  H  , H  ,  H  ,MOD_WRITE ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ L, L, H ,  L , H ,  L  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ L, L, H ,  L , H ,  L  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ L, L, H ,  L , H ,  H  , H  ,  H  ,  RETRY   ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ L, L, H ,  L , H ,  H  , H  ,  L  ,  RETRY   ];
 [ C , H , X,  X ,   L   , X ,  X ,  3 ] -> [ H, H, H ,  L , L ,  L  , H  ,  H  , REFRESH  ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ H, H, H ,  L , L ,  H  , H  ,  H  , REFRESH  ];
 [ C , H , X,  X ,   X   , X ,  X ,  1 ] -> [ H, H, H ,  L , L ,  H  , L  ,  H  , REFRESH  ];
 [ C , H , X,  X ,   X   , X ,  X ,  2 ] -> [ H, H, H ,  L , H ,  L  , H  ,  H  ,ACCESS_CHK];
 [ C , H , X,  X ,   L   , X ,  X ,  0 ] -> [ H, H, H ,  L , H ,  H  , H  ,  H  ,  IDLE   ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ H, H, H ,  L , H ,  H  , H  ,  H  , RAS_DLY  ];
 [ C , H , X,  X ,   X   , X ,  X ,  0 ] -> [ H, H, H ,  L , L ,  L  , H  ,  H  , REFRESH  ];

 end _EDACCOE
```

Mean Time Between Events

A Discussion of Device Failures in DRAMs

TEXAS
INSTRUMENTS

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Contents

List of Illustrations

List of Tables

Introduction

System reliability is a function of many factors, most of which can be traced to proper system design techniques. As systems have become more memory intensive in recent years, the overall system reliability tends to be very closely related to the reliability of the memory. There are two general reliability terms applied to failures in memory devices, soft errors and hard failures. Soft errors refer to those types of events in which data that had been stored at a given memory location changes, but subsequent accesses can store the correct data with no more likelihood of returning incorrect data than any other location. Hard failures refer to events where a location becomes permanently affected such that data can not be reliably stored in that location. The term "events" is used to imply either or both of the two general reliability terms. The system reliability is then a combination of these two types of events. The following information will provide you with a greater knowledge of the system reliabililty events.

Mean Time Between Events

One measure of system reliability can be obtained by observing the probability that an event will occur within an interval of time. Assuming that all events are independent (i.e., any event is not caused by another event, nor will it induce a subsequent event to occur), the probability that exactly r events occur in n locations follows the general form:

$$P_r = \frac{n!}{r!(n-r)!}\, p^r\, (1-p)^{(n-r)} \qquad (1)$$

Where:

P_r = Probability of exactly r events

n = number of independent trials (i.e., number of bits)

r = number of events (i.e., number of errors)

p = probability of event r (i.e., probability of an error in a single bit)

The probability that at least r events occur is the sum of probabilities for all possible error combinations of r through n:

$$P_{total} = P_r + P_{(r+1)} + P_{(r+2)} + \ldots + P_n$$

Calculations show that for relatively small time intervals (up to 10 hours), the first term (P_r) dominates the total such that all subsequent terms may be ignored, therefore:

$$P_{total} = P_r$$

The value for p shown in the general equation (1) above may be calculated for soft errors (ps) from the error rate for a device and the number of bits contained within that device as:

$$ps = \frac{Soft\ Error\ Rate\ (errors/device-hours)}{Bits\ per\ device} \qquad (2)$$

Since soft errors have been shown predominantly to affect only single bits, division by the number of bits in the device obtains the probability for a single bit to be in error. Hard failures may affect a single bit, a group of bits, or an entire device. The groups of bits are usually located in a single row or a single column within the device; thus, the value of p for hard failures (ph) is:

$$ph = FR\left(\frac{\%B}{BD} + \frac{\%R}{BR} + \frac{\%C}{BC} + \%D\right)/100 \qquad (3)$$

Where:

FR = Hard Failure Rate (failures/device-hours)
BD = Bits per Device
BR = Bits per Row within a device
BC = Bits per Column within a device
%B = Percent of failures to a single Bit
%R = Percent of failures to a Row
%C = Percent of failures to a Column
%D = Percent of failures affecting the entire device

The probabilities calculated in equations 2 and 3 are expressed as errors per bit-hour or failures per device-hour, respectively. They could also be expressed as events per hour, where for soft errors the event is the expected number of errors per bit and for hard failures the event is the expected number of failures per device. Most designers are concerned with the "Mean Time Between Failures" (MTBF) for a particular system; however, soft errors are not necessarily failures (e.g., in error corrected systems), and this term is thus inaccurate. A more appropriate term would be "Mean Time Between Events" (MTBE) where the type of event is specified. The MTBE (expressed as hours per event) is calculated as the reciprocal of the probability, thus:

$$MTBE = 1/P \qquad (4)$$

To show how all of these formulas apply to an actual system, an example may clarify some questions. Consider a system with 64 Megawords of 1Mx1 dynamic random-access memories (DRAMs), where each word is 32 bits of data plus 7 bits for Error Detection and Correction (EDAC). This configuration consists of 64 banks of 39 devices for a total of 2496 DRAMs. Assume the system provides a distributed refresh cycle each 12 microseconds to one row and accesses the memory during active cycles every 250 nanoseconds. Also, for this example, assume the DRAMs have a Soft Error Rate of 1000 FITs (FIT = Failure In Time; thus, 1 FIT is equivalent to one event in one billion hours) and a Hard Failure Rate of 200 FITs (for this example, assume all hard errors cause the entire device to malfunction). The memory is scanned once each hour to detect and correct any soft errors that may be present (this scanning process is called "scrubbing").

The probability of one soft error occurring in any single bit during an hour is:

$$ps = \frac{Failure\ Rate\ (errors/device-hours)}{Bits\ per\ device}$$

$$= \frac{1000/1,000,000,000}{1,048,576} = 9.52 \times 10^{-13}\ errors/bit-hour$$

Similarly, the probability of a hard failure occurring during an hour is:

$$ph = FR\left(\frac{\%B}{BD} + \frac{\%R}{BR} + \frac{\%C}{BC} + \%D\right)/100$$

$$= \frac{200}{1,000,000,000}\left(\frac{0}{BD} + \frac{0}{BR} + \frac{0}{BC} + 100\right)/100$$

$$= 2.00 \times 10^{-7}\ failures/device\text{–}hour$$

For these values of ps and ph, the value of (1-p)(n-r) in equation 1 becomes very close to 1 (the actual error affects the equation by less than 1% so that it may be ignored). Equation 1 may then be used as:

$$P_r = \frac{n!}{r!(n-r)!}\ p^r \qquad (5)$$

For the system under consideration, the probability of a single soft error (SE) occurring is:

$$P_{1S} = \frac{(2496\ devices)\ (1,048,576\ bits/device)!}{(1\ SE)!\ ((2496 \times 1,048,576)-1\ SE)!}\left(9.52 \times 10^{-13}\right)^{(1SE)}$$

$$= \frac{(2496 \times 1,048,576)}{1}\left(9.52 \times 10^{-13}\right) = 0.0025$$

This shows that the probability of a soft error is 0.0025 events/hour. The Mean Time Between Events is the reciprocal of the probability, thus:

$MTBE_{1S}$ = 1/P

= 1/(0.0025 events/hour)

= 400 hours/event or about 16.7 days

Analysis of the probability equation shows that for the case of a single soft error, the equations can be reduced to:

$$P_{1S} = \frac{(Number\ of\ devices)\ (FITs)}{1,000,000,000}$$

and

$$MTBE_{1S} = \frac{1,000,000,000}{(Number\ of\ devices)(FITs)}$$

For systems that employ Error Detection and Correction (EDAC), such as the one under consideration, a single error will be corrected and thus not affect system operation. However, the occurrence of two bits being in error in the same word will cause problems in the system because the EDAC cannot correct a double-bit error in the scheme described. Realize that in this case, the bits of interest are in a given word and the probability is based upon the word size of the memory system. Because the memory is scrubbed each hour, the probability of two errors occurring within a single word of 39 bits is:

$$P_{2s(word)} = \frac{39!}{2!\ (39-2)!}\left(9.52 \times 10^{-13}\right)^2$$

$$= \frac{(39 \times 38)}{2}\ 9.07 \times 10^{-25} = 6.72 \times 10^{-22}$$

and because the system contains 16 Megawords, the probability of one double-bit error occurring in the system is:

$$P_{2S} = \frac{(67,108,864)!}{1!(67,108,864-1)!} 6.72 \times 10^{-22} = 4.51 \times 10^{-14}$$

thus the MTBE for a double bit failure is:

$$MTBE_{2S} = 1/4.51 \times 10^{-14} = 2.21 \times 10^{13}$$

This would indicate that with "scrubbing" of the memory at least once an hour, the possibility of a double-bit failure is very remote (once in 24 hundred million years!). For the system that does not scrub the memory, the probability equation results in a dependent equation that is the probability that an error will occur in one of the remaining bits in a word (i.e., given that an error has occurred, what is the likelihood that a subsequent error will happen in that word). For the example of a 32-bit system with EDAC, the probability that one of the remaining 38 bits in a 39-bit word would fail is:

$$P_{SS} = \frac{(38)!}{1!(38-1)!}\left(9.52 \times 10^{-13}\right)^1 = \frac{(38)}{1}\ 9.52 \times 10^{-13} = 3.62 \times 10^{-11}$$

$$MTBE_{SS} = 1/3.62 \times 10^{-11} = 2.76 \times 10^{10}$$

Given that an error has occurred in a word, the system will operate an average of 27.6 billion hours (28 hundred thousand years) before a subsequent soft error will cause a double-bit error.

Table 1 shows results for several systems with differing word lengths to give an indication of how often various events might be expected in a system. Notice that each of the configurations listed is for a 64-Megaword memory array. Word sizes have been chosen to reflect a common nonprotected (no parity or EDAC) word length and the protected (either parity for 8-bit word or EDAC for other word lengths) word. Data in this table is calculated using the complete probability equation given in Equation 1.

Table 1. Mean Time Between Events for Various System and Error Types
Device Type 1M DRAM
Soft Error FITs = 1000 Hard Error FITs = 200
System with 64 Megawords

Bits per Word	8	9	16	22
Total Devices	512	576	1024	1408
1 Soft Error	1954	1736	977	710
1 Hard Error	9767	8682	4884	3552
2 Soft/system	7.63E+06	6.03E+06	1.91E+06	1.01E+06
2 Hard/system	1.91E+08	1.51E+08	4.77E+07	2.52E+07
2 Soft/Word	1.46E+14	1.14E+14	3.41E+13	1.77E+13
2 Hard/Word	1.40E+10	1.57E+10	2.79E+10	3.84E+10
Hard then Soft	1.25E+05	1.11E+05	6.25E+04	4.55E+04
Hard then Hard	7.14E+05	6.25E+05	3.33E+05	2.38E+05
Soft then Hard	7.14E+05	6.25E+05	3.33E+05	2.38E+05
Soft then Soft	3.74E+10	3.28E+10	1.75E+10	1.25E+10

Bits per Word	32	39	64	72
Total Devices	2048	2496	4096	4608
1 Soft Error	488	401	244	217
1 Hard Error	2442	2004	1222	1086
2 Soft/system	4.77E+05	3.21E+05	1.19E+05	9.42E+04
2 Hard/system	1.19E+07	8.03E+06	2.98E+06	2.36E+06
2 Soft/Word	8.26E+12	5.53E+12	2.03E+12	1.60E+12
2 Hard/Word	5.58E+10	6.80E+10	1.12E+11	1.26E+11
Hard then Soft	3.13E+04	2.56E+04	1.56E+04	1.39E+04
Hard then Hard	1.61E+05	1.32E+05	7.94E+04	7.04E+04
Soft then Hard	1.61E+05	1.32E+05	7.94E+04	7.04E+04
Soft then Soft	8.46E+09	6.90E+09	4.16E+09	3.69E+09

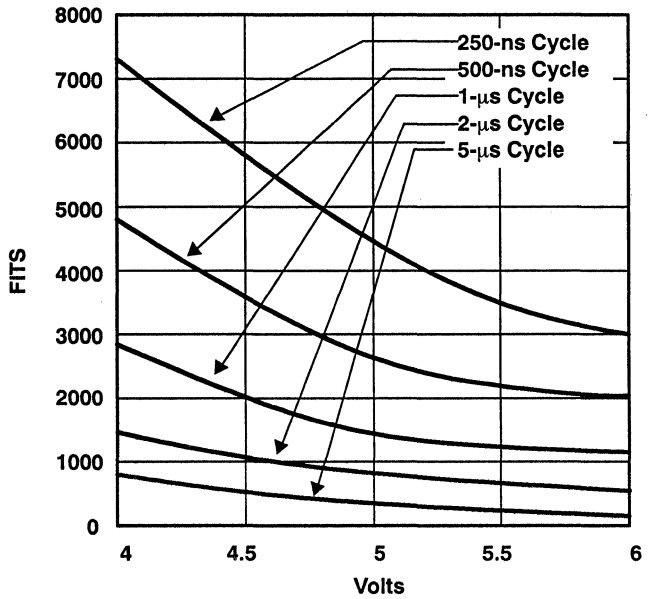
Soft Error Rates have been demonstrated to be dependent upon cycle time and operating voltage as shown in Figure 1. The average cycle time at which the memories operate in a system is not necessarily the same as the active memory cycle time. If the processor performs accesses to memory such that not all devices are accessed for a given memory cycle, then those not accessed are not being cycled. When there are multiple banks of memory in the system, some of which are just being refreshed while one bank is active, then the Average Cycle Time (ACT) for the system is given by:

$$ACT = \frac{(\#AD \times CT) + ((\#TD - \#AD) \times RT)}{(\#TD)}$$

Where:

ACT = Average Cycle Time
#AD = Number of Active Devices each processor cycle
#TD = Total Number of Devices
CT = Active memory Cycle Time for processor access
RT = Refresh Cycle Time (Average per row)

Note that the quantity (#TD – #AD) is the number of devices just being refreshed.



1 FIT = 1 Failure per billion device hours

Figure 1. DRAM Failures vs Voltage (Failures in FITs)

Table 2 shows the ACT for some systems comprised of a given number of memory banks and varying Refresh Cycle Times for an Active Cycle Time of 250 nanoseconds.

Referring to the system that has been used for all of the calculations in this report, the Average Cycle Time would appear in the column under 64 banks and since the refresh time is 12 μs, the ACT is 11.82 μs.

Using the data from Figure 1 and Table 2, a Table of Mean Time Between Events can be derived as in Table 3 for systems of various sizes.

The MTBE for hard failures (which are not dependent on cycle time) are combined in Figure 2 to allow determination of system MTBE for a single hard or soft event. A single such chart cannot be made for double events since there is a dependency upon the word width, however, the information provided in this report may be used to determine the Mean Time Between Events for any system.

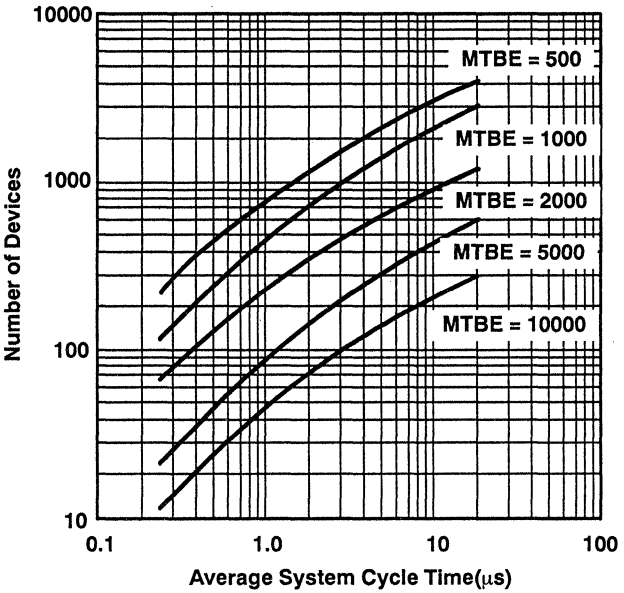
Table 2. Average Cycle Time for Various Memory Configurations

Active Cycle Time	250 ns							
Total Banks	1	2	4	8	16	32	64	128
Refresh Cycle Time (μs)								
1	0.25	0.63	0.81	0.91	0.95	0.98	0.99	0.99
2	0.25	1.13	1.56	1.78	1.89	1.95	1.97	1.99
4	0.25	2.13	3.06	3.53	3.77	3.88	3.94	3.97
6	0.25	3.13	4.56	5.28	5.64	5.82	5.91	5.96
8	0.25	4.13	6.06	7.03	7.52	7.76	7.88	7.94
10	0.25	5.13	7.56	8.78	9.39	9.70	9.85	9.92
12	0.25	6.13	9.06	10.53	11.27	11.63	11.82	11.91
14	0.25	7.13	10.56	12.28	13.14	13.57	13.79	13.89
15	0.25	7.63	11.31	13.16	14.08	14.54	14.77	14.88
15.625†	0.25	7.94	11.78	13.70	14.66	15.14	15.38	15.50
16	0.25	8.13	12.06	14.03	15.02	15.51	15.75	15.88

† A Refresh Cycle Time of 15.625 μs is the maximum allowed by the specification for DRAMs operating with a distributed refresh cycle.

Table 3. MTBE for a Given Cycle Time and Number of Devices

Observed FITs	7400	3700	2000	1100	500	250	125
Cycle Time (μs)	0.25	0.50	1.00	2.00	5.00	10.00	20.00
Number of Devices							
16	8446	16892	31250	56818	125000	150000	500000
32	4223	8446	15625	28409	62500	125000	250000
64	2111	4223	7813	14205	31250	62500	125000
128	1056	2111	3906	7102	15625	31250	62500
256	528	1056	1953	3551	7813	15625	31250
512	264	528	977	1776	3906	7813	15625
1024	132	264	488	888	1953	3906	7813
2048	66	132	244	444	977	1953	3906
4096	33	66	122	222	488	977	1953



NOTE: 4.5 V, Soft Errors = 1000 FITs, Hard Errors = 2000 FITs

Figure 2. MTBE for a System Combination of Hard and Soft Errors

Contents

Memory Mapping Using SN74LS610 and SN74LS612

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Contents

List of Illustrations

List of Tables

Introduction

Microprocessors, due to the advent of high-density semiconductor memories (i.e., 64K or larger), are being used more and more in systems featuring memory structures larger than 64K bytes. Some of the microprocessors in use or available today have a 16-bit address bus, with a maximum addressing capability of 64K words. Due to this limitation, some sort of memory mapping is necessary to adapt these microprocessors to applications where large memory structures are required.

The memory mappers (SN74LS610 and SN74LS612) from TI were designed to alleviate this addressing limitation. These devices employ a paged memory mapping technique in expanding the system memory address bus by 8 bits, thus effectively increasing the system addressing capability by a factor of 2^8 or 256. For microprocessors with a 16-bit address bus (such as the Z-80, the 8085, and the 6800), this results in an increase in the maximum addressing capability from 64K bytes to 16M bytes and for the TMS9900 (which has a 15-bit address bus), the result is an increase from 32K words to 8M words (words = 2 bytes).

In the mapping operation, the four MSBs of the microprocessor address word are used to access one of the sixteen 12-bit registers of the memory mapper's 16 × 12-bit RAM array. Each mapper register is capable of holding a 12-bit address that will be termed the page address and will be used as the 12 MSBs of the memory address bus. The remaining 12 bits (11 in the case of the TMS9900) of the microprocessor address bus will be transferred directly to memory from the microprocessor and will be used to address the memory locations within each page. (See Figure 1)

The memory will be organized into 2^x pages (where x equals the number of bits of the page address) with 2^{n-4} words or bytes (where n is the bit length of the microprocessor address bus) per page. Once loaded, the mapper can access only 16 pages or 64K bytes (32K words in the TMS9900 cases). In order to access more pages, the memory mapper RAM array must be reloaded with 16 new page addresses. This is done by the microprocessor via the data bus with the mapper in the WRITE mode. (A more detailed description of the modes of operation will be given later in this report.)

Functional Description

A functional block diagram of the SN74LS610 memory mapper, which consists mainly of: a 4-bit 2-to-1 multiplexer, a 16 × 12-bit RAM array, a 12-bit 2-to-1 multiplexer, 24 3-state buffers, control logic, and in the case of the 'LS610, a 12-bit transparent latch, is shown in Figure 2. Table 1 lists the functional differences between the 'LS610 and 'LS612. Table 2 lists the function of each pin.

Depending on the state of the input control signals (i.e., $\overline{CS}$. R/$\overline{W}$, $\overline{STROBE}$, $\overline{MM}$, and $\overline{ME}$), the mapper can be operated in three basic modes of operation, I/O (READ or WRITE), MAP, and PASS. An explanation of each mode and the control signals necessary to achieve that mode of operation is given below: (Refer to Table 3)

Input/Output Mode

In this mode, a page address can be loaded either into a mapper register or can be read from a memory mapper register depending on the state of the R/$\overline{W}$ (READ/WRITE) input. This input signal controls either the READ or WRITE function of the I/O Mode.

WRITE Mode

One of the sixteen 12-bit registers is loaded with a page address via the D0-D11 I/O ports from the microprocessor. The address of the selected register is inputted via the RS0-RS3 inputs and is usually the four LSBs of the microprocessor address word. The chip select ($\overline{CS}$), the strobe ($\overline{STROBE}$), and R/$\overline{W}$ controls should all be low.

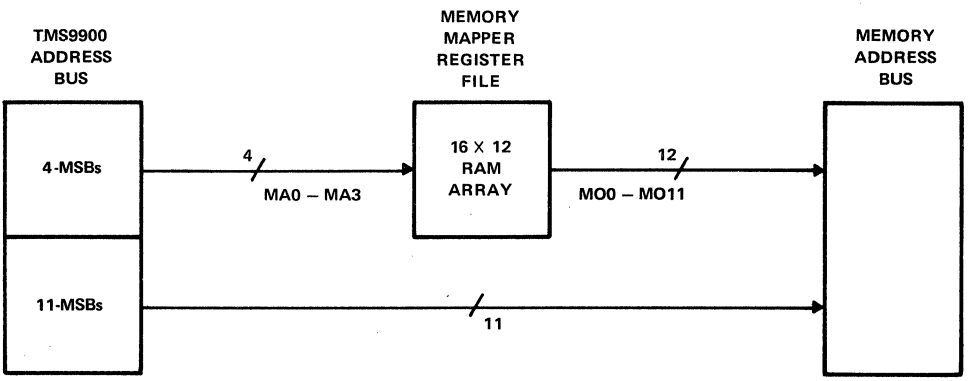

Figure 1. Mapping Operation

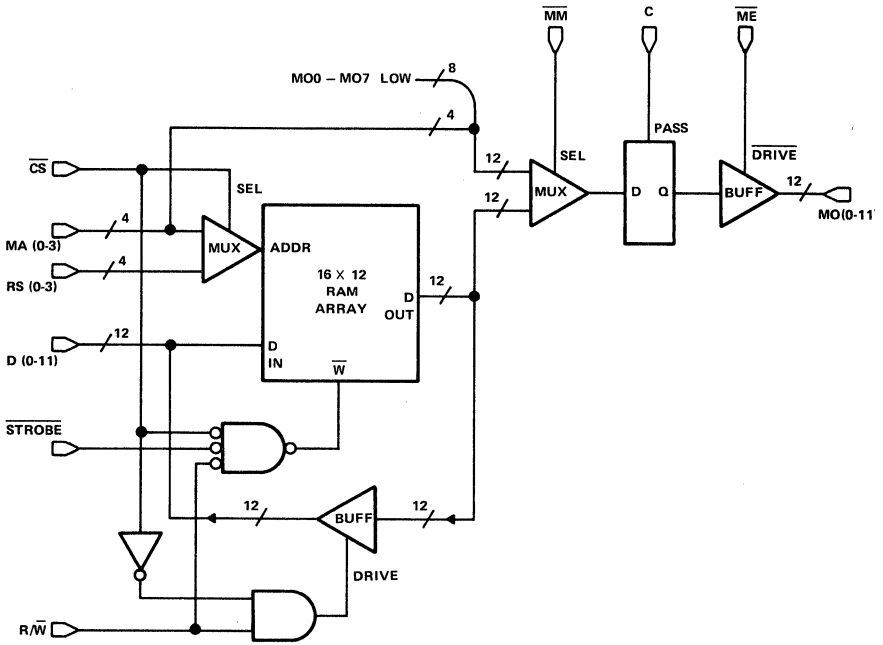

Figure 2. Logic Diagram of the Memory Mapper 'LS610

Table 1. Device Comparison

Device	Map Outputs Latched	Map Output Type
SN74LS610	Yes	3-State
SN74LS612	No	3-State

READ Mode

The contents of one of the sixteen 12-bit registers is read from the mapper via the D0-D11 I/O ports. As in the WRITE mode, the mapper register is selected by the address on the RS0-RS3 inputs. Again chip select ($\overline{CS}$) should be low, while the R/$\overline{W}$ should be kept high.

MAP Mode

The contents of one of the sixteen 12-bit memory mapper registers is outputted to the system address bus via the MO0-MO11 outputs. The address on MA0-MA3 selects the mapper register and is usually the four MSBs of the microprocessor address word. The chip select ($\overline{CS}$) must be inactive (high), the map mode ($\overline{MM}$) control and the map enable ($\overline{ME}$) must both be active (low). The n – 4 LSBs, where n equals the microprocessor address bit length, of the microprocessor address bus will be transferred directly to memory from the microprocessor, while the remaining 12 MSBs of the system address bus will be driven onto the bus by the memory mapper.

Table 2. Pin Functions

Pin	Pin Name	Functional Description
7-12 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$. (D0 corresponds to MO0 and is the most significant bit.)
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations. (RS3 is the least significant bit.)
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high). (MA3 is the least significant bit.)
14-19 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO-MO11 and low levels on MO0-MO7. (MO11 is the least significant bit.)

Table 2. Pin Functions (Continued)

Pin	Pin Name	Functional Description
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the four bits present on the map address inputs are passed to the map outputs.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 (no internal connection for 'LS612). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	Power supply (5 V) and network ground (substrate) pins

Table 3. Modes of Operation

Mapper Inputs	I/O		Map	Pass
	Write (Load)	Read (Verify)		
$\overline{CS}$	Active (Low)	Active (Low)	Inactive (High)	Inactive (High)
$\overline{STROBE}$	Active (Low)	Don't Care	Don't Care	Don't Care
R/$\overline{W}$	Low	High	Don't Care	Don't Care
$\overline{MM}$	Don't Care	Don't Care	Active (Low)	Inactive (High)
$\overline{ME}$	Inactive (High)	Inactive (High)	Active	Active
RS0-RS3	Address of Selected Register	Address of Selected Register	Don't Care	Don't Care
MA0-MA3	Don't Care	Don't Care	Address of Selected Register	Address of Selected Register
MO0-MO11	High Impedance	High Impedance	Valid Address	Valid Address
D0-D11	Register contents to be loaded (input)	Register contents to be read (output)	Input Mode	Input Mode

PASS Mode

The four LSBs (MO8-MO11) of the memory mapper address bus (MO0-MO11) will be the same as the address on the MA0-MA3 input bus, while the remaining eight MSBs of the memory mapper address bus will all be low. The chip select ($\overline{CS}$) and the map mode ($\overline{MM}$) should both be inactive (high); map enable ($\overline{ME}$) should be active. In other words, the address on the system address bus will be the same as the address outputted by the microprocessor, and the memory mapper becomes transparent to the system.

SYSTEMS INTEGRATION

The flexibility of the memory mapper is such that it can be used with microprocessors that have either an 8-bit or a 16-bit data bus. In order to use the memory mapper to its fullest potential (i.e., expand the address bus by eight bits) with an 8-bit microprocessor, the 12-bit page address must be multiplexed into the mapper via the 8-bit data bus. This means that the

time it normally takes to load or read the memory mapper will be at least doubled and extra external circuitry will be necessary. If the requirement of the system is such that the address bus needs to be increased by only four bits, then there is no need for multiplexing in the page address. Of course, this means that the address bus is expanded to only 20 bits resulting in a 1-megabyte addressing capability. Next in this report, we will look at two 8-bit systems utilizing the 'LS612 memory mapper.

TMS9995-Based System

Figure 3 shows a TMS9995-based system using the 'LS612 to expand the address bus by four bits. The TMS9995 is an 8-bit microprocessor with a 16-bit address bus. This system employs the Programmable System Interface (TMS9901) to control the operation of the mapper. The control of the mapper is software programmable via the I/O ports of the TMS9901. Since the mapper registers are viewed as part of the logical memory space, an address decode (AD0) of the 12 MSBs is gated with a CRU bit to select the mapper for a READ or WRITE operation. The specific mapper register is then selected by the four LSBs of the microprocessor address bus (A15-A12) via the RS0-RS3 inputs of the mapper. Table 4 shows the state of the three control signals P0, P1, and AD0 and the corresponding mode of operation of the mapper. When placed in the I/O mode, the READ or WRITE operation is then controlled by memory signals from the microprocessor (i.e., $\overline{WE}$/$\overline{CRUCLK}$, $\overline{MEMEN}$, and $\overline{DB\ IN}$). On POWER-UP and RESET, the I/O ports of the '9901 are put into the input mode. The pull-up resistors R1 and R2 will ensure the mapper is placed in the pass mode during POWER-UP and RESET. The resultant address bus is 20 bits wide, and SA19 is the LSB.

Z-80-Bassed System

Figure 4 shows another 8-bit (Z-80-based) system using the TI memory mapper. In this case, the control of the mapper is implemented by two flip-flops feeding $\overline{MM}$ and $\overline{CS}$. These flip-flops are programmed by the Z-80 and are addressed by the data bus, D0-D1. Table 5 shows the necessary states of D0 and D1 to set the mapper in its proper mode of operation. Again during POWER-UP or RESET, the flip-flops are both cleared by $\overline{RST}$, which is supplied by the system and which puts the mapper in the pass mode.

Table 4. TMS9900/'LS610 Control Signals

Memory Mapper Mode of Operation	Control Signals		
	P1	P0	AD0
MAP	L	H	L
PASS	H	H	L
I/O	H	L	L

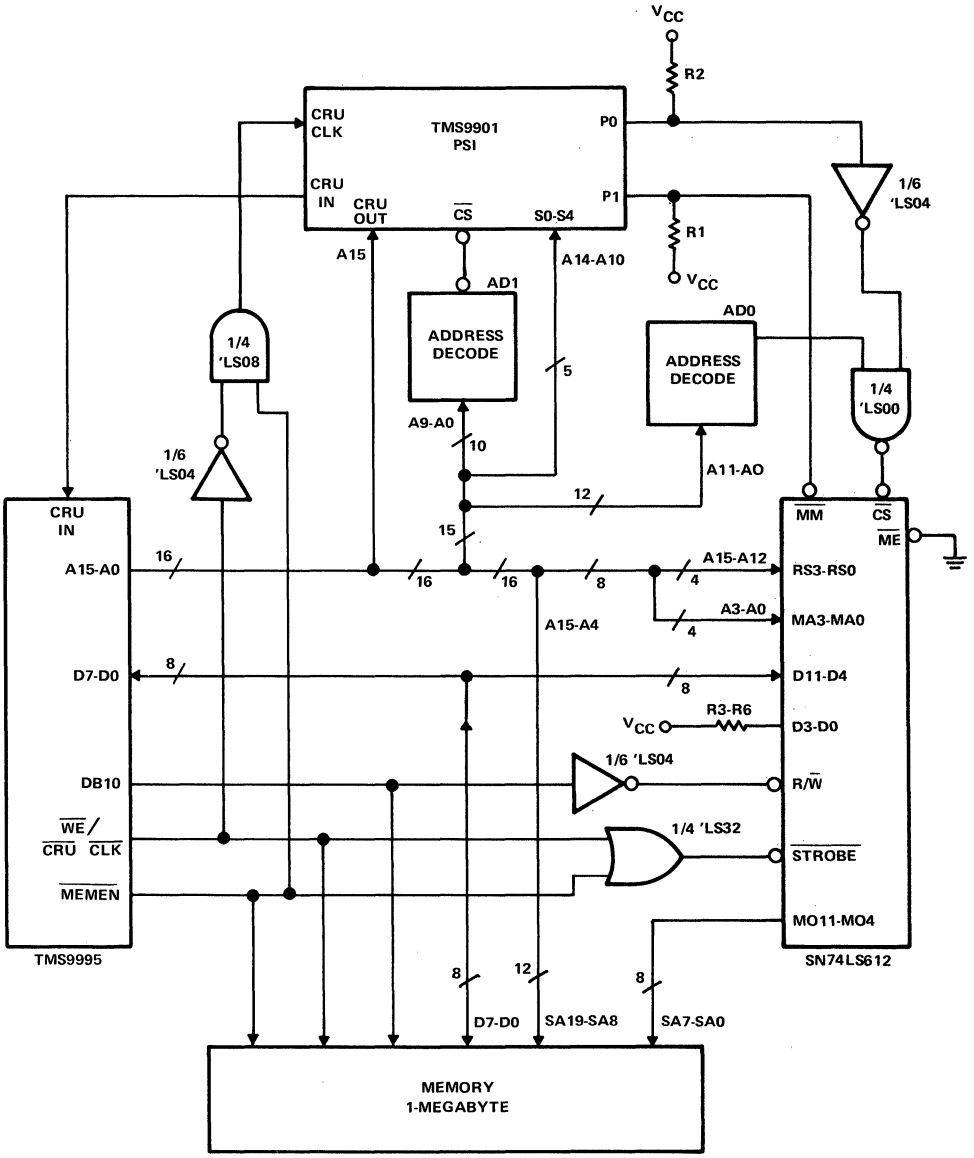

Figure 3. TMS9995 with Memory Mapper

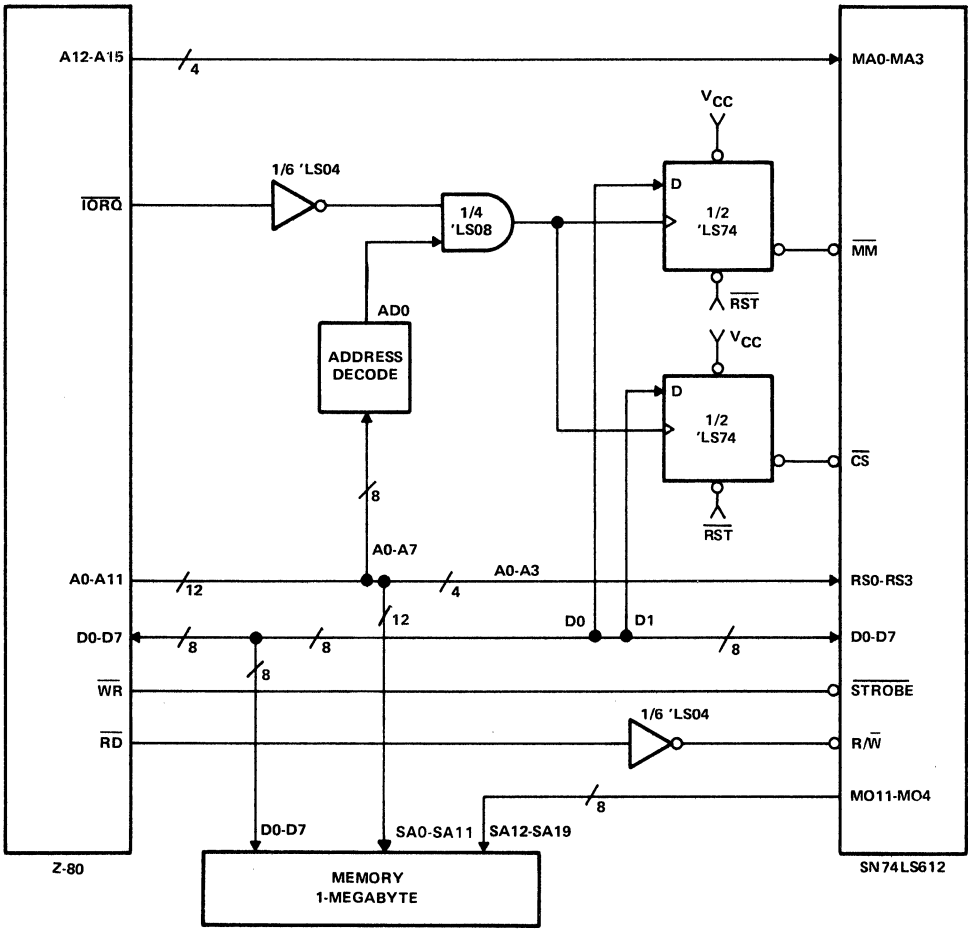

Figure 4. Z-80 with Memory Mapper

Table 5. Z-80/'LS610 Control Signals

Control Signals			Memory Mapper
D0	D1	(AD0) $\overline{IORQ}$	Mode of Operation
L	L	↑	MAP
H	L	↑	PASS
L	H	↑	I/O

TMS990-Based System

One of the limitations of using an 8-bit microprocessor with the memory mapper, without multiplexing the page address, is that the address bus can only be expanded four bits. In a 16-bit system, one based on a 16-bit microprocessor like the TMS9900, no extra circuitry is necessary to load the mapper with the full 12-bit address. Figure 5 shows a TMS9900 with an SN74LS612 for memory mapping. The control of the mapper is implemented in the same fashion as the system using the TMS9995 mentioned previously in the report. The resultant addressing capability is eight megawords. These TI microprocessors have set aside address space for RESET, XOP and INTERRUPT VECTORS, which are addressed when the microprocessor performs a context switch. During a context switch, the microprocessor must be able to address these locations which are part of the logical address (i.e., locations that are capable of being addressed by the microprocessor independently). One method, besides placing the mapper into the pass mode, is to load the memory mapper register whose 4-bit address is O_H with the address of the first page of physical memory. This, like the pass mode, will effectively make the memory mapper appear to be transparent.

Another point worth noting is that in all three of the previously mentioned systems, the $\overline{ME}$ input was always connected to ground. This caused the mapper address buffers to be enabled during all modes of operation of the mapper. This is only a problem during the I/O mode where, when loading the mapper register, other memory locations are also being written into. The method used to avoid destroying data already in memory was to put the mapper into the pass mode during the I/O operation. This was accomplished simply by pulling $\overline{MM}$ input high, thus making the system address equal to the microprocessor address.

Multimapper Systems

In a system employing a single memory mapper, the maximum active addressing capability is only 16 pages; if increased addressing capabilities are needed, the mapper must be reloaded. To avoid this procedure, another mapper may be added to the system. This will not increase the overall addressing capability of the system, but it will double the amount of active pages and will also afford twice the active addressing capability. Even though the control of two mappers is a little more detailed than the control of one, the same basic methods employed in the systems with one mapper can be used here.

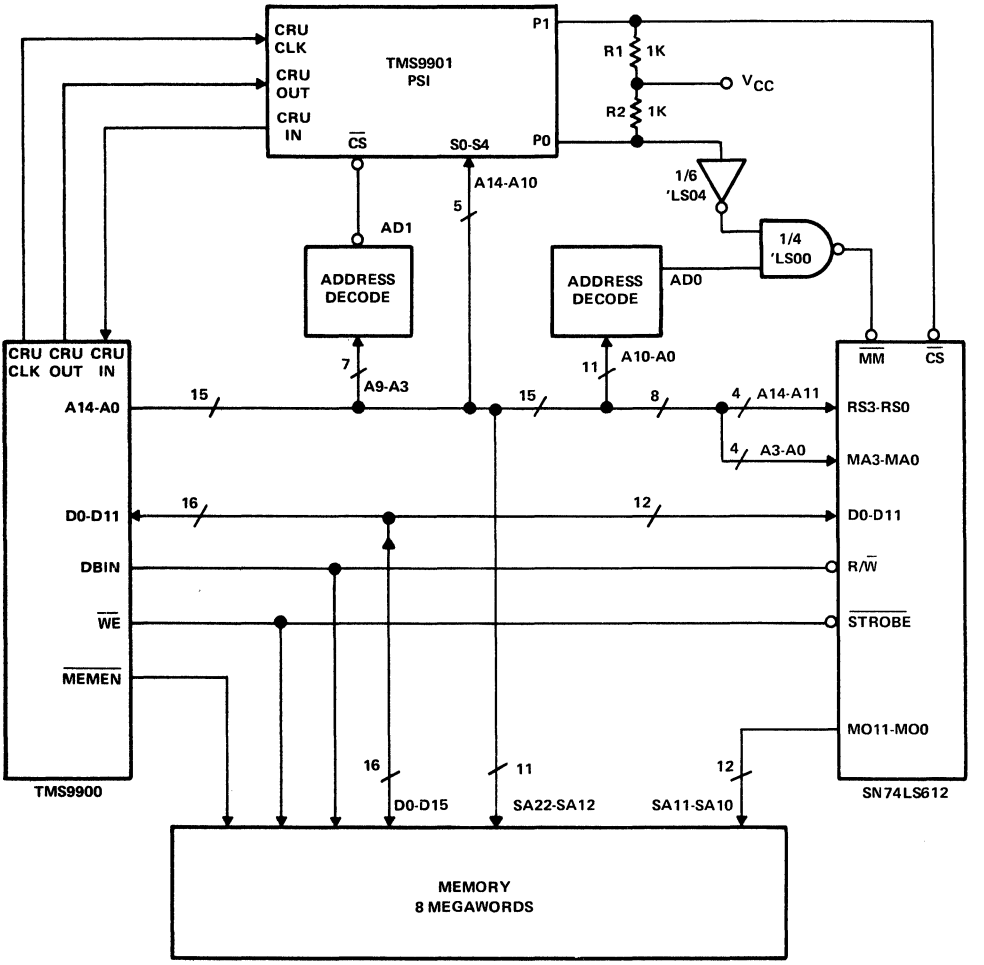

Figure 5. TMS9900 with Memory Mapper

TIMING

The subject of how the maper affects the critical timing parameters of the memory READ/WRITE cycles and what changes, if any, are needed to accommodate the mapper, have not been discussed in this report. First, looking at the I/O mode of operation where the mapper registers are either loaded or read from, it is seen that the mapper registers can be regarded as standard common I/O, static RAMs, with maximum access times (RS to valid MO, $T_A = 25°C$, $C_L = 50$ pF, $V_{CC} = 5$ V) of 75 ns. Once the I/O mode is set ($\overline{CS}$ = low), the only two signals necessary to read or write into the mapper are $\overline{STROBE}$ and R/$\overline{W}$. As shown in the previously mentioned system, these signals were supplied directly from the microprocessor with no wait states necessary to perform either function. This will be the case with most microprocessors.

In the MAP and PASS mode, the main concern is the maximum access time (MA to MO). This access time is specified at a maximum of 70 ns, which, depending on the timing of the microprocessor and the memory used, may or may not cause any problems. In the Z-80-based system, no wait states were introduced by the mapper because the memory control signals become active 95 ns after the microprocessor address bus became valid. This gives the address bus sufficient time to settle down.

SUMMARY

The possible uses of the memory mapper and the various techniques that can be employed to control its operation are numerous and only some examples were shown in this report. Some of the other possible applications of the mapper include: (1) achieving system addressing capability greater than 16 megabytes is accomplished by reducing the number of mapper registers used by a factor of 2, thus increasing the size of each page by the same factor of 2 without affecting the total amount of pages; (2) being used in systems employing DMA; (3) memory protection which can be accomplished by sacrificing one or two bits of the page address, and gating these bits with the memory control signals.

Another technique that may be employed in controlling the modes of operation of the mapper is to use PROMs.

The SN74BCT2423 and SN74BCT2424 in Memory Interleave/Interface Applications

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Contents

List of Illustrations

Memory Interleave Applications

Memory interleaving is an organizing technique for Dynamic RAMs that results in significantly reduced memory access cycle times. When even-address words of memory are located in one bank of DRAM and odd-address words of memory are located in the other bank, sequential accesses from the memory will be requested from alternating banks. This organization scheme takes advantage of the fact that when memory banks are accessed alternatively, the access cycles can be overlapped to avoid the DRAM's $\overline{RAS}$ precharge time.

A typical access cycle timing of a 100-ns DRAM is shown in Figure 1. For this type of access cycle without memory interleave, the subsequent access cycle to the DRAM cannot begin until the $\overline{RAS}$ precharge time of 80 ns has expired. Based on this timing diagram, every access cycle takes 180 ns.

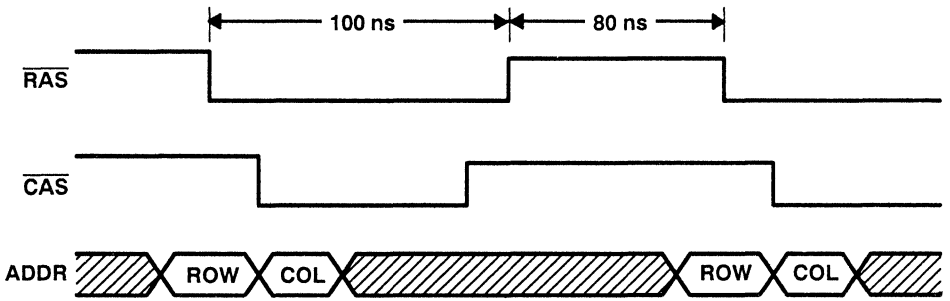


Figure 1. Typical DRAM Access Cycle Timing

In an interleaved memory organization, BANK0 of the DRAM is accessed by $\overline{RAS0}$ and $\overline{CAS0}$ signals and BANK1 is accessed by $\overline{RAS1}$ and $\overline{CAS1}$ signals as shown in Figure 2. When the DRAM banks are accessed alternatively, the access cycle to the next bank need not wait for the previous bank's $\overline{RAS}$ precharge time. Based on this timing, each access cycle takes 100 ns. The reduction in memory access time for this ideal case is:

$$\%\ time\ improvement\ \text{for}\ interleaving = \frac{180\ ns - 100\ ns}{180\ ns} = 44\%$$

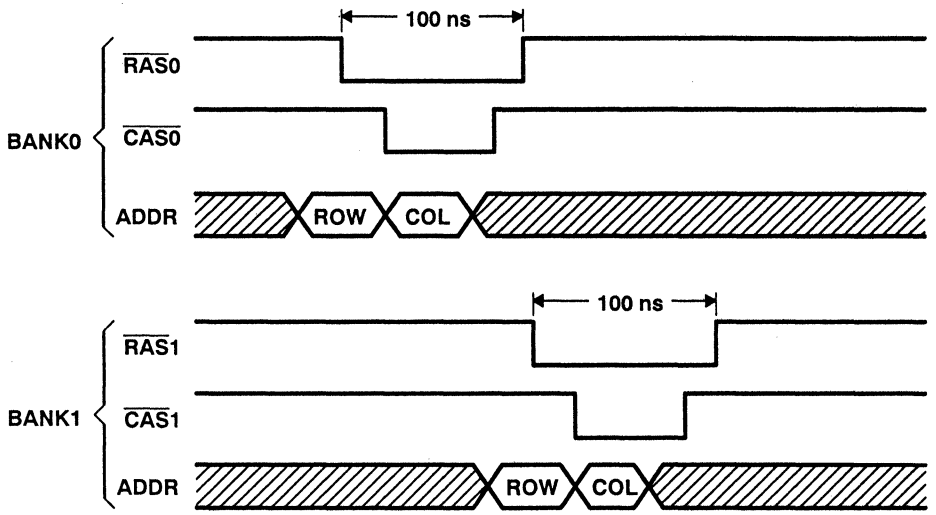


Figure 2. Two-Way DRAM Access Cycle Timing

Realistically, these two types of access cycles will be interspersed because of the sequential nature of the instruction fetches and random nature of the operand (data) accesses. A typical breakdown between these two types of access cycle is 50%. Under this assumption, the following calculations can be made:

$$\textit{Access cycles without interleave} = 180\ ns$$

$$\textit{Interspersed access cycles} = (180\ ns \times 50\%) + (100\ ns \times 50\%) = 140\ ns$$

$$\%\ \textit{time improvement for interleaving} = \frac{180\ ns - 140\ ns}{180\ ns} = 22\%$$

Figure 3 shows how the 'BCT2423/24 can be used to implement a memory interleave organization. Since the access cycles of the memory are overlapped, the need for latches arises. The 'BCT2423/24's input latches are available to meet this need. The multiplexed operation of the 'BCT2423/24 makes the device ideal for any memory interleave application where 2n banks of memory data must be multiplexed onto one bus. In addition to the multiplexing feature, 'BCT2423/24's large output drive capability eliminates the need for bus drivers to interface to the processor bus. The BiCMOS process used on 'BCT2423/24 greatly reduces the standby power of the device, which is an attractive feature when power consumption and noise problems are major concerns for the memory design.

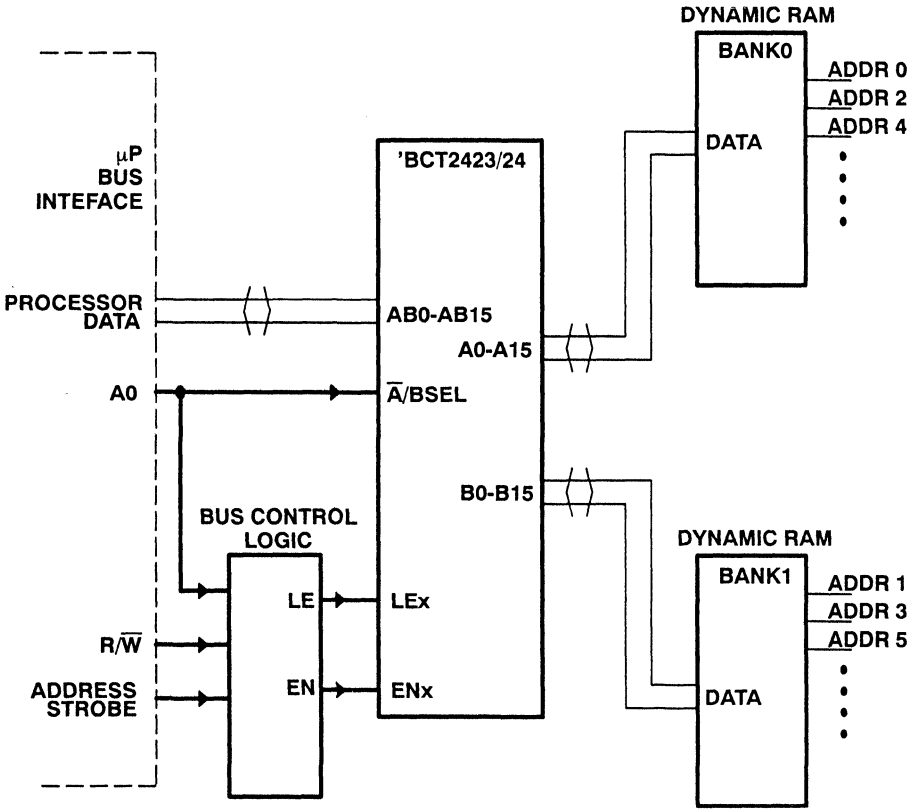
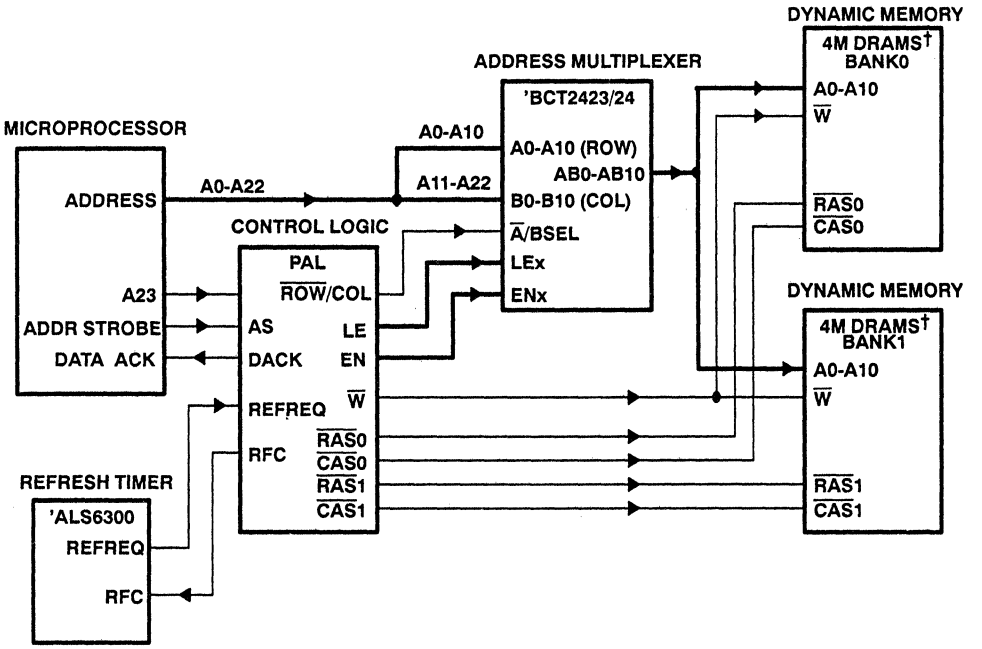


Figure 3. Memory Interleave System Interface

Memory Interface Applications

In addition to memory interleave application, the 'BCT2423's and 'BCT2424's multiplexing function can also be used to multiplex the memory address into row and column address of the DRAM. As the DRAM sizes get larger, more address signals are needed to access the memory. Figure 4 shows how the 'BCT2423 or 'BCT2424 is used in a typical address multiplexing of the 4M DRAMs in a discrete logic implementation of the DRAM control logic. To generate the refresh address that is normally provided by the counter internal to the multiplexer, one can make use of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh feature of the DRAM, where refresh addresses are generated by the DRAM.



† Use the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh feature of the DRAM to take advantage of the DRAM's internal refresh counter.

Figure 4. Use of SN74BCT2423 and SN74BCT2424 in DRAM Interface Applications

Explanation of Logic Symbols

by F.A. Mann

Contents

List of Tables

List of Illustrations

Explanation of Logic Symbols†

1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

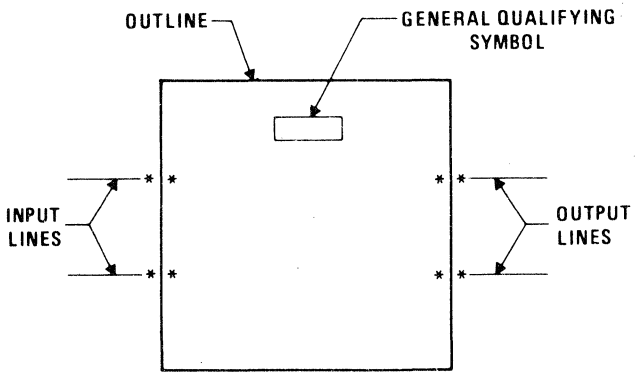
Internationally, IEC Technical Committee TC-3 has approved a new document (Publication 617-12) that consolidates the original work started in the mid 1960s and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations, and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables to further help that understanding.

2 Symbol Composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbol is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left, and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

† Written by F. A. Mann.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 1. Symbol Composition

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols, and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that, unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition, the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

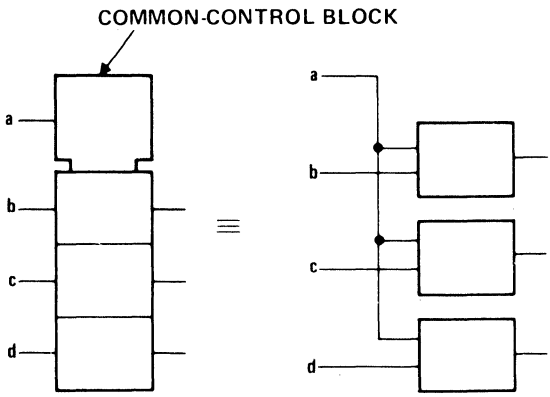


Figure 2. Common-Control Block

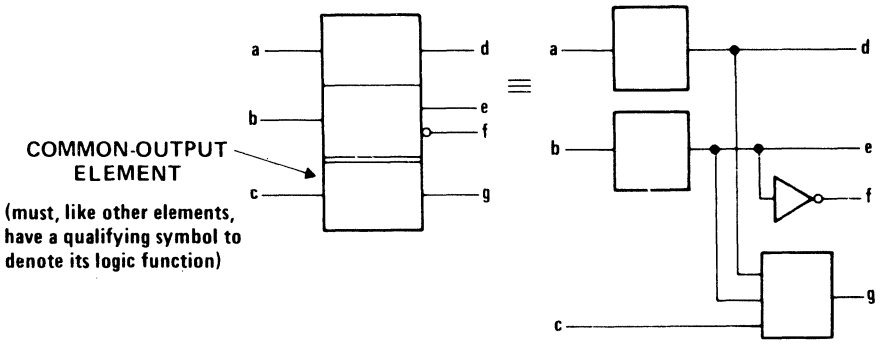


Figure 3. Common-Output Element

3 Qualifying Symbols

3.1 General Qualifying Symbols

Table 1 shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

Table 1. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k + 1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⊓	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OCT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	†	SN74LS385
CPG	Look-ahead carry generator.	'HC182	SN74182
π	Multiplier.	†	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⊓	Retriggerable monostable.	'HC123	SN74LS422
1⊓	Nonretriggerable monostable (one-shot).	'HC221	SN74121
G ⊓	Astable element. Showing waveform is optional.	†	SN74LS320
!G ⊓	Synchronously starting astable.	†	SN74LS624
G! ⊓	Astable element that stops with a completed pulse.	†	†
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020	†

† Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table 1. General Qualifying Symbols (Continued)

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
ROM	Read-only memory.	†	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	†	SN74LS222
I=0	Element powers up cleared to 0 state.	†	SN74AS877
I=1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	'ACT2140	SN74LS608

†Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

3.2 General Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2, and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table 2. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line, and, if confusion can arise about the number of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in section 4.

Table 2. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

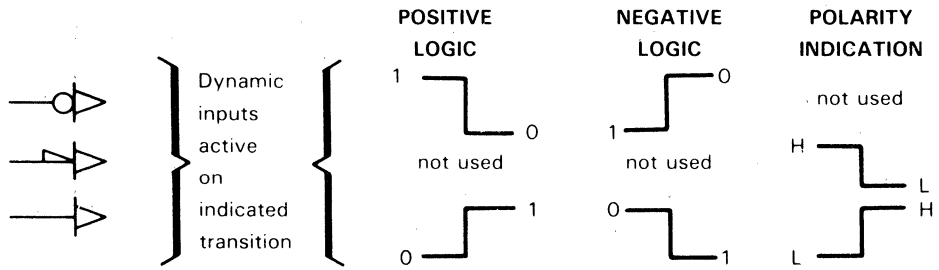
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 3-14).

Input for digital signals (on an analog symbol) (see Figure 3-14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, then these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table 3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state, it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in section 8. Binary-weighted inputs are arranged in order, and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document, weights of input and output lines will usually be represented by powers of two only when the binary grouping symbol is used; otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 31). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs, and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally, these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 3. Symbols Inside the Outline

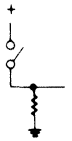
Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See paragraph 5.

Bi-threshold input (input with hysteresis)

N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection.

Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.

N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection.



Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.

Three-state output

Output with more than usual output capability (symbol is oriented in the direction of signal flow).

Enable input

When at its internal 1-state, all outputs are enabled.

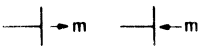
When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are in the high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.

J, K, R, S

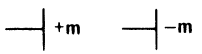
Usual meanings associated with flip-flops (e.g., R = reset to 0, S = reset to 1).

Toggle input causes internal state of output to change to its complement.

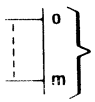
Data input to a storage element equivalent to:



Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.



Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.



Binary grouping. m is highest power of 2.

Table 3. Symbols Inside the Outline (Continued)

CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

4 Dependency Notation

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined, and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table 4 at the end of section 4.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General Rules for Dependency Notation
4.4	V, OR
4.5	N, Negate (Exclusive-OR)
4.6	Z, Interconnection
4.7	X, Transmission
4.8	C, Control
4.9	S, Set and R, Reset
4.10	EN, Enable
4.11	M, Mode
4.12	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a**, and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

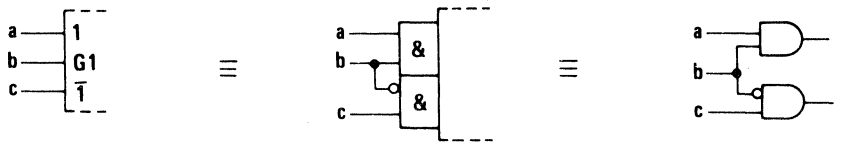


Figure 4. G Dependency Between Inputs

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

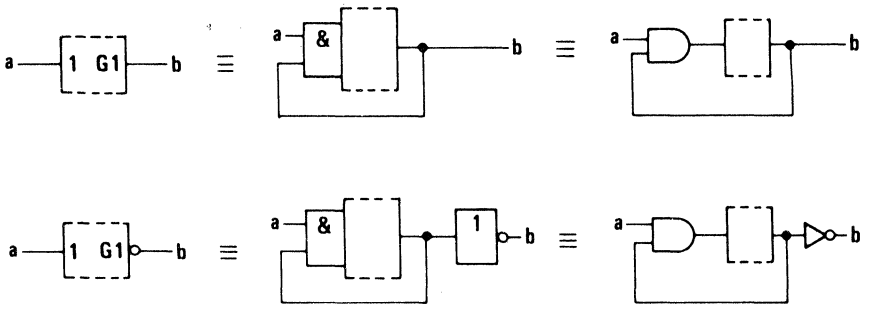


Figure 5. G Dependency Between Outputs and Inputs

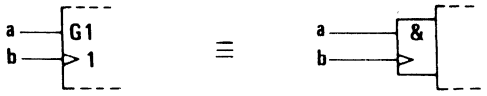


Figure 6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

> When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 4).

If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR relationship to each other (Figure 7).

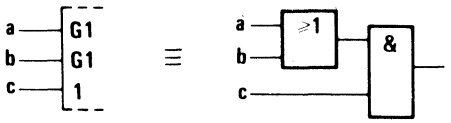


Figure 7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label

of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs may be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 8).

Figure 8. Substitution for Numbers

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 9),

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

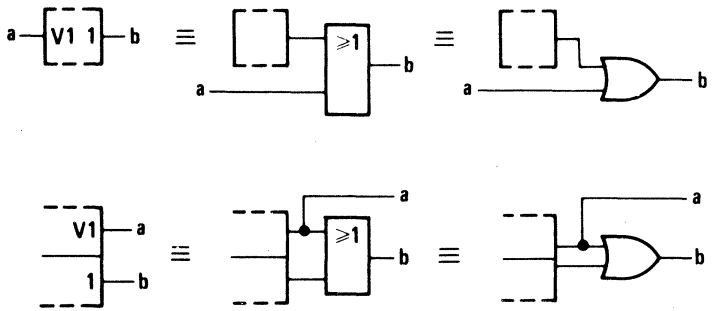
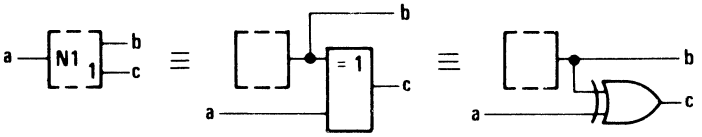


Figure 9. V (OR) Dependency

4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.



If a = 0, then c = b
If a = 1, then c = $\bar{b}$

Figure 10. N (Negate) (Exclusive-OR) Dependency

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 11).

4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 12).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 12, 13, and 14 are omitted.

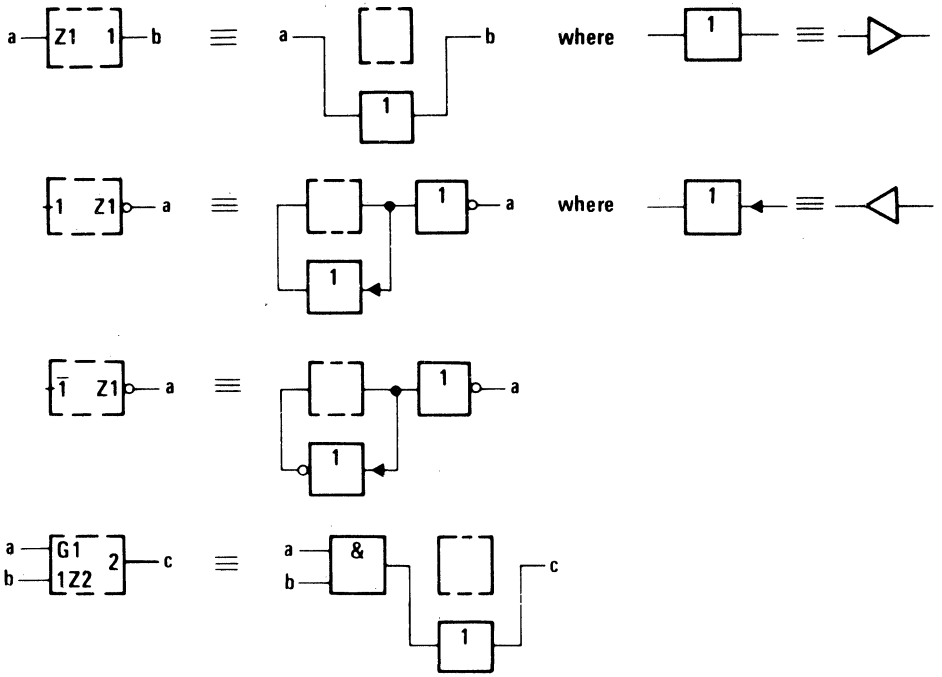
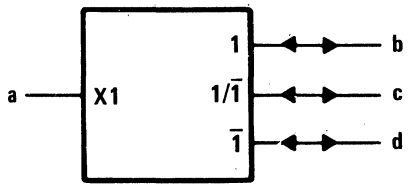


Figure 11. Z (Interconnection) Dependency



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 12. X (Transmission) Dependency

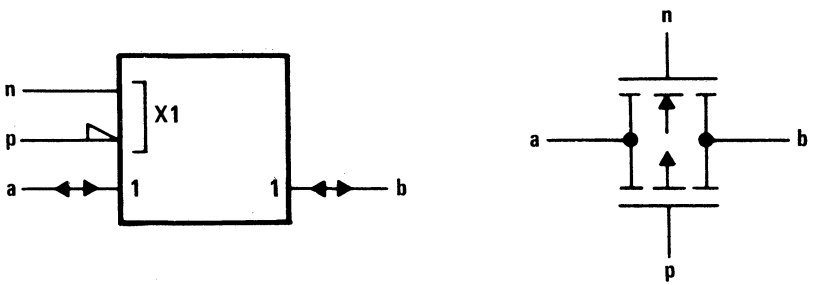


Figure 13. CMOS Transmission Gate Symbol and Schematic

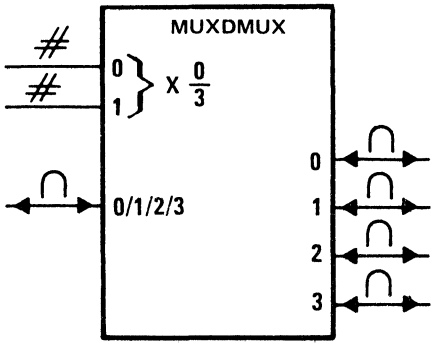


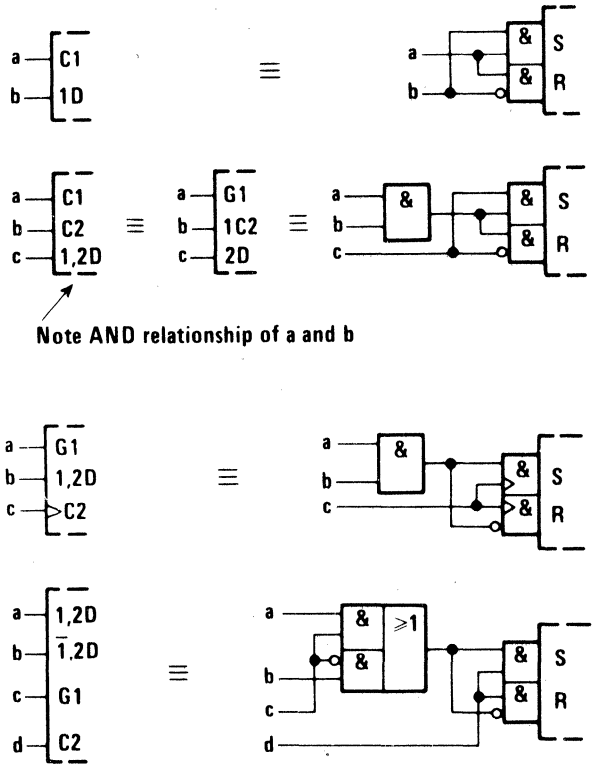
Figure 14. Analog Data Selector (Multiplexer/Demultiplexer)

4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case, the dynamic input symbol is used as shown in the third example of Figure 15.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element; i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.



Input c selects which of a or b is stored when d goes low.

Figure 15. C (Control) Dependency

4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 16 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

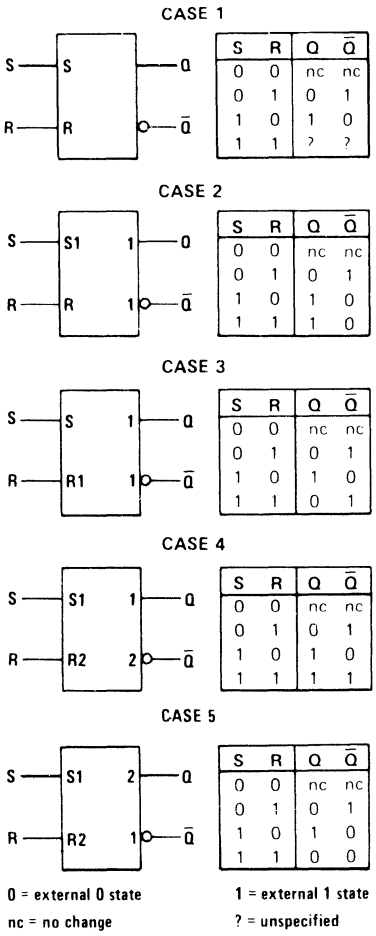
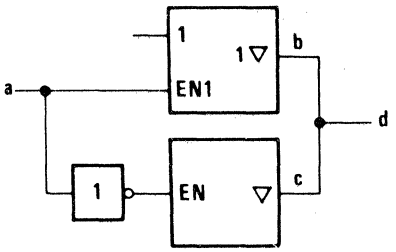


Figure 16. S (Set) and R (Reset) Dependencies

4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 17).



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

Figure 17. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element, and the outputs affected by this input stand at their normally defined internal logic states; i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

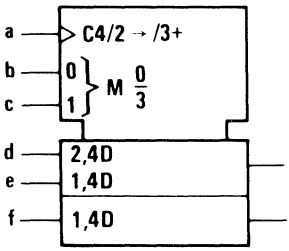
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 22).

4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element; i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d, e,** and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading), and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 18. M (Mode) Dependency Affecting Inputs

4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states; i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 19 shows a symbol for a device whose output can behave as either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state, and, in that case, the three-state symbol applies, and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect, and the open-element symbol applies.

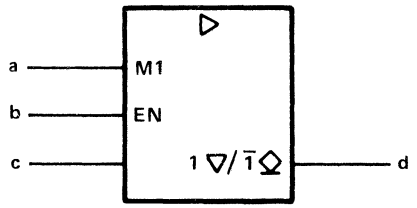


Figure 19. Type of Output Determined by Mode

In Figure 20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

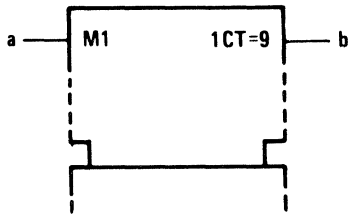


Figure 20. An Output of the Common-Control Block

In Figure 21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

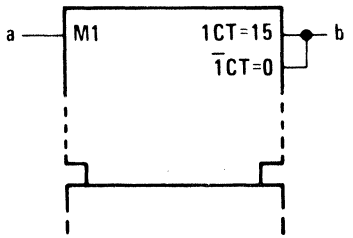


Figure 21. Determining an Output's Function

In Figure 22, inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

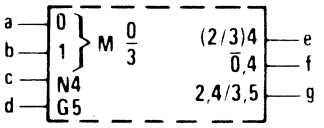


Figure 22. Dependent Relationships Affected by Mode

At output **e**, the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1, this output stands at its normally defined state as if it had no labels. At output **f**, the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0, the label set has no effect so the output stands at its normally defined state. In this example, $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g**, there are two label sets: the first set, causing negation (if **c** = 1), is effective only in mode 2; the second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

Figure 23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs; i.e., only those enabled by the active EN functions.

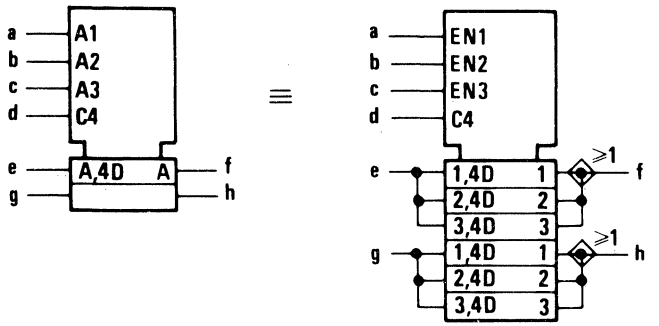


Figure 23. A (Address) Dependency

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency inputs (e.g., G, V, N, . . .), because, in the general section presented by the symbol, they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Since they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 24 is another illustration of the concept.

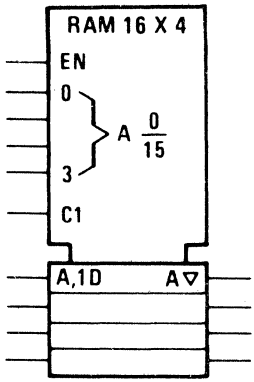


Figure 24. Array of 16 Sections of Four Transparent Latches with State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table 4. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 3.3.

5 Bistable Elements

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 25). The first column shows the essential distinguishing features; the other columns show examples.

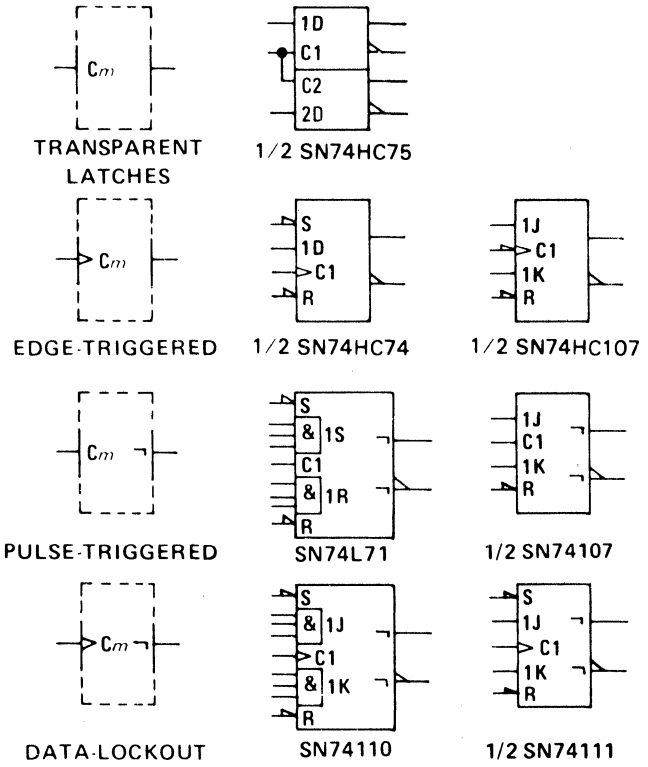


Figure 25. Four Types of Bistable Circuits

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lockout element is similar to the pulse-triggered version except that the C input is considered dynamic in that, shortly after C goes through its active transition, the data inputs are disabled, and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

6 Coders

The general symbol for a coder or code converter is shown in Figure 26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

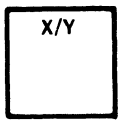


Figure 26. Coder General Symbol

Indication of code conversion is based on the following rule:

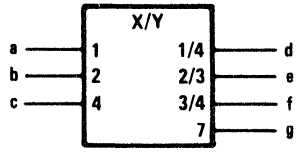
> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case, the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency



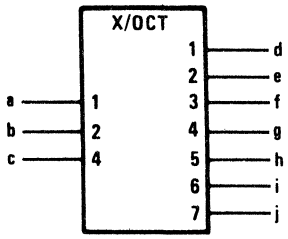
TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 27. An X/Y Code Converter

(see section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9=4/5/6/7/8/9) or by

2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 28.



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 28. An X/Octal Code Converter

Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.

7 Use of a Coder to Produce Affecting Inputs

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case, use can be made of the symbol for a coder as an embedded symbol (Figure 29).

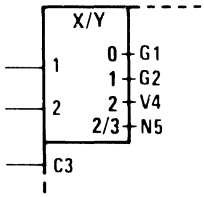


Figure 29. Producing Various Types of Dependencies

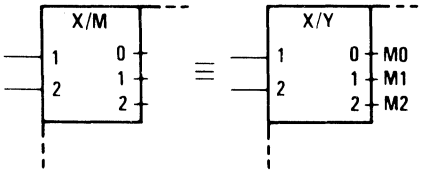


Figure 30. Producing One Type of Dependency

If all affecting inputs produced by a coder are of the same type as their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 30).

8 Use of Binary Grouping to Produce Affecting Inputs

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 31.

9 Sequence of Input Labels

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

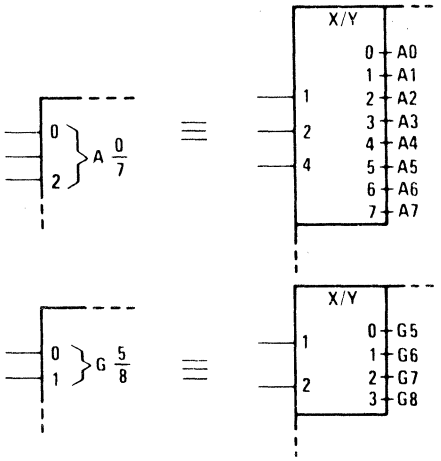


Figure 31. Use of the Binary Grouping Symbol

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases, the input may be shown once with the different sets of labels separated by solidi (Figure 32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed, and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 33).

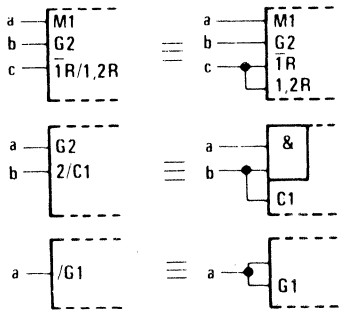


Figure 32. Input Labels

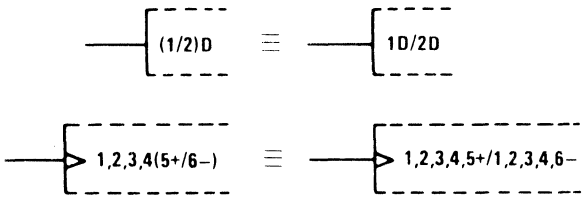


Figure 33. Factoring Input Labels

10 Sequence of Output Labels

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 34).

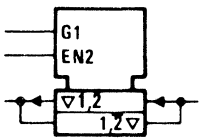


Figure 34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases, the output may be shown once with the different sets of labels separated by solidi (Figure 35).

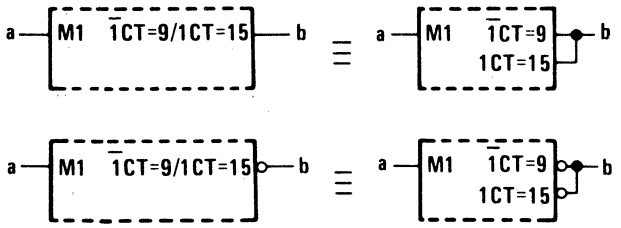


Figure 35. Output Labels

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 36).

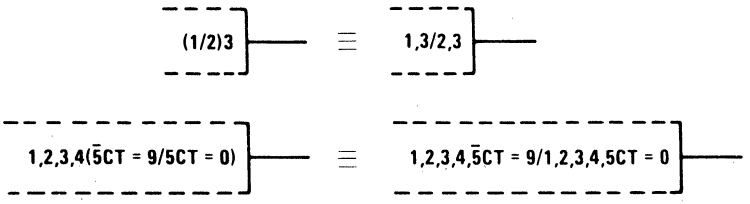


Figure 36. Factoring Output Labels

If you have questions on this Explantion of Logic Symbols, please contact:

Texas Instruments Incorporated
F.A. Mann, MS 3684
P.O. Box 655012
Dallas, Texas 75265

Telephone (214) 997-2489

IEEE Standards may be purchased from:

Institute of Electrical and Electronic Engineers, Inc.
IEEE Standards Office
445 Hoes Lane
P.O. Box 1331
Piscataway, N.J. 08855-1331

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

Contents

MECHANICAL DATA CROSS-REFERENCE

Table 1. Cache

DEVICE TYPE	PIN NO.	PACKAGE TYPE
SN74ACT2140A	52	FN
SN74ACT2150A	24	DW, JD, NT
SN74ACT2151/53	28	FN, N
SN74ACT2152A/54A	28	FN, N
SN74ACT2155	44	FN
SN74ACT2156	44	FN
SN74ACT2157	44	FN
SN74ACT2158/59	44	FN
SN74ACT2160	32	FM
SN74ACT2163/64	32	FM
SN74BCT2160	32	FM
SN74BCT2163/64/66	32	FM
TMS2150	24	DW, JD, NT

Table 2. Dynamic Memory Controller

DEVICE TYPE	PIN NO.	PACKAGE TYPE
SN74ACT4503	52	JD, N
	68	FN
SN74ALS6300	16	N
	24	DW
SN74ALS6301/02	52	JD, N
	68	FN
SN74ALS6310A/11A	20	DW, FN, N
THCT4502B	48	JD, N
	68	FN
TMS4500A	40	N
	44	FN

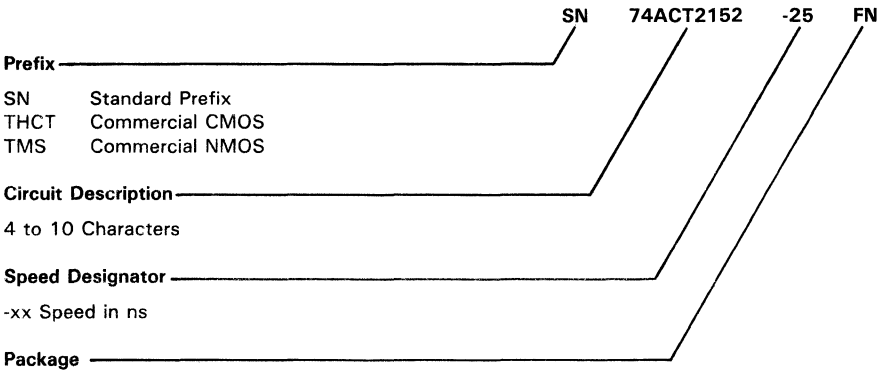
Table 3. Error Detection and Correction

DEVICE TYPE	PIN NO.	PACKAGE TYPE
SN74ALS632B	52	JD, N
	68	FN
SN74AS632	52	JD, N
	68	FN
SN74AS632A	52	JD, N
	68	FN
SN74AS6364	17 x 17	GA

Table 4. Supporting Products

DEVICE TYPE	PIN NO.	PACKAGE TYPE
SN74BCT2423/24	68	FN
SN74LS610/612	40	JD, N

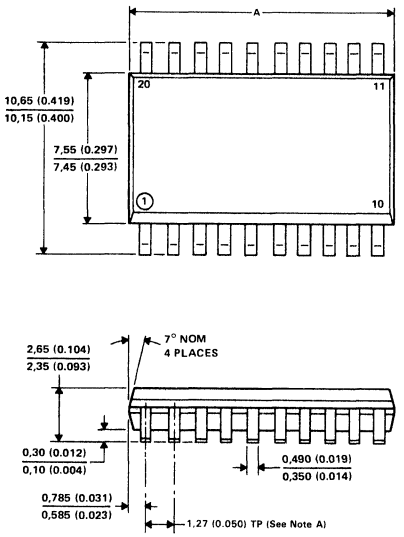
Factory orders for Cache Memory Management products described in this book should include a four-part type number as explained in the following example:

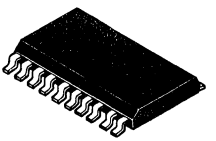


DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16 (0.400)	12,70 (0.500)	15,29 (0.602)	17,68 (0.696)
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.704)

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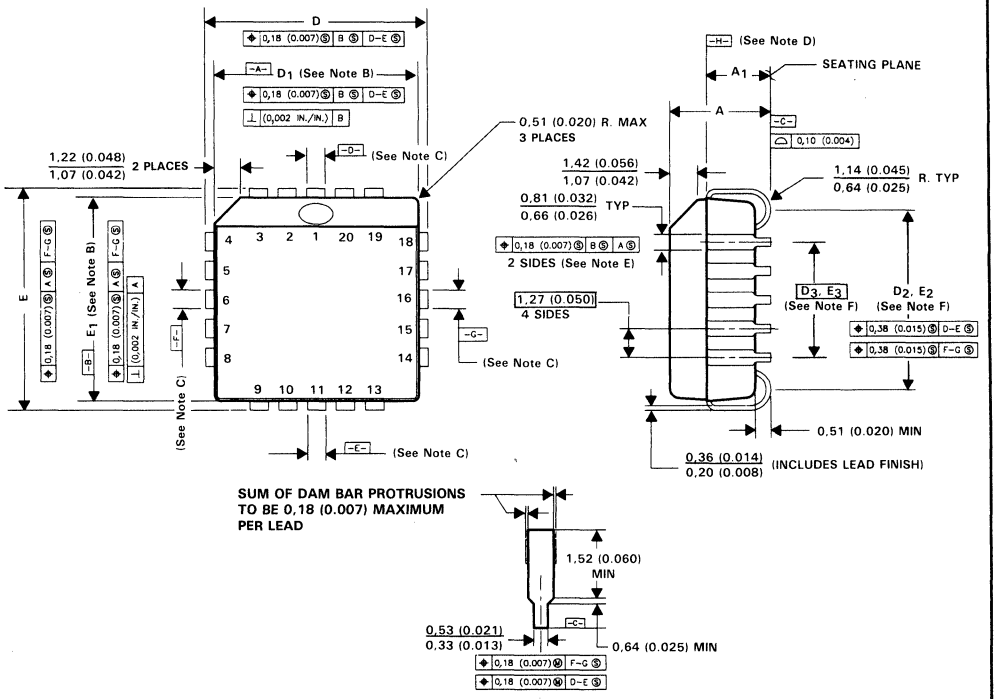
†The 28-pin package drawing is presently classified as Advance Information.

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FN020, FN028, FN044, FN052, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN052, FN068, and FN084
(20-terminal package used for illlustration)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

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FN020, FN028, FN044, FN052, FN068, and FN084 plastic chip carrier packages (continued)

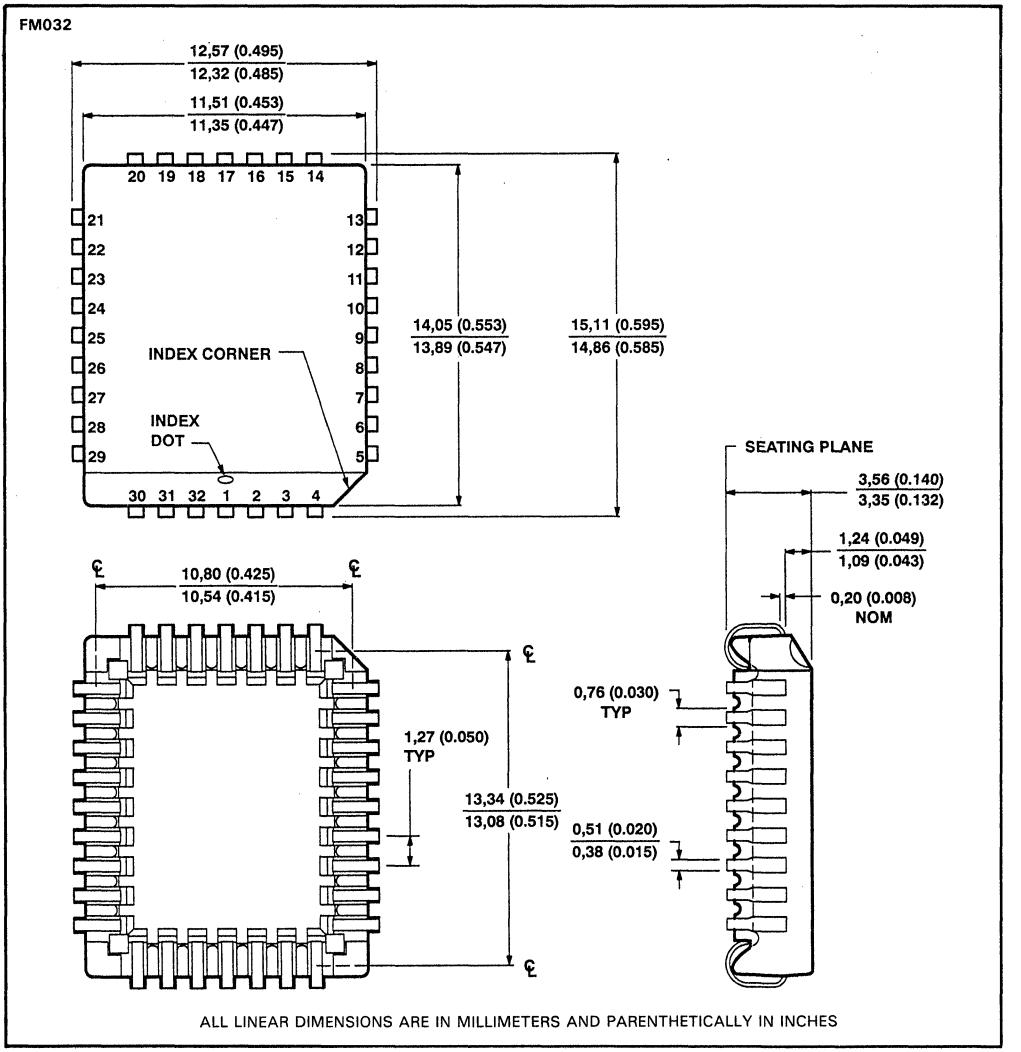
JEDEC OUTLINE	NO. OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2 (See Note F)		D_3, E_3 BASIC
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 (0.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)
MO-047AC	44	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	14,99 (0.590)	16,00 (0.630)	12,70 (0.500)
MO-047AD	52	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	19,94 (0.785)	20,19 (0.795)	19,05 (0.750)	19,20 (0.756)	17,53 (0.690)	18,54 (0.730)	15,24 (0.600)
MO-047AE	68	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.958)	22,61 (0.890)	23,62 (0.930)	20,32 (0.800)
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M–1982.

F. Determined at seating plane $\boxed{-C-}$

FM032 plastic lead chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



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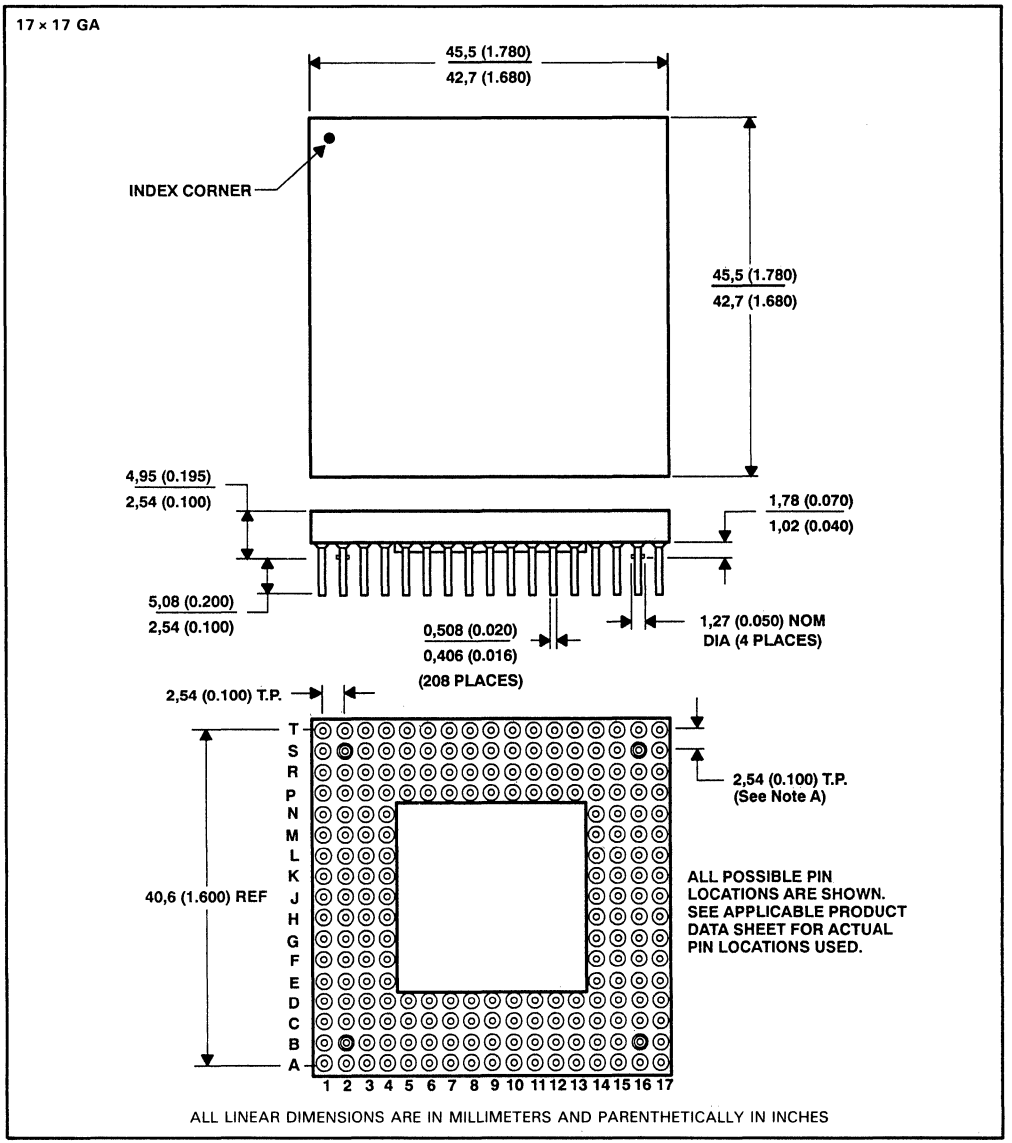
GA ceramic pin-grid-array package

This is a hermetically sealed package with metal cap and gold-plated pins.

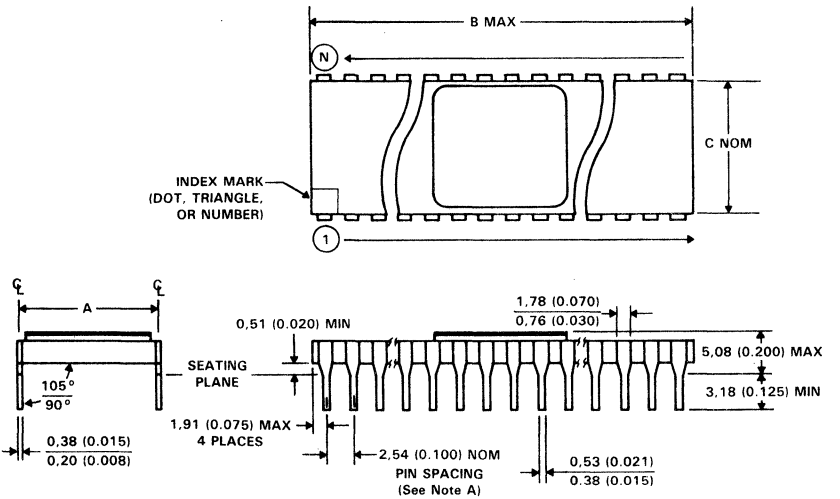


NOTE A: Pins are located within 0,13 (0.005) radius of true position relative to each other at maximum material condition and within 0,381 (0.015) radius relative to the center of the ceramic.

JD ceramic side-braze dual-in-line packages

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.

JD CERAMIC–SIDE-BRAZE



DIM \ PINS (N)	16	18	20	22	24
A +0,51 (+0.020) −0,25 (−0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)
B (MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)
C (NOM)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	9,91 (0.390)	7,37 (0.290)

DIM \ PINS (N)	24	28	40	48	52	64
A +0,51 (+0.020) −0,25 (−0.010)	15,24 (0,600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B (MAX)	31,8 (1.250)	36,8 (1,450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C (NOM)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	15,0 (0.590)	22,6 (0.890)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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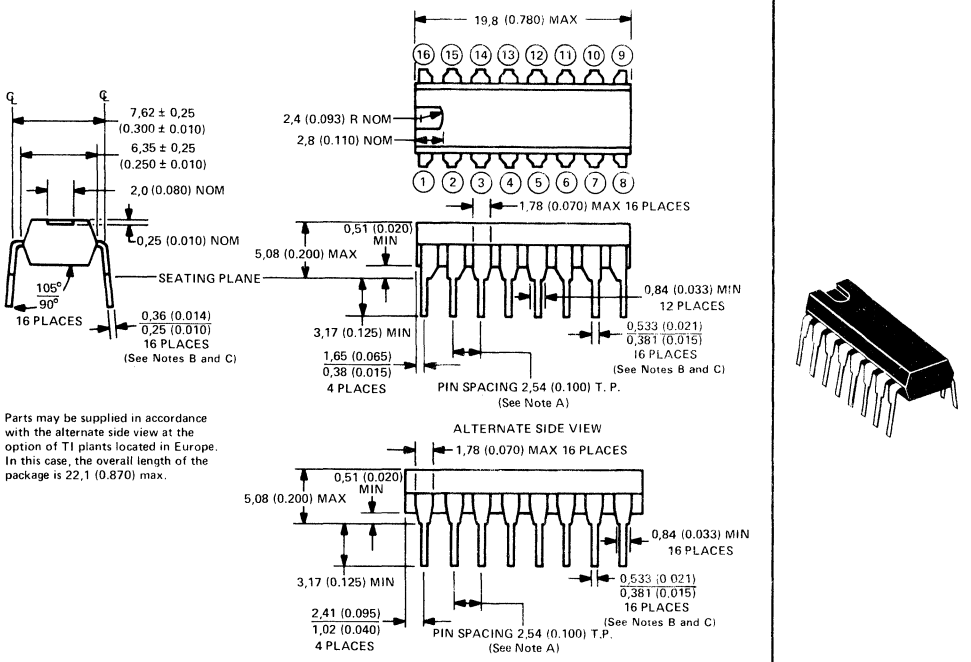
N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016

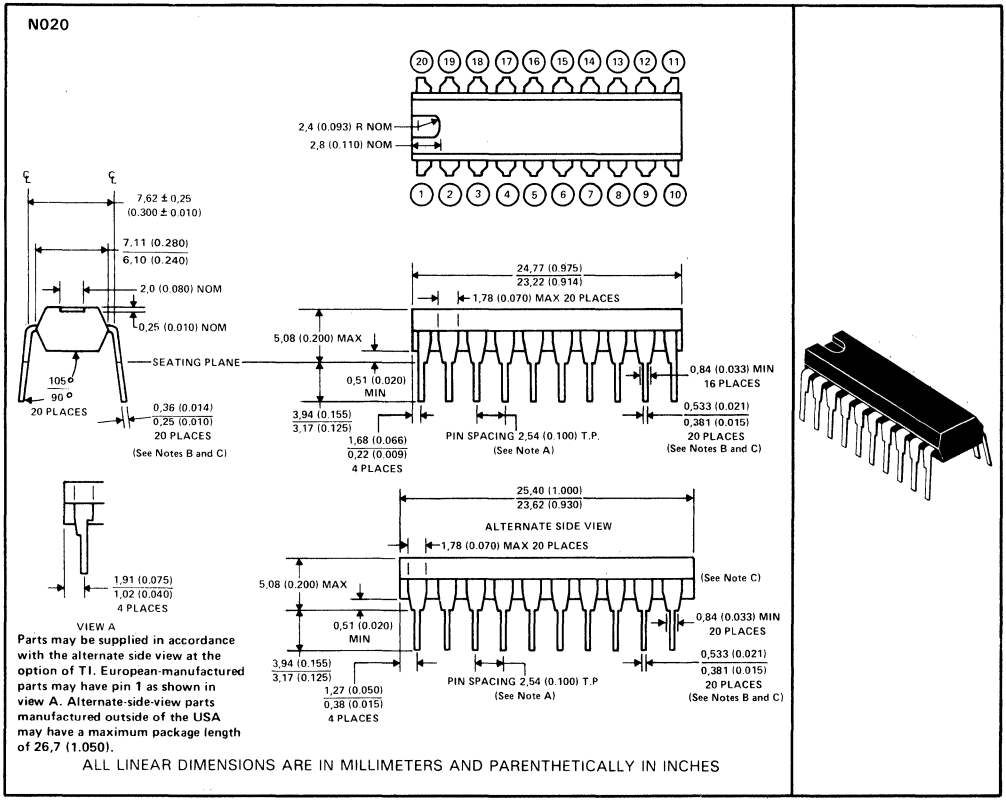


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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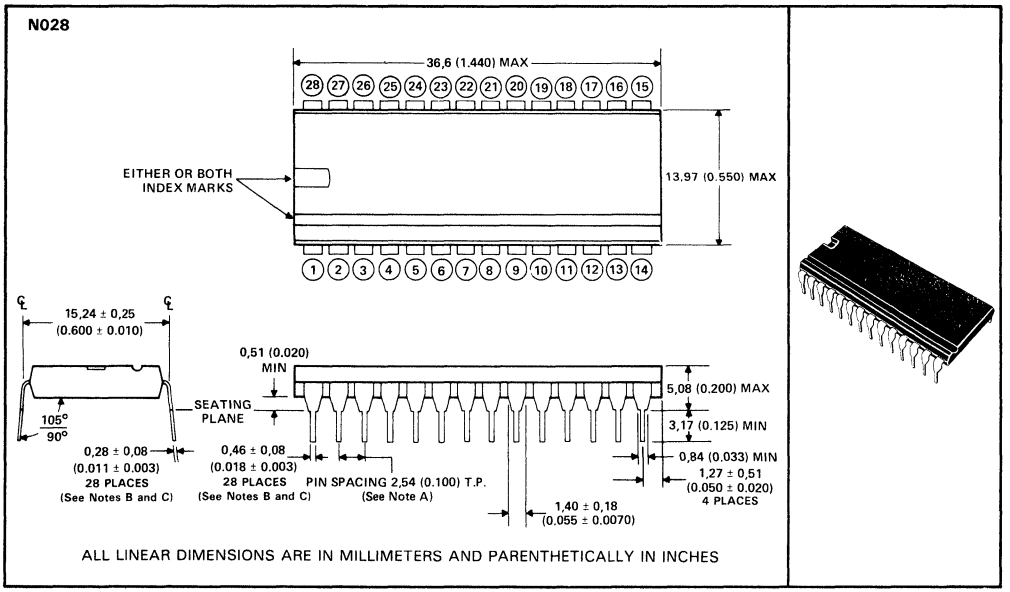
N028 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

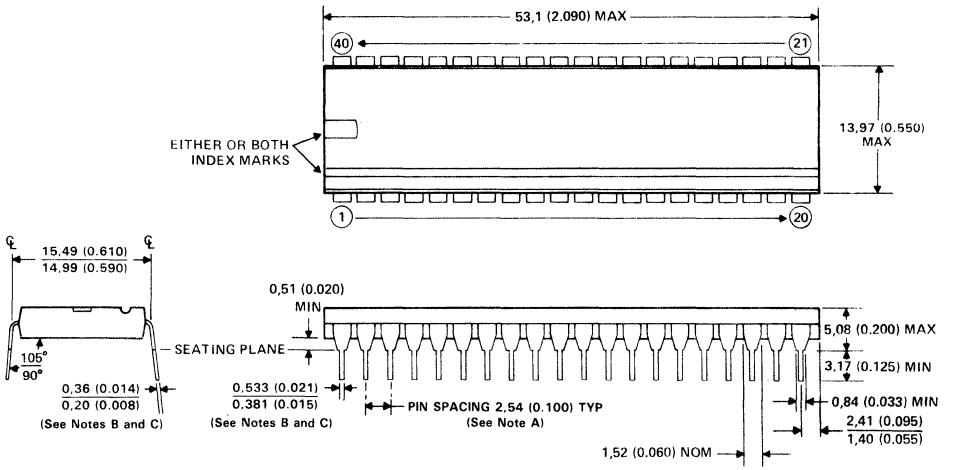


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N040 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows typically on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

40-PIN N PLASTIC



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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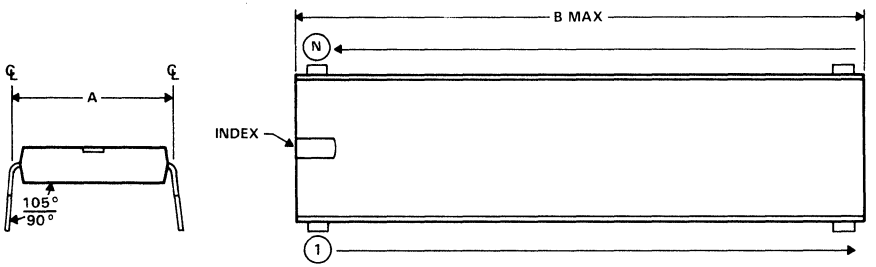
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

N048, N052, and N064 plastic dual-in-line package

These dual-in-line packages consist of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 15,24 (0.600), 15,24 (0.600), and 22,86 (0.900) centers for the N048, N052, and N064, packages respectively. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



PIN SPACING 2,54 (0.100) TYP
(See Note A)

DIM \ PINS (N)	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

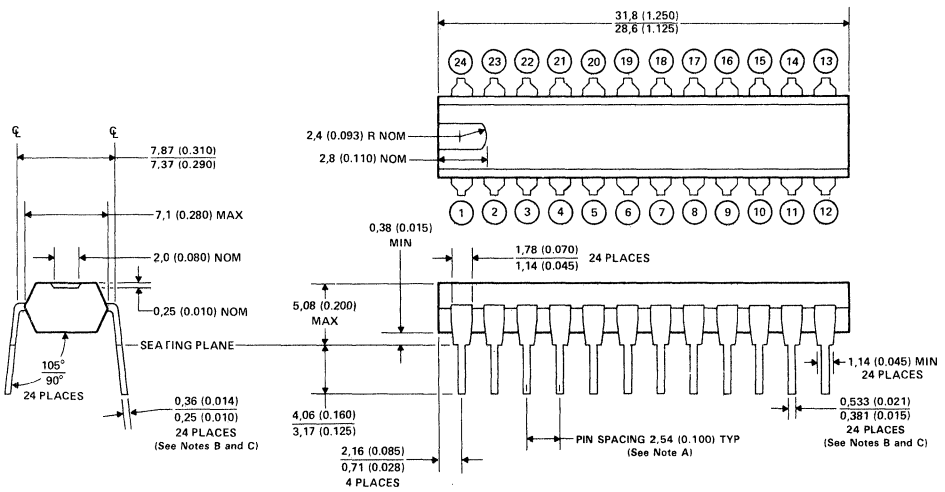
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

INTRODUCTION

Texas Instruments has developed solutions for today's high density packaging needs. The TI facility at Attleboro, Massachusetts (one of the world's largest suppliers of multimetal systems) provides leading-edge technology which, combined with reliable, high-volume, off-the-shelf interconnection products, allows TI to quickly meet volume commercial applications.

During the last decade, TI has produced one of the largest IC socket families. TI's sockets include every type and size socket in common use today and are available in a wide choice of contact materials and designs.

Our sockets are designed for:

- easy and efficient hand assembly
- compatibility with automatic assembly equipment
- maximum performance and board density

This section provides information on the following types of IC socket products.

PRODUCTION SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Single-In-Line Packages	SIP
Pin-Grid Arrays	PGA
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Quad-In-Line	QUIP

BURN-IN/TEST SOCKETS	TYPE
Plastic Leaded Chip Carrier	PLCC
Pin Grid Array	PGA
Small Outlilne	J Lead
Dual-In-Line	DIP
Dual-In-Line 0.070-inch spacing	Shrink Pack
Small Outline	Flat Pack
Quad	Flat Pack

Specially formulated alloys give the TI contact springs:

- Low Contact Resistance
- High Contact Strength (to stand up to repetitive insertions and withdrawals)
- High normal forces assure gas-tight reliability

A full line of reliable, readily available, low-cost interconnection systems means premium performance at an economical price.

Additional information on these and other TI products, including pricing and delivery quotations, may be obtained from your nearest authorized TI Distributor, TI Sales Representative or:

Texas Instruments Incorporated
Connector Systems Department, MS 14-3
Attleboro, Massachusetts 02703
Telephone: (508) 699-5345
TELEX: 92-7708

IC SOCKETS
PLASTIC LEADED CHIP CARRIER

PERFORMANCE SPECIFICATIONS

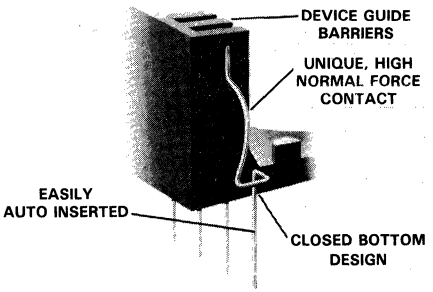
Mechanical
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Vibration: 15 G max
Shock: 100 G max
Insertion force: 0.59 lbs per position typ
Withdrawal force: 0.25 lbs per position typ
Normal force: 200 g min, 450 g typ
Wipe: 0.075 in min
Durability: 5 cycles min
Contact retention: 1.5 lbs min

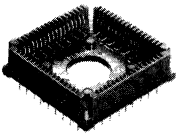
Electrical
Current carrying capacity: 1 A per contact
Insulation resistance: 5000 MΩ min
Dielectric withstanding voltage: 1000 V ac rms min
Capacitance: 1 pF max

Environmental
Operating temperature:
Operating: – 40°C to 85°C
Storage: –40°C to 95°C
Temperature cycling with humidity: will conform to final EIA specifications

MATERIALS
Body – Ryton R-4 (40% glass) UL 94 V-0 rating
Contacts – CDA 510 spring temper
Contact finish – 90/10 tin/lead (200 μin –400 μin) over 40 μin copper

Extraction tool available, consult factory
Contact factory for detailed information



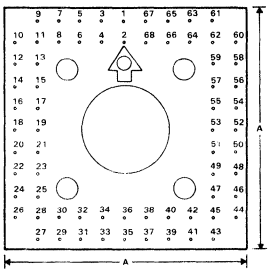


PART NUMBER SYSTEM

CPR PH XXX – X – X – O

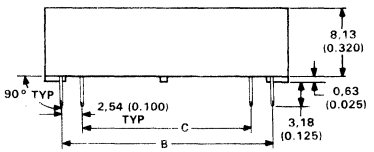
- O: Contact surface 1 – tin/lead plating
- X: Contact spacing 1 - 0.050 in
- XXX: Number of pos (044, 052, 068, 084)
- PH: Plated thru hole, solder tail
- CPR: TI socket Series, Plastic leaded chip carrier

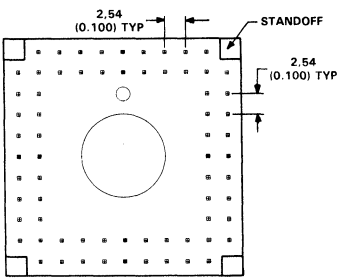
PLASTIC LEADED CHIP CARRIER CPR SERIES



68-Pin shown

NOTE: Socket electrical pin-out pattern represents component side of P.C.B. layout. (TYP. counter clockwise numbering pin-out system.)





Pos	A	B	C
44	21,43 (0.844)	17,78 (0.700)	12,70 (0.500)
52	23,98 (0.944)	20,32 (0.800)	15,24 (0.600)
68	29,06 (1.144)	25,40 (1.000)	20,32 (0.800)
84	34,14 (1.344)	30,48 (1.200)	25,40 (1.000)

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PRODUCT FEATURES

Can be loaded by top actuated insertion or press-in insertion, either manually or automatically
High reliability due to high pressure contact point
Open,body and high stand-off design provide high efficiency in heat dissipation
High durability up to 10,000 cycles
Compact design

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles 10 mΩ max contact resistance change
Insertion force: Zero g
Withdrawal force: Zero g†

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 500 V ac rms per MIL-STD 202, Method 301

Environmental

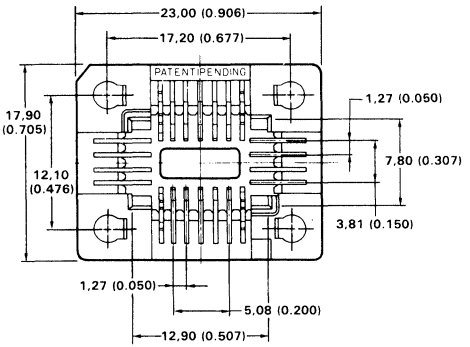
Thermal shock: 100 cycles, −25°C to +150°C
Temperature soak: 150°C for 48 hours
Operating temperature: −40°C to +150°C

MATERIALS

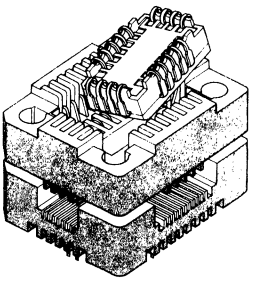
Body — ULTEM glass filled (UL 94 V-0)
Contact — copper alloy
Plating‡ — overall gold plate 4 μin over min 70 μin nickel plating

†After IC is unlocked from the socket
‡For additional plating options contact factory
For complete test report contact the factory

PLCC BURN-IN/TEST SOCKETS CPJ SERIES



Dimensions in parentheses are inches
Contact factory for detailed information

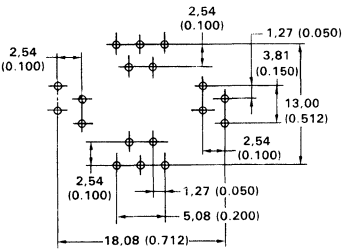


PART NUMBER SYSTEM

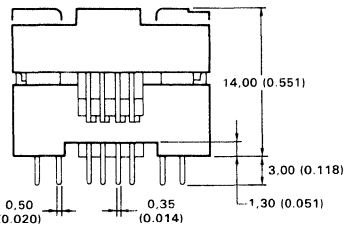
CPJ XX XX X – XXX – B

- CPJ: TI Burn-in PLCC series
- XX: Material — AA = copper alloy
- XX: Contact finish — 33 = overall gold plate
- X: Pitch — A = 0.050
- XXX: Number of contacts
- B

18 PIN FOOTPRINT SHOWN



SIZES: 18 PIN
22 PIN



PERFORMANCE SPECIFICATIONS†

Mechanical
Vibration: MIL-STD-202
Durability: 30 cycles
Insertion force: Zero g
Withdrawal force: Zero g‡
Contact (normal) force: 200 g min
Contact retention force: 2 lbs per circuit min

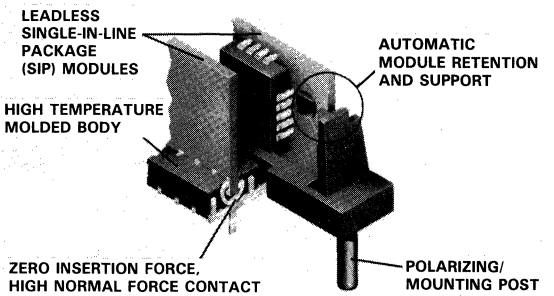
Electrical
Contact rating: 1 A
Contact resistance: 30 mΩ max initial
Insulation resistance: 1000 MΩ at 500 dc
Dielectric strength: 1500 V ac rms
Capacitance: 2 pF max

†Values may vary due to test sequence and SIP module configuration
‡After module is unlocked from the receptacle
For a complete test report, please contact factory

Environmental
(20 mΩ max contact resistance change after all tests)
Operating and storage temperature: −40°C to 100°C
Humidity: MIL-STD 202, Method 106D, 10 days
Temperature soak: 85°C for 160 hours
Thermal Shock: 5 cycles, −40°C to 85°C per MIL-STD 202, Method 107E

MATERIALS
Body — PES polyether sulfone, glass filled, UL 94 V-0
Contact — Beryllium copper C17000; phosphor bronze alloy CA510
Contact finishes — Post plate min 200 µin tin/lead over min 50µin nickel overall
Post plate min 30 µin hard gold over min 75 µin nickel overall

For additional plating options contact the factory.



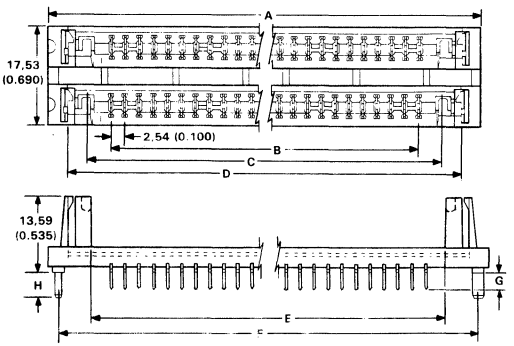
PART NUMBER SYSTEM

TS8X XX XX X −XX − XX

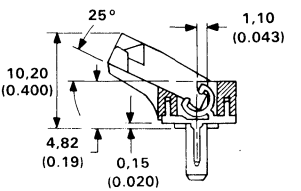
- XX (last): Variations
  00 — standard product
- −XX: Size (number of contacts per row)
- X: Housing material
  A — PES
- XX: Contact base material/plating
  01—C17000/30 µin gold
  02—CA510/30 µin gold
  03—C17000/200 µin tin/lead
  04—CA510/200 µin tin/lead
- XX: Configuration/row-to-row spacing
  01—single row/N/A
  03—dual row/0.300 in
  04—dual row/0.400 in
  05—dual row/0.500 in
- TS8X: Series number denotes
  0—0.100 in pitch, vertical mount
  1—0.100 in pitch, low-profile (25°) mount

Consult factory for availability of configurations, materials, and sizes.

DUAL ROW VERTICAL



SINGLE ROW LOW PROFILE



Ckt Size	A	B	C	D	E	F	G	H
30	96,52 (3.800)	73,66 (2.900)	82,14 (3.234)	89,28 (3.515)	80,52 (3.170)	92,71 (3.650)	2,79 (0.110)	3,86 (0.152)

Contact factory for detailed information

Dimensions in parentheses are in inches

TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.015 in to 0.021 in diameter
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.002 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force: 3.6 oz (102 g) per pin typ using 0.018 in diameter test pin
Withdrawal force: 0.5 oz (14 g) per pin min using 0.018 in diameter test pin

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

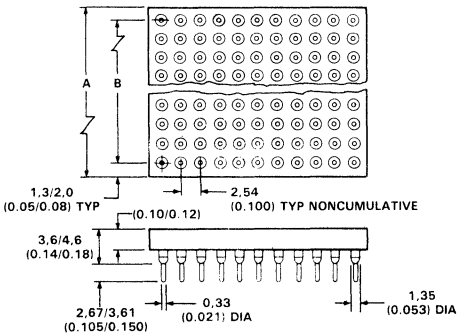
Environmental

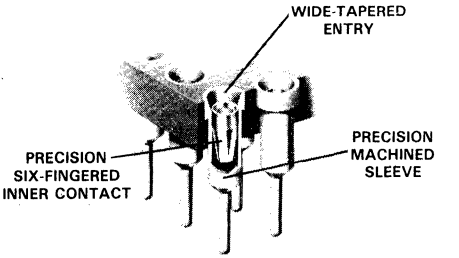
Operating temperature: −65°C to 125°C, gold; −40°C to 100°C, tin/lead
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — PBT polyester UL 94 V-0
On request, G10/FR4 or Mylar film
Outer sleeve — Machined Brass (QQ-B-626)
Inner contact — Beryllium copper (QQ-C-530) heat treated
Plating: (specified by part number)

PIN GRID ARRAY





Inner contact — 30 μin gold over 50 μin nickel or 100 μin tin/lead over 50 μin nickel
Outer sleeve — 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel

PART NUMBER SYSTEM

C X G XX – XXX X X – X X

- C — TI Socket
- X — BODY MATERIAL: G — Glass Filled Epoxy; P — PBT Polyester
- G — Pin Grid Array
- XX — Overall Grid Size: 5×5=05 to 18×18=18
- XXX — Number of Pins: 024 to 324
- X — Contact Loading Pattern
- X — Body Style and Orientation

P/N	Sleeve	Clip
0	Gold	Gold
5	Tin	Gold

- X — Plating

WIRE WRAP	SOLDER TAIL
3-0.510 long	9-0.105/0.150

- X — Pin Length

Insulator Size	A ±0.010	B ±0.005†
9×9	(0.950) 24,13	(0.800) 20,32
10×10	(1.050) 26,67	(0.900) 22,86
11×11	(1.150) 29,21	(1.000) 25,40
12×12	(1.250) 31,75	(1.100) 27,94
13×13	(1.350) 34,29	(1.200) 30,48
14×14	(1.450) 36,83	(1.300) 33,02
15×15	(1.550) 39,37	(1.400) 35,56
16×16	(1.650) 41,91	(1.500) 38,10
17×17	(1.750) 44,45	(1.600) 40,64
18×18	(1.850) 46,99	(1.700) 43,18

†Noncumulative
Dimensions in parentheses are inches
Consult factory for detailed information

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 10,000 cycles, 20 mΩ max contact resistance change
Insertion force: 1.3 oz per position max
Withdrawal force: 8.8 grams per position min

Electrical

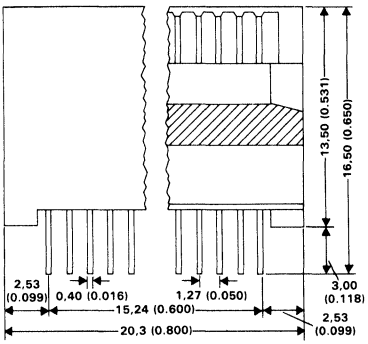
Contact rating: 1.0 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ per MIL-STD 202, Method 302, Condition B
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 202, Method 301

Environmental

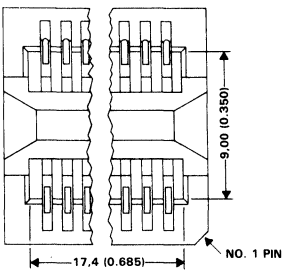
Thermal shock: 100 cycles, −25°C to +180°C, 1 hour
Temperature soak: 180°C for 1000 hours, 80 mΩ max change
Operating temperature: −65°C to +180°C

MATERIALS

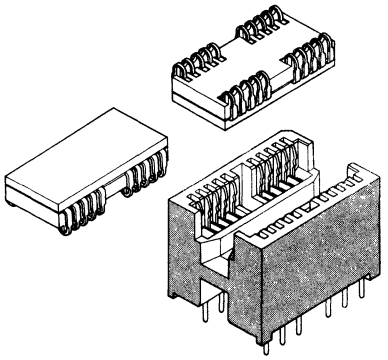
Body — PES glass filled UL 94 V-0
Contact — copper alloy
Plating — overall gold plate min 4 μin over min 70 μin nickel plating



02 VERSION SHOWN



Dimensions in parentheses are inches
Contact factory for detailed information



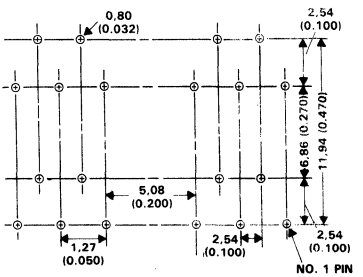
PART NUMBER SYSTEM

CSJT XXX – XX – XX X

- CSJT — TI SOJ series
- XXX — Number of Contacts
- XX — Contact Finish
  - 37 = Overall gold plate 4 μin
  - 38 = Overall gold plate 30 μin
  - 57 = Selective gold plate 4 μin
  - 58 = Selective gold plate 30 μin
- XX — Body Variation
  - 02 = Standard 1 forward/backward insertion
  - 03 = Special/orientation pin
  - 04 = Special/high standoff
  - 05 = Special/24-pin
  - 06 = Standard 2 forward insertion, BECU
- X — Body Material
  - Blank = G.F. PES
  - A = PPS R4-03
  - B = G.F. PEI

SIZES: 20 pin
26 pin

20-PIN (02 VERSION) FOOTPRINT SHOWN



TEXAS INSTRUMENTS
34 Forest Street • Attleboro, Massachusetts 02703

PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 ± 0.003 in by 0.018 ± 0.003
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Recommended hole grid pattern: 0.100 in ± 0.003 in each direction
Vibration: 15 G, 10-2000 Hz per MIL-STD 1344A, Method 2005.1 Test Condition III.
Shock: 100 G, sawtooth waveform, 2 shocks each direction per MIL-STD 202, Method 213, Test Condition I
Durability: 5 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016
Insertion force (C7X and C86): 16 oz (454 g) per pin max
Withdrawal force: (40 g) per pin min

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc per MIL-STD 1344, Method 3003
Dielectric withstanding voltage: 1000 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

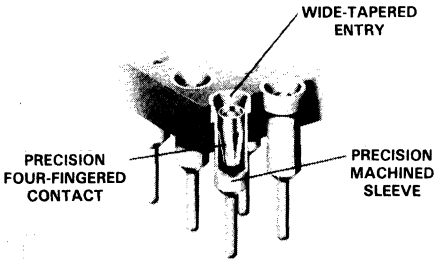
Environmental

Operating temperature: −55°C to 125°C, gold; −40°C to 100°C, tin
Corrosive atmosphere: 10 mΩ max contact resistance change when exposed to 22% ammonium sulfide for 4 hours
Gas tight: 10 mΩ max contact resistance change when exposed to nitric acid vapor for 1 hour
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

Materials (C7X and C86)

Body — PBT polyester UL 94 V-0
C7X Contacts — Outer sleeve: brass
Clip: BECU
Contact finish — clip 30 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
Specified by Part Number — sleeve 10 μin gold over 50 μin nickel or 50 μin tin/lead over 50 μin nickel
C86 Contacts — Phosphor bronze base metal
C86 Contact-finish — Tin plate 200 μin over copper flash

C7X SERIES — SCREW MACHINE

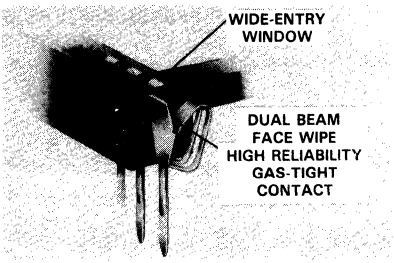


C7X SERIES — SCREW MACHINE PART NUMBER SYSTEM

C7X (X) XX − X X

- C7X: Screw Machine Socket
  - 1 — wire wrap
  - 2 — solder tail
- (X): S — Single-in-line package (where applicable)
- XX: Number of Positions
- X: Plating (Sleeve/Clip)
  - 0 — Gold/Gold
  - 5 — Tin/Gold
- X: Variations
  - Solder Tail : 9 Pin length 0.125 Typ
  - Wire Wrap : 3 Pin length 0.510

C86 SERIES — STAMPED AND FORMED

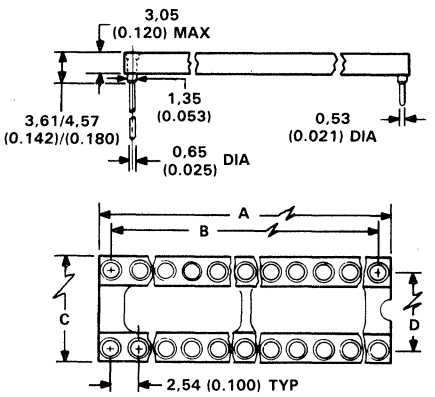


C86 SERIES PART NUMBER SYSTEM

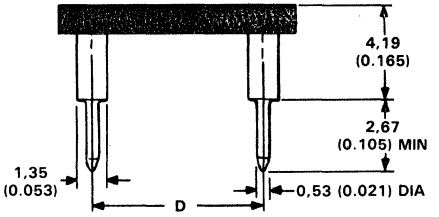
C 86 XX − 01

- C: TI Socket Series
- 86: Tin Dual Beam Face Wipe
- XX: Number of positions
- 01: Variation
  - 01 — Standard product

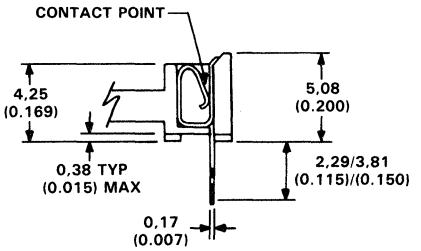
DUAL-IN-LINE
C7X AND C86 SERIES



C7X SERIES



C86 SERIES



DIPS

Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005	Positions	Dim A Max	Dim B ±0.005	Dim C Max	Dim D ±0.005
6	7,62 (0.300)	5,08 (0.200)	10,16 (0.400)	7,62 (0.300)	†24	30,48 (1.200)	27,94 (1.100)	12,76 (0.500)	10,16 (0.400)
8	10,16 (0.400)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	28	35,56 (1.400)	33,02 (1.300)	17,78 (0.700)	15,24 (0.600)
14	17,78 (0.700)	15,24 (0.600)	10,16 (0.400)	7,62 (0.300)	32	40,64 (1.600)	38,10 (1.500)	17,78 (0.700)	15,24 (0.600)
16	20,32 (0.800)	17,78 (0.700)	10,16 (0.400)	7,62 (0.300)	34	45,72 (1.800)	43,18 (1.700)	17,78 (0.700)	15,24 (0.600)
18	22,86 (0.900)	20,32 (0.800)	10,16 (0.400)	7,62 (0.300)	40	50,80 (2.000)	48,26 (1.900)	17,78 (0.700)	15,24 (0.600)
20	25,40 (1.000)	22,86 (0.900)	10,16 (0.400)	7,62 (0.300)	48	60,96 (2.400)	58,42 (2.300)	17,78 (0.700)	15,24 (0.600)
22	27,94 (1.100)	25,40 (1.000)	12,76 (0.500)	10,16 (0.400)	50	63,50 (2.500)	60,96 (2.400)	25,40 (1.000)	7,62 (0.900)
24	30,48 (1.200)	27,94 (1.100)	17,78 (0.700)	15,24 (0.600)	64	81,28 (3.200)	78,74 (3.100)	25,40 (1.000)	22,86 (0.900)
†24	30,48 (1.200)	27,94 (1.100)	10,16 (0.400)	7,62 (0.300)					

†Nonstandard sizes
Not all sizes available in each series
Dimensions apply to all series

Dimensions in parentheses are inches
Contact factory for detailed information

TEXAS INSTRUMENTS
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PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads 0.011 in by 0.018 in
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hold size range: 0.032 in to 0.042 in
Durability: 10K cycles – CM Series, 5K cycles – CP/CQ

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1000 MΩ at 500 V dc
Dielectric withstanding voltage: 1000 V ac rms
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

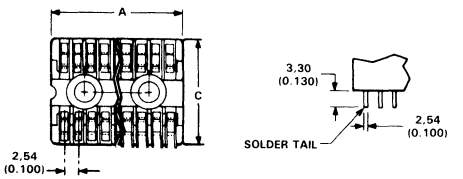
Operating temperature: –65°C to 170°C – CP/CM Series,
–65°C to 150°C – CQ Series
Humidity: 10 mΩ max contact resistance
Temperature Soak: 10 mΩ max contact resistance change

MATERIALS

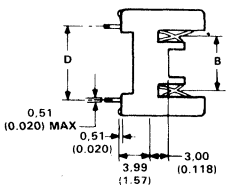
Body – PPS (polyphenylen sulfide) UL 94 V-0
Contacts – Higher performance copper nickel alloy
Plating:† 4 μin of gold min over 100 μin of nickel min

†For additional plating options consult the factory

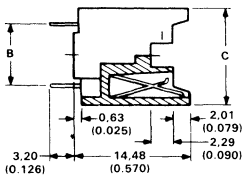
BURN-IN/TEST DIP SOCKETS



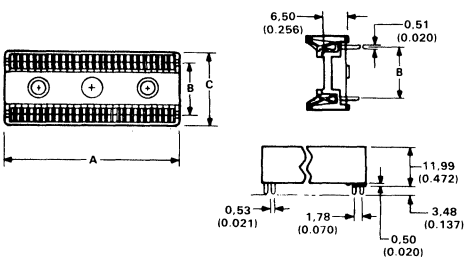
CQ37 SERIES



CP37 SERIES



CM37 SERIES



PART NUMBER SYSTEM

C X 37 XX – 22 S X

- C X: TI Socket Series
- 37: Series Features
  - Q – Auto unloadable
  - P – High density mounting
  - M – Shrink 0.070 centers
- XX: Overall gold plate
- 22: Number of positions
- S: Copper nickel alloy Soldertail
- X: PPS high temperature body material
- Pin to pin
  - A – 0.100 centers
  - B – 0.070 centers

CQ37 SERIES

Number of Positions	A ±0.01 Length	D ±0.02	C ±0.01 Width	B ±0.01 Contact
14	20,32 (0.800)			
16	22,35 (0.880)	12,70	15,24	7,62
18	24,89 (0.980)	(0.500)	(0.600)	(0.300)
20	27,43 (1.080)			
24	32,51 (1,280)			
28	37,59 (1.480)	19,05	22,86	15,24
40	52,83 (2.080)	(0.750)	(0.900)	(0.600)
42	55,37 (2.180)			

CP37 SERIES

Number of Positions	A max Length	B ±0.02	C max Width
8	11,68 (0.460)		
14	17,78 (0.700)		
16	20,32 (0.800)	7,62	12,70
18	22,86 (0.900)	(0.300)	(0.500)
20	25,40 (1.000)		
24	30,48 (1.200)		
28	35,56 (1.400)	15,24	20,32
40	50,80 (2.000)	(0.600)	(0.800)

CM37 SERIES

Number of Positions	A ±0.016 Length	B ±0.02	C ±0.016 Width
28	27,18 (1.070)	10,67 (0.420)	17,20 (0.677)
40	37,85 (1.490)		
42	39,62 (1.560)	16,51 (0.650)	23,11 (0.910)
54	50,29 (1.980)		
64	59,18 (2.330)	20,32 (0.800)	26,92 (1.060)

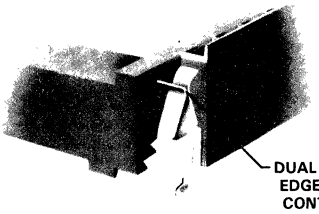
Dimensions in parentheses are inches
Contact factory for detailed information

PERFORMANCE SPECIFICATIONS

Insertion force: 16 oz (454 g) per pin max
Withdrawal force: 1.5 oz (42 g) per pin min
Operating temperature: −40°C to 100°C, tin/lead
Accommodates IC leads 0.011 ± 0.0003 in by 0.018 ± 0.003 in
Contact rating: 1 A per contact

MATERIALS

Body — PBT polyester UL 94 V-0
C4S & CxW Contacts — Copper alloy
Contact finish — Reflow tin plating, 40 µin min



PART NUMBER SYSTEM FOR CxW SERIES

C X W XX − 11

- XX: Number of contacts (42, 52, 64)
- W: Staggered leads
- X: 5 — 64 contacts; 6 — 42, 52 contacts
- C: TI Socket Series

QUAD-IN-LINE (CxW SERIES)

Product Number	A Max Length	B Row to Row	C Max Row to Row
C5W64-11	41,90 (1.65)	22,90 (0.950)	19,05 (0.750)
C6W42-11	27,90 (1.10)	22,90 (0.900)	17,80 (0.700)
C6W52-11	34,30 (1.35)	22,90 (0.900)	17,80 (0.700)

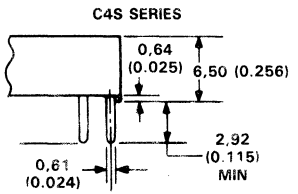
Dimensions in parentheses are inches
Contact factory for detailed information

PART NUMBER SYSTEM† FOR C4S SERIES

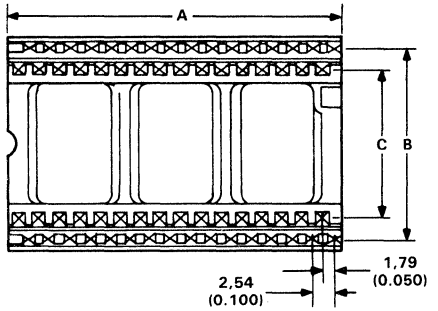
C 4 S XX − 02

- XX: Number of contacts 28, 40, 42, 52, 54, 64
- S: Shrink Pack (0.070 in pin-to-pin contact spacing)
- 4: Reflow tin plating
- C: TI Socket Series

†Also available in screw machine contacts



QUAD-IN-LINE (CxW SERIES)

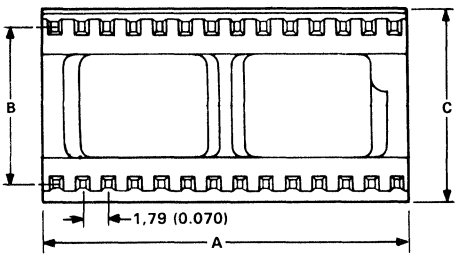


C4S SERIES

Positions	A Max Length	B Row to Row	C Max Width
28	25,02 (0.985)	10,16 (0.400)	13,00 (0.512)
40	35,69 (1.405)	15,24 (0.600)	17,98 (0.708)
64	57,07 (2.247)	19,05 (0.750)	21,62 (0.851)

Dimensions in parentheses are inches

SHRINK PACK DIP (C4S SERIES)



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PERFORMANCE SPECIFICATIONS

Mechanical

Accommodates IC leads per specific IC device
Recommended PCB thickness range: 0.062 in to 0.092 in
Recommended PCB hole size range: 0.032 in to 0.042 in
Durability: 5000 cycles, 10 mΩ max contact resistance change per MIL-STD 1344, Method 2016

Electrical

Contact rating: 1 A per contact
Contact resistance: 20 mΩ max initial
Insulation resistance: 1 MΩ at 500 V dc per MIL-STD 1344, Method 3003.1
Dielectric withstanding voltage: 700 V ac rms per MIL-STD 1344, Method 3001.1
Capacitance: 1 pF max per MIL-STD 202, Method 305

Environmental

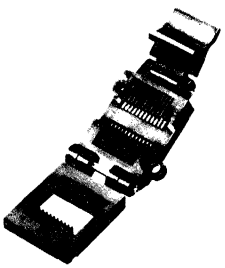
Operating temperature: −65°C to 170°C
Humidity: 10 mΩ max contact resistance change when tested per MIL-STD 202, Method 103B
Temperature soak: 10 mΩ max contact resistance change when exposed to 105°C temperature for 48 hours

MATERIALS

Body — CFP Series — PES (polyether sulfone) glass filled UL 94 V-0
Temperature: −65°C to 170°C
Contact — Beryllium copper
Plating:† Overall gold plate min 4 μin over min 70 μin nickel plating

†For additional plating option consult the factory.
Dimensional drawings available from factory.

SMALL OUTLINE FLAT PACK (CFPH/K SERIES)

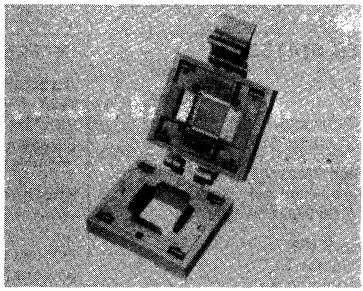


PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C — TI Series socket
- XX — Style FP — Flat pack
- X — Configuration
  - H — 14, 16, 18, 20 Positions
  - K — 24, 28 Positions
- XXX — Number of positions
- XX — Plating: 37 — overall gold plate
- 01

QUAD FLAT PACK (CFPM SERIES)

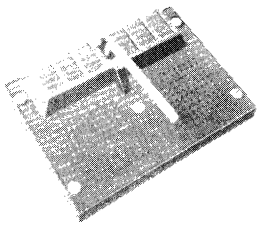


PART NUMBER SYSTEM

CXX X – XXX – XX – 01X

- CXX — TI socket
  - Style PF — Flat pack
- X — Configuration
  - M — Quad pack
- XXX — Number of positions
- XX — Plating: 37 — overall gold plate
- 01X — Variations
  - A — 1.0 mm ℄ contact spacing
  - B — 0.8 mm ℄ contact spacing

PIN GRID ARRAY (CZFW SERIES)



PART NUMBER SYSTEM

C XX X – XXX – XX – 01

- C — TI Series socket
- XX — Style ZF — Zero force
- X — Configuration
  - W — 11 × 11 × 2
- XXX — Number of positions
- XX — Plating: 37 — overall gold plate
- 01

AVAILABLE SIZES

CFPH Series 14, 16, 18, 20	Small Outline
CFPK Series 24, 28	Flat Pack
CFPM Series 64, 80	Quad Flat Pack
CZFW Series 11 × 11 × 2	Pin Grid Array

Contact factory for detailed information

For more information contact your local distributor or contact TI directly:

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Introduction

A new packaging system, *SMti*™ Tape and Reel, has emerged along with the introduction of surface-mount semiconductor packages by Texas Instruments.

Benefits

SMti Tape and Reel not only offers a new shipping method that protects components from mechanical and electrical damage, but also includes the benefits of automated inventory control, ship to stock, and total compatibility with today's automated placement systems. *SMti* Tape and Reel continues the trend towards industry automation and cost reduction and contributes to the overall goal of electronic system quality and reliability.

Features

The features of *SMti* Tape and Reel packaging are as follows.

- *SMti* Tape and Reel packaging is in full compliance with EIA Standard 481-A, "Taping of Surface-Mount Components for Automatic Placement."
- Industry-compatible tape format allows second sourcing without costly and time-consuming equipment changeovers and record-keeping changes.
- Static-inhibiting materials, used in carrier tape manufacture, provide device protection from static damage.
- Rigid, dust-free polystyrene reels provide mechanical protection and clean room compatibility for optimum equipment operation and manufacturing yield.
- Completely compatible with dereeling equipment currently available on most high-speed automated placement systems.
- Medium-density Code 39 bar coding enables inventory and manufacturing automation, as well as complete component traceability prior to, during, and after system manufacture.
- Efficient packaging offers savings in storage space and manufacturing overhead.

General Description

***SMti* Tape and Reel offers users of surface-mounted semiconductor devices a new and efficient method of component handling. Tape and reel consists of three major elements: a carrier tape, a cover tape, and a reel.**

Carrier Tape

The carrier tape is a conductive material with custom-embossed pockets for a particular surface-mount package. Components are oriented in the embossed pockets per EIA 481-A specification "Taping of Surface-Mount Components for Automatic Placement."

Cover Tape

With each component in its embossment and protected from mechanical and static damage, a continuous opaque cover tape is heat sealed over the entire length of the carrier tape, isolating each component from the outside environment. This heat-sealing process guarantees sufficient seal strength to prevent components from falling from the pockets before use. The cover tape has a peel strength of 40 $\pm$ 30 grams in compliance with EIA 481-A and sufficient strength to ensure consistency during dereeling operations.

Reel

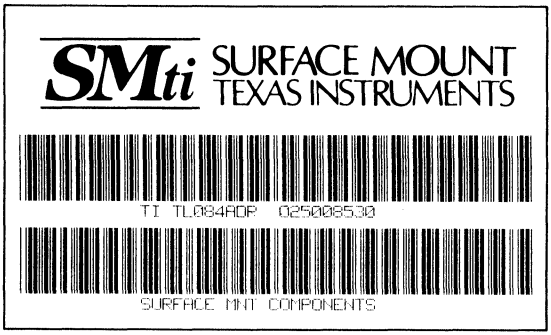
The entire assemblage is wound on a high-strength polystyrene based reel. The reel provides a means of easy storage and handling as well as a method for feeding large quantities of packages to high-speed placement systems. In addition, *SMti* Tape and Reel offers a factory-automation alternative through the use of medium-density Code 39 bar coding on all reel assemblies. The bar code provides source, part number, date code, and quantity.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Bar-Code Labeling

Each reel of *SMti* components is labeled with a "man-and-machine" readable label that uses a medium-density Code 39 bar code in combination with alphanumeric characters.

Figure 1 ***Bar-Code Label***



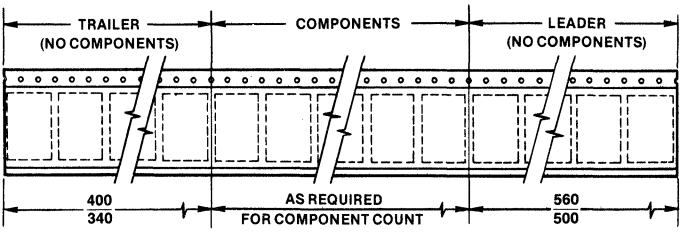
Notes

1. Sample labels are available for system compatibility testing.

Specification

***SMti* Tape and Reel components are available in formats that are compatible with most industry standard component loading and tape drive equipment. Figures 2 through 6 and Tables 1 through 6 provide information regarding these formats. All dimensions are given in millimeters.**

Figure 2 ***Tape Format***



Notes

1. Carrier tape is conductive with a resistivity value of less than 1×10^5 ohms per square.
2. Cover tape is sealed over the entire length of the carrier tape.

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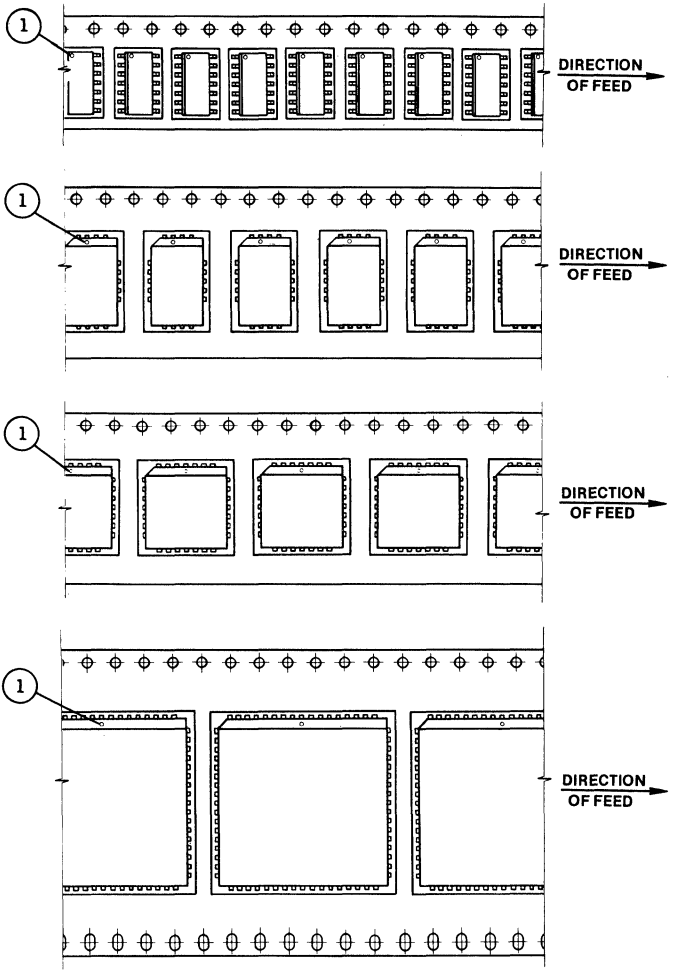
Figure 3 ***Component Format*** (All components are packaged per Note 1.)



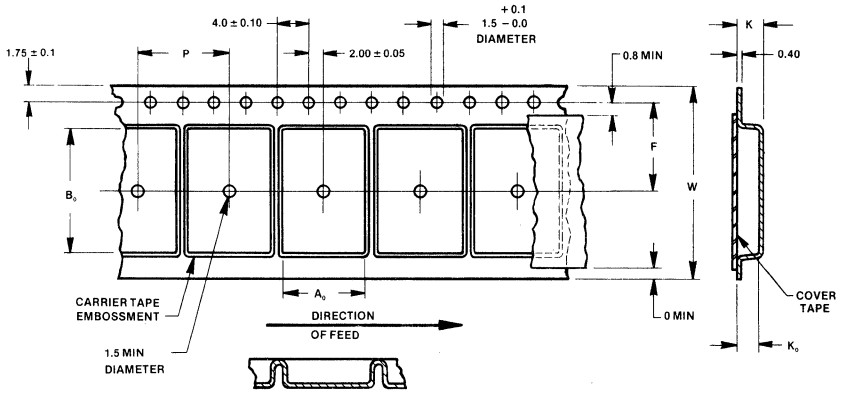
Note

1. Pin #1 orientation.

Specification (Continued)

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 4 ***Single-Sprocket Tape Dimensions***



Notes

1. Tape widths are 12, 16, and 24 mm.
2. Camber per EIA Standard 481-A.
3. Minimum bending radius per EIA Standard 481-A.

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Table 1 ***Single-Sprocket Variable Tape Dimensions***

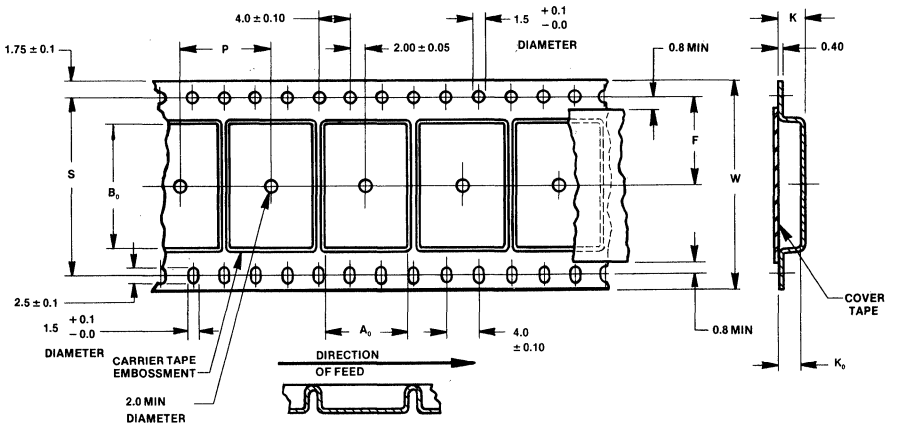
Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
SO-8	D	12	8	6.4	5.2	2.1	2.5	5.5*
SO-14	D	16	8	6.5	9.5	2.1	2.5	7.5
SO-16	D	16	8	6.5	10.3	2.1	2.5	7.5
SO-16L	DW	16	12	10.9	10.7	3.0	3.4	7.5
SO-20L	DW	24	12	10.9	13.2	3.0	3.4	11.5
SO-24L	DW	24	12	10.9	15.8	3.0	3.4	11.5
SO-28L	DW	24	12	10.9	18.3	3.0	3.4	11.5
PLCC-18	FP**	24	12	8.7	12.2	3.75	4.1	11.5
PLCC-18	FM	24	12	8.7	13.9	3.75	4.1	11.5
PLCC-22	FM	24	12	8.7	13.9	3.75	4.1	11.5
PLCC-32	FM	24	16	12.9	15.5	3.75	4.1	11.5
PLCC-20	FN	16	12	10.3	10.3	4.9	5.3	7.5
PLCC-28	FN	24	16	13.0	13.0	4.9	5.3	11.5
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

*Tolerance for this part is: ±0.05.
**FP is a package designator for TMS4164 and TMS4416.

Specification (Continued)

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

Figure 5 ***Double-Sprocket Tape Dimensions***



Notes

1. Tape widths are 32, 44, and 56 mm.
2. Camber per EIA Standard 481-A.
3. Minimum bending radius per EIA Standard 481-A.

Variables are used in Figures 4 and 5 and Tables 1 and 2. The definitions for the variables are as follows: W is tape width, P is pocket pitch, A_0 is pocket width, B_0 is pocket length, K_0 is pocket depth, K is maximum tape depth, and F is the distance between the drive hole and the centerline of the pocket. All dimensions are given in millimeters.

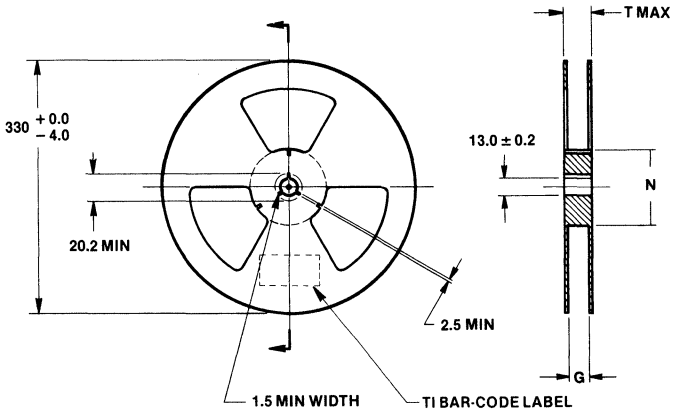
Table 2 ***Double-Sprocket Variable Tape Dimensions***

Package Type	Package Designator	Dimension W	P	A_0	B_0	K_0	K	F
PLCC-44	FN	32	24	18.0	18.0	4.9	5.3	14.2
PLCC-52	FN	32	24	20.5	20.5	5.3	5.7	14.2
PLCC-68	FN	44	32	25.6	25.6	5.3	5.7	20.2
PLCC-84	FN	44	36	30.7	30.7	5.3	5.7	20.2
PLCC-100	FN	56	40	35.8	35.8	5.3	5.7	26.2
PLCC-124	FN	56	48	43.4	43.4	5.3	5.7	26.2
Tolerance		±0.3	±0.1	±0.1	±0.1	±0.1	max	±0.1

Specification (Continued)

Variables are used in Figure 6 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Figure 6 *Reel Dimensions*



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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Variables are used in Figure 6 and Table 3. The definitions for the variables are as follows: G is the distance between the flanges, T is the maximum reel width, and N is the diameter of the reel hub. All dimensions are given in millimeters.

Table 3 *Variable Reel Dimensions*

Package Type	Package Designator	Dimension G	T	N
SO-8	D	12.4	18.4	100
SO-14	D	16.4	22.4	100
SO-16	D	16.4	22.4	100
SO-16L	DW	16.4	22.4	100
SO-20L	DW	24.4	30.4	100
SO-24L	DW	24.4	30.4	100
SO-28L	DW	24.4	30.4	100
PLCC-18	FP*	24.4	30.4	100
PLCC-18	FM	24.4	30.4	100
PLCC-22	FM	24.4	30.4	100
PLCC-32	FM	24.4	30.4	100
PLCC-20	FN	16.4	22.4	100
PLCC-28	FN	24.4	30.4	100
PLCC-44	FN	32.4	40.4	100
PLCC-52	FN	32.4	40.4	100
PLCC-68	FN	44.4	52.4	150
PLCC-84	FN	44.4	52.4	150
PLCC-100	FN	56.4	64.4	150
PLCC-124	FN	56.4	64.4	150
Tolerance		+2.0	max	±2.0

*FP is a package designator for TMS4164 and TMS4416.

Specification (Continued)

All dimensions are given in millimeters.

Table 4 *Tape and Reel Format Summary*

Package Type	Package Designator	Tape Width	Package Pitch	Pocket Dimensions Width	Length	Depth	Reel Diameter	Reel Hub Diameter	Parts Per Reel
SO-8	D	12	8	6.4	5.2	2.1	330	100	2500
SO-14	D	16	8	6.5	9.0	2.1	330	100	2500
SO-16	D	16	8	6.5	10.3	2.1	330	100	2500
SO-16L	DW	16	12	10.9	10.7	3.0	330	100	1000
SO-20L	DW	24	12	10.9	13.2	3.0	330	100	1000
SO-24L	DW	24	12	10.9	15.8	3.0	330	100	1000
SO-28L	DW	24	12	10.9	18.3	3.0	330	100	1000
PLCC-18	FP*	24	12	8.7	12.2	3.75	330	100	1000
PLCC-18	FM	24	12	8.7	13.9	3.75	330	100	1000
PLCC-22	FM	24	12	8.7	13.9	3.75	330	100	1000
PLCC-32	FM	24	16	12.9	15.5	3.75	330	100	1000
PLCC-20	FN	16	12	10.3	10.3	4.9	330	100	1000
PLCC-28	FN	24	16	13.0	13.0	4.9	330	100	750
PLCC-44	FN	32	24	18.0	18.0	4.9	330	100	500
PLCC-52	FN	32	24	20.5	20.5	5.3	330	100	400
PLCC-68	FN	44	32	25.6	25.6	5.3	330	150	250
PLCC-84	FN	44	36	30.7	30.7	5.3	330	150	250
PLCC-100	FN	56	40	35.8	35.8	5.3	330	150	100
PLCC-124	FN	56	48	43.4	43.4	5.3	330	150	100

*FP is a package designator for TMS4164 and TMS4416.

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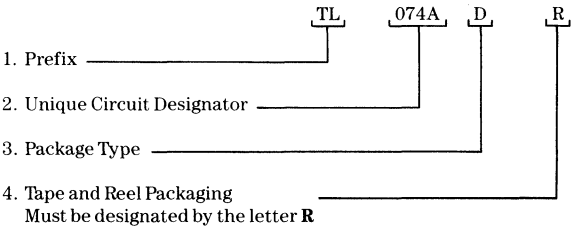
Ordering Information

To order tape and reel components, you need to provide information about part numbers, quantities, shipping, and sample package applications.

Ordering by Part Number

When ordering tape and reel components, add the letter **R** as a suffix to the part number. An example of the ordering sequence follows.



Formats and Quantities

All orders for tape and reel packaging **must be for whole reels**. For example, if a customer requires 9,900 TL074's in Tape and Reel packaging, he needs to place the order for a quantity of 10,000 TL074's. The order will be filled and shipped on four reels containing 2,500 parts per reel.

Note: TI reserves the right to provide a smaller quantity of devices per reel to preserve date code integrity.

A list of package and tape formats and the quantity of devices per reel is provided in Table 5.

Shipping

Taped and reeled components are shipped in individual packing boxes measuring approximately 14″ × 14″. The depth of each box is tailored to the tape width. Individual boxes are packed in a larger box whose size depends on the quantity of components ordered.

Ordering Information (Continued)

All dimensions are given in millimeters.

Table 5 *Condensed Tape and Reel Formats*

Package Type	Package Designator	Tape Width	Package Pitch	Reel Diameter	Parts Per Reel
SO-8	D	12	8	330	2500
SO-14	D	16	8	330	2500
SO-16	D	16	8	330	2500
SO-16L	DW	16	12	330	1000
SO-20L	DW	24	12	330	1000
SO-24L	DW	24	12	330	1000
SO-28L	DW	24	12	330	1000
PLCC-18	FP*	24	12	330	1000
PLCC-18	FM	24	12	330	1000
PLCC-22	FM	24	12	330	1000
PLCC-32	FM	24	16	330	1000
PLCC-20	FN	16	12	330	1000
PLCC-28	FN	24	16	330	750
PLCC-44	FN	32	24	330	500
PLCC-52	FN	32	24	330	400
PLCC-68	FN	44	32	330	250
PLCC-84	FN	44	36	330	250
PLCC-100	FN	56	40	330	100
PLCC-124	FN	56	48	330	100

*FP is a package designator for TMS4164 and TMS4416.

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Sample Package Applications

Sample components are available for a number of applications, such as standard mechanical sample packages, "daisy-chained" bars, and K-factor bars. Table 6 provides sample ordering information.

Table 6 ***Sample Package Applications***

Package Type	Package Designator	Mechanical Sample	Daisy Chain	K Factor
SO-8	D	SN102589	SN102590	N/A
SO-14	D	SN72197	SN200054	SN200060
SO-16	D	SN72198	SN200055	SN200061
SO-16L	DW	N/A	N/A	N/A
SO-20L	DW	SN72199	SN200056	SN200062
SO-24L	DW	SN72200	SN200057	SN200063
SO-28L	DW	N/A	N/A	N/A
PLCC-18	*	TMS1864MS	TMS1864DC	TMS1864KF
PLCC-18	*	TMS18256MS	TMS18256DC	TMS18256KF
PLCC-22	*	TMS22464MS	TMS22464DC	TMS22464KF
PLCC-32	FM	N/A	N/A	N/A
PLCC-20	FN	SN72201	SN200058	N/A
PLCC-28	FN	SN72202	SN200059	N/A
PLCC-44	FN	SN102767	SN102768	N/A
PLCC-52	FN	N/A	N/A	N/A
PLCC-68	FN	SN750002	SN750003	N/A
PLCC-84	FN	N/A	N/A	N/A
PLCC-100	FN	N/A	N/A	N/A
PLCC-124	FN	N/A	N/A	N/A

*The type of package is indicated by MS, DC, or KF at the end of the part number.

More Information

As a major manufacturer of SMCs, TI is committed to helping you make the transition to surface-mount as easy and as economical as possible. Getting started in SMT—switching from older and less efficient methods of PCB fabrication—means learning some new manufacturing techniques, and it entails some capital outlay. But in volume production, it can actually reduce your capital and space costs by up to 50 percent.

Ship-to-Stock Eliminates Incoming Inspection

As your usage per surface-mount component (SMC) grows, TI can implement its ship-to stock program for you. With all the necessary quality-control procedures built into our standard testing process, your SMCs can be shipped directly to you in tape and reel or in factory-sealed boxes. Benefits to you:

- Incoming inspection, scrap, and rework reduced or eliminated.
- Inventory reduced.
- Quality levels maximized.

Learn by Doing

To help you realize the advantages of surface-mount technology (SMT), Texas Instruments maintains a surface-mount laboratory. There you can gain hands-on experience and guidance in building a surface-mount board from start to finish. To schedule an appointment, contact your TI Field Sales Engineer or call (800) 232-3200 for the address of the TI Field Sales Office nearest you. A description of the lab's equipment and services is available from TI.

Outside Help Available

You can also find assistance among the growing number of SMT assembly houses, consultants, and associations. They can help you reduce the costs of converting to SMT, while supplying some valuable information on the latest technological advances and industry standards.

Suppliers of assembly equipment such as pick-and-place machines and soldering and test equipment can also help you make the transition to SMT board fabrication. A current list of these suppliers is available from TI.

Want to Learn More?

How to Use Surface Mount Technology is available free of charge from Texas Instruments. This technical summary includes chapters on the process and the tooling required to implement it; the wide variety of available SMCs; inspection, testing, and repair; quality and reliability; and how to mix SMCs with standard DIP packages.

For additional information on the availability of TI's growing line of SMCs, contact your local TI Field Sales Office or distributor.

If you would like to have your name placed on our mailing list for additional SMT information as it becomes available from TI, please write Texas Instruments Incorporated, Dept. SSP05, P.O. Box 809066, Dallas, Texas 75380-9066.

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Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to the following:

1) All discrete semiconductors and ICs
2) Hybrid microcircuits
3) Thin film passive devices.

Definitions

1. Antistatic material: ESD protective material which minimizes the generation of static charges when rubbed against or separated from itself or other similar materials.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^{12} Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.
4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: Equipment that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

1. For the purpose of this specification, all microelectronic devices are considered to be ESDS Class 1. ESDS Class 1 devices require minimum protective packaging of a conductive container or an antistatic container within an electrostatic field shielding barrier.
2. Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls:

1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of

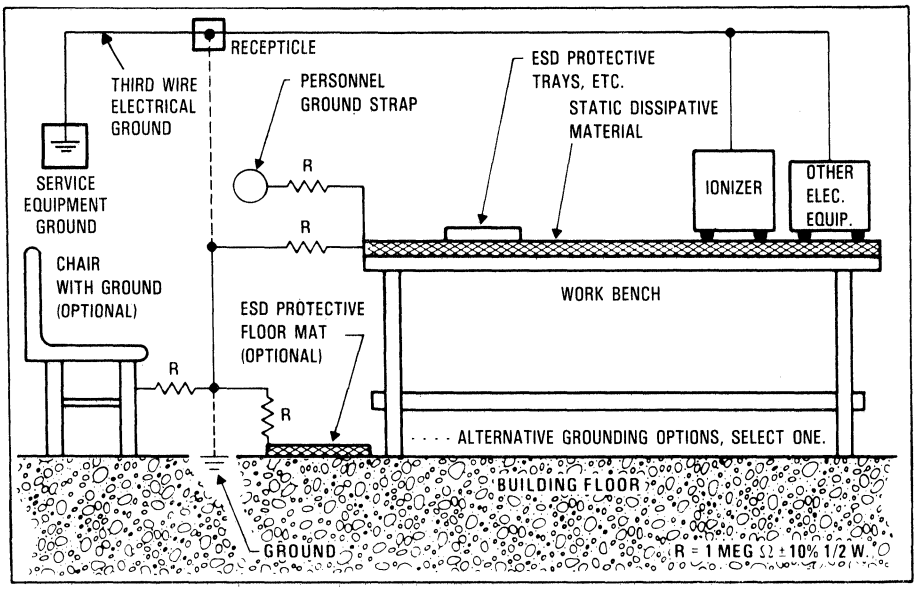
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual
8) EIA-541 Packaging Material Standards for ESD Sensitive Items

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with static dissipative material attached to ground through a 1 MΩ ±10% resistor, an attached grounding wrist strap with integral 1 MΩ ±10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. If no insulator materials are present at the work station, operators may wear static dissipative smocks in lieu of using an ionizer. The wrist strap shall be connected to the static dissipative material at the same metallic button or contact used to ground the material. Ground must utilize either earth ground or third wire (green) electrical ground, refer to Figure 1. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps for nonseated personnel. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 1.



All electrical equipment sitting on the static dissipative work surface must be hard grounded and must be isolated from the static dissipative work surface. Ground fault circuit interrupter (GFCI) is recommended for operator safety.

NOTE: Earth ground consists of a metal pipe or rod inserted at least three (3) feet into the earth. All static-free work stations in a single building may utilize a single earth ground.

Figure 1. Static-Free Work Station

Table 1. General Grounding Requirements

	ANTISTATIC, STATIC DISSIPATIVE OR CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Eqipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubs	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor.

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation:

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information or its equivalent.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 40%-60%.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a static dissipative work surface connected to ground through a 1 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the static dissipative work surface, and an ionizer constitute a static-free work station (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. If possible, operators should avoid touching leads or contacts even though grounded.

CAUTION

Personnel shall never be attached to ground without the presence of the 1 MΩ ± 10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static-sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots, cotton gloves, antistatic gloves or conductive gloves (free of reactive elements such as chlorine, phosphorus, etc.) may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the static dissipative bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle.
5. All operations on the items should be performed with the items in contact with the static dissipative bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.
6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe/heel strap may be used along with conductive tile/mats.

8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station. (See exception in FACILITIES FOR STATIC-FREE WORK STATION.)
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags are prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only be a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATIONS FOR WORKING AT STATIC-FREE WORK STATIONS.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.
2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.

3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas**.
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION**. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS**, item 2.
3. Any void-fillers shall be made of an antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Wrist Straps (once a day)

Wrist straps shall be checked for minimum resistance to provide operator safety and maximum resistance to insure that proper body contact is maintained to drain generated charges. A go-no-go tester may be used provided it checks to a minimum of no less than 500 kΩ and a maximum of no greater than 2 MΩ.

Ground Continuity (minimum of once a month)

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ $\pm$10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week)

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week)

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week)

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month)

Conductive floors must have a resistance of not less than 100 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 100 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 99.

Records

Written records must be kept of all these QC audits.

TRAINING

Training is applicable for all areas where individuals come in contact with ESDS (Class 1) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

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